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Description	

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Ferroelectric-Gate Thin-Film Transistor Fabricated by Total Solution Deposition Process

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Abstraction

We have fabricated inorganic ferroelectric-gate thin film transistors (FGTs) using only a chemical solution deposition (CSD) process. All layers, including the $LaNiO_3$ (LNO) gate electrode, $Pb(Zr,Ti)O_3$ (PZT) ferroelectric-gate insulator, indium-tin-oxide (ITO) source/drain electrodes , and ITO channel, were formed on a $SrTiO_3$ (STO) substrate by the CSD process. We obtained an local epitaxially grown PZT/LNO perovskite hetero-structure with good crystalline quality and no interfacial layer. The fabricated FGT exhibited typical n-channel transistor operation, with a counterclockwise hysteresis loop due to the ferroelectric nature of the PZT-gate insulator, and also exhibited good drain current saturation in output characteristics. These properties are equivalent to or better than those obtained with FGTs fabricated by means of conventional vacuum processes. The obtained on/off current ratio, memory window, and subthreshold voltage swing were about 10^5, 2.5 V, and 357 mV/decade, respectively.

KEYWORD: solution process, chemical solution deposition, ferroelectric-gate, thin-film transistor, FeRAM, nonvolatile memory, $Pb(Zr, Ti)O_3$, $LaNiO_3$, ITO, oxide semiconductor

1. Introduction

A ferroelectric-gate field-effect transistor has attracted much attention as a nonvolatile memory element with low power consumption, high speed, and high endurance owing to the ferroelectric nature and such a transistor is applicable for various applications including wireless IC cards and tools for mobile communications.[1,2)] Among the ferroelectric-gate memory transistors, Si-based ferroelectric-gate transistors have been studied most intensively for random access memory (FeRAM) applications and several reports have demonstrated good electrical properties.[3,4)] However, the Si-based ferroelectric-gate

memory transistors still are not used practically because they suffer from two major problems. The first problem is that it is very difficult to obtain a good interface between the ferroelectric layer and the silicon substrate. It is well known that high crystallization temperature used to deposit ferroelectric films promotes the interdiffusion of constituent elements of the ferroelectric layer into Si substrate and formation of an interfacial layer between the ferroelectric layer and the silicon substrate, which leads to poor electrical properties. To prevent such an interdiffusion, multi-stacked structures including a buffer layer such as a metal-ferroelectric-insulator-semiconductor (MFIS) or metal-ferroelectric-metal-insulator-semiconductor (MFMIS) have been used to fabricate Si-based ferroelectric-gate memory transistors.[5-7] The second problem involves charge mismatch. More specifically, the remanent polarization of polycrystalline ferroelectric films is typically 10-35 $\mu C/cm^2$, whereas the charge density needed to control the conductivity of the MOSFET channel is generally calculated to be no greater than 1.5 $\mu C/cm^2$. Even if a breakdown field is applied to the SiO_2-gate insulator in an MFIS stacked structure, the induced charge is limited to about 3.5 $\mu C/cm^2$. Therefore, the full polarization (saturated polarization loops) of the ferroelectric-gate insulator in Si-based memory transistors cannot be utilized. MFMIS stacked structures, which equivalently reduce the full ferroelectric polarization by increasing the area of the lower MIS capacitor as compared with the upper MFM capacitor, have been used to overcome this problem. However, such a complicated structure is not suitable for low-cost-fabrication and for high integration, because the area of the MIS capacitors must be much larger than that of the MFM capacitors. Because of these problems, it would be difficult for the Si-based ferroelectric-gate memory transistors to realize low-cost processing and high-density implementation.

On the other hand, oxide-based ferroelectric-gate thin-film transistors (FGTs) could be one of the most promising candidates for low-cost, high-performance, highly integrated devices, because FGTs do not require a Si substrate and thus do not require complicated processing, because FGTs have a very simple oxide-semiconductor/ferroelectric stacked structure and can be fabricated by only deposited films. In addition, unlike Si-based memory transistors, this type of memory can use full ferroelectric polarization without charge-mismatch problem because a conductive oxide channel can be directly deposited on the FGT's ferroelectric-gate insulator. We have already reported good transistor operation of FGTs using a $(Bi,La)_4Ti_3O_{12}$[8,9] or $Pb(Zr,Ti)O_3$ (PZT)[10] film as a gate insulator and an indium-tin-oxide (ITO) film as a channel. Note that ITO, which is a conductive oxide with a high carrier concentration, can be used as a channel owing to the huge charge density of the ferroelectric-gate insulator (10–35 $\mu C/cm^2$). In our previous work, we mainly used conventional vacuum deposition processes to fabricate FGTs which results in high processing costs. To further reduce the processing costs associated with FGTs, we investigated solution deposition processes for FGT fabrication in this study.

The replacement of the conventional vacuum deposition processes by solution deposition processes would facilitate low-cost processing because of the low equipment costs and process simplicity associated with solution deposition process. Furthermore, solution deposition processes enable us to use direct patterning of FGTs by means of printing techniques. In recent years, inorganic transistors with paraelectric-gate and ferroelectric-gate insulators fabricated with solution-derived films have been reported. Those transistors used various materials for the channel layer such as ZnO,[11-13) In-Zn-O,[14,15) In_2O_3,[16) ITO,[8-10,17) and Si-based channels.[6) However, solution-based fabrication processes were used for only some parts of those transistors' fabrication processes, and conventional vacuum deposition processes were used for the rest of the transistor parts. To achieve ultra-low-cost and ultra-low-energy fabrication, a total solution-based process should be employed, in which all parts of the device are fabricated from solution-derived materials only. This total solution processing could eventually lead to "total printing electronics" for further cost reduction.

In this study, we investigated FGT fabrication in which all layers were fabricated by a chemical solution deposition (CSD) process. We used $LaNiO_3$ (LNO) film as a gate electrode on which a PZT ferroelectric gate insulator was formed, and ITO films were used both for the channel and source-drain electrodes. The fabricated FGT had a bottom gate electrode and bottom source-drain electrodes on a single-crystal $SrTiO_3$ (STO) substrate as shown in Fig. 1(a). Fig. 1(b) shows the magnified top-view microscope image of this device. We adopted LNO film as a gate electrode to obtain PZT films with good crystalline quality and electrical properties, because LNO is a perovskite-type conductive oxide with a lattice constant of a=~3.86 Å that is compatible with that of PZT (a=~4.01 Å).

2. Experimental Procedure

To prepare the FGT, the LNO bottom gate (100 nm) was first formed by the CSD process. A precursor solution of LNO film was prepared by dissolving 0.1mol/kg lanthanum nitrate hexahydrate [$La(NO_3)_3 \cdot 6H_2O$] and 0.1mol/kg nickel acetate tetrahydrate [$Ni(OAc)_2 \cdot 4H_2O$] in 2-methoxyethanol at 80 °C for 10min. The LNO precursor solution was spin coated on STO(110) substrate, dried at 160 °C in air for 5min and then crystallized at 750 °C in O_2 for 15min. Then, the LNO gate electrode was patterned by photolithography and wet-etching. In the second step of the FGT fabrication, the $Pb_{1.2}Zr_{0.4}Ti_{0.6}O_3$ (PZT) gate insulator (225 nm) was formed by the CSD process. We used an alkoxide-based 8wt% PZT precursor solution. This solution was spin coated, dried at 240 °C in air for 10min and consolidated at 400 °C in air for 10min. Then, a gate contact hole was formed by photolithography and wet-etching. After that, the PZT film was crystallized at 625 °C in air for 15min. In the third FGT fabrication step, the ITO source-drain electrodes (200 nm) were formed by the CSD process using a

carboxylate-based ITO precursor solution (5 wt% SnO_2-doped). This solution was spin coated on the PZT layer, consolidated at 300 °C in air for 10 min and patterned by photolithography and wet-etching. After the exposed PZT surface (the channel region) was treated by Ar plasma, the ITO source-drain electrodes were crystallized at 600 °C in air for 15min. Finally, the ITO channel (20 nm) was fabricated by the CSD process. The ITO precursor solution was spin coated, consolidated at 300 °C in air for 10min and patterned by photolithography and wet-etching followed by crystallization at 450 °C in air for 40min. The channel length (L_{SD}), channel width (W) and gate electrode width (L_G) of the fabricated device were 5-30μm, 60μm and 50μm, respectively.

Structural characterization of films were carried out by X-ray diffraction (XRD) analysis, cross-sectional transmission electron microscope (TEM) observation, TEM-EDX (energy dispersive X-ray spectroscopy), and transmission electron diffraction (TED) analysis. The resistivity of LNO films was measured by a four probes method. The carrier density and resistivity of ITO films were measured by the van der Pauw method using Hall-effect measurement system (Accent HL5500). The transfer characteristics (I_D-V_G), output characteristics (I_D-V_D) and leakage current property were measured by semiconductor parametric analyzer (Agilent 4155C).

3. Results and Discussion

3.1 Structural properties

Fig. 2(a) shows an XRD spectrum obtained from the PZT/LNO/STO(110) perovskite hetero-structure. We annealed LNO and PZT films at 750 °C and 625 °C, respectively, because the annealing temperature of LNO film should be higher than that of PZT from a process stability point of view. We found that both LNO and PZT films exhibited a (110) preferred orientation that was induced from the single-crystal STO(110) substrate. Fig. 2(b) shows a cross-sectional TEM image of the PZT/LNO hetero-interface region and TED patterns of PZT and LNO films. The TEM image reveals that the PZT/LNO interface almost does not have any interfacial layers which would have prevented good crystal growth and electrical properties of the PZT films. A lattice structure in both the LNO and PZT films also can be observed in the TEM image. Clear diffraction spots appeared in the TED patterns, indicating that high-quality crystalline LNO and PZT films were obtained even in the solution-derived stacked structure. The TED patterns also indicate that (110)-oriented PZT/LNO hetero-structure was almost epitaxially grown on STO substrate, with a measured lattice mismatch of less than 5%.

Fig. 3(a) shows a cross-sectional TEM image of the ITO-channel (20 nm)/PZT (225 nm) interfacial region in the FGT device fabricated in this work. The PZT and ITO-channel layers were annealed at 625 °C and 450 °C, respectively. As shown in the image, we observed an interfacial layer around 4 nm thick

which was rather porous and constructed by double layers, i.e. upper layer and lower one. TEM-EDX line analysis was carried out across the ITO-channel/PZT interface, including these double interface layers and it is revealed that In and Sn atoms, the elements of the ITO film, diffused slightly to the upper interface layer, whereas Pb, Zr, and Ti atoms, the elements of the PZT film, exhibited inhomogeneous atomic diffusion. In particular, Zr and Ti atoms were segregated in the upper and the lower interface layer, respectively. The relative atomic composition ratio of Pb/Zr/Ti in the upper and the lower interface layers were about 11/58/29 and 25/27/48, respectively. These inhomogeneous interfacial layers are suspected to have some serious influences on the electrical properties of FGTs fabricated in this study. Fig. 3(b) shows TED patterns of ITO-channel. Debye-Scherrer rings, halo patterns and rather bright spots were observed together in the TED image, indicating that the 450 °C-anneal ITO-channel has not been fully crystallized, but still kept small amount of amorphous-like phase in it.

3.2 Electrical properties

Fig. 4 shows the dependence of the annealing temperature on the resistivity of LNO films (100 nm) fabricated on STO(110) substrates. The resistivity was measured by using the four-probe method. As the figure shows, resistivity less than 10^{-3} Ωcm, which is lower than the reported one,[18-22] was obtained when the film was annealed at higher than 600 °C.

Fig. 5 shows the resistivity and carrier density of ITO films (20 nm) measured by using the van der Pauw method. The resistivity of the 20-nm-thick ITO thin film decreased with increasing annealing temperature, whereas the carrier density increased with increasing annealing temperature. Notably, ITO was used both as a channel layer and for the source-drain electrodes in the FGTs prepared in this study. Because a channel requires an appropriate carrier density for its complete depletion, whereas the electrodes require low resistivity, we prepared these two types of ITO films under different annealing conditions according to the results shown in Fig. 3. In particular, a 450 °C-annealed ITO film was used for the channel to achieve a carrier density of 4.8×10^{19} cm^{-3} and a resistivity of 2.0×10^{-1} Ωcm, while 600 °C-annealed ITO films were used for the source-drain electrodes to achieve a carrier density of 1.0×10^{20} cm^{-3} and a resistivity of 1.8×10^{-2} Ωcm.

Fig. 6 shows the polarization-voltage (*P-V*) hysteresis loops of ITO/PZT/LNO (200 nm/225 nm/100 nm) capacitor measured by applying voltage to the LNO electrode with ITO electrode grounded. We annealed ITO, PZT and LNO films at 600 °C, 625 °C and 750 °C, respectively. The obtained remanent polarization (P_r) is about 30 μC/cm^2, which is a typical P_r value for a PZT. On the other hand, according to the carrier concentrations of ITO films shown in Fig.5, the charge per unit area of an ITO film annealed at 450 ºC was calculated to be as low as 9.6 μC/cm^2, which was smaller than the P_r of PZT

film. This difference in charge densities indicates that the huge polarization charge of the PZT film could deplete all the electrons in a 20-nm-thick ITO film. If a paraelectric SiO_2 film was used as a gate insulator, controlling all the charge in ITO channel (9.6 μC/cm^2) would be impossible, because the maximum charge of such an SiO_2 film is generally limited to only 3.5 μC/cm^2 even at the breakdown voltage of around 10 MV/cm.

Fig.7 shows the I_D-V_G and I_D-V_D characteristics of the fabricated FGT device. For I_D-V_G characteristics, we obtained a typical n-channel transfer curve with a counterclockwise hysteresis loop at low operation voltage (less than ±10 V) owing to the ferroelectric nature of the PZT gate insulator, and for I_D-V_D characteristics we observed good drain current saturation. The obtained on/off current ratio and memory window were about 10^5 and 2.5 V, respectively. In addition, we obtained a good subthreshold voltage swing of 357 mV/decade, which probably can be attributed to the large equivalent capacitance of the PZT gate insulator.

We tried to measure the data retention property of FGT fabricated here. To write the data, we applied gate voltage of +10V or -10V with the pulse width of 50μsec. Then, the gate was grounded during the measurement of drain current. It was confirmed that the data was only kept around 1 hour. Such short data retention property may be caused by the formation of inhomogeneous interfacial layers between ITO-channel and PZT-gate insulator as shown in Fig. 3(a). This issue would be improved by introducing some cap layers on PZT surface to stabilize both of PZT and ITO compositions, or by selecting an adequate material combination of channel and gate insulator because the wide selectivity of materials is one of the most advantageous points of oxide-based FGTs.

The field-effect mobility, μ_{FE}, was deduced from $\mu_{FE} = I_{ds}[(W / 2L_{SD})C_{ox} \cdot (V_G - V_T)^2]^{-1}$, where I_{ds} is the output current in saturation region, C_{ox} is the equivalent capacitance per unit area of the gate insulator, V_G is the gate voltage, V_T is the threshold voltage, W is the channel width and L_{SD} is the channel length. We assumed equivalent C_{ox} as $P(V_G) / V_G$ from P-V hysteresis, where $P(V_G)$ is the polarization of the PZT film as a function of the gate voltage. By using the parameters of $P(V_G)$ = 43.1 μC/cm^2, V_G = 7.0 V, V_T = 2.3 V, W = 60 μm and L_{SD} = 5 μm, we estimated the μ_{FE} of this FGT to be 0.08 cm^2/Vs. This apparent low mobility may have been caused by the deficient conductivity of the ITO source-drain electrodes, and this issue could be solved by using a different highly conductive material for electrodes. However, despite the estimated low channel mobility, an adequate on-current was obtained because of the large charge density induced by the ferroelectric-gate insulator.

Next, we investigated the capacitor characterization of the FGT channel (W/L_{SD}= 60μm/20μm) to understand depletion/accumulation dynamics caused by the PZT ferroelectric gate. For that purpose, we used an ITO/PZT/LNO (200 nm/225 nm/100 nm) capacitor with a capacitor area of 1.06×10^{-4} cm^2 as a

reference. This reference capacitor is the same as that shown in Fig. 6. The reference capacitor can behave PZT capacitor because 600 °C-annealed ITO top electrode has higher carrier density, whereas the FGT capacitor contains the channel layer whose conductivity would be changed by field effect from the PZT gate insulator. Fig. 8(a) shows the capacitance-voltage (*C-V*) curves measured for the reference capacitor (ITO/PZT/LNO) and FGT device, and the zoom image of *C-V* curve measured for FGT is shown in Fig. 8(b). The dotted curve shows the *C-V* characteristics of the reference capacitor, and the solid curve shows those of the FGT capacitor. Both curves were measured by applying voltage to the LNO electrode with the ITO electrode or the ITO source-drain electrodes grounded. The *C-V* curve of the FGT capacitor (solid line) exhibits a saturated capacitance at positive applied voltage (C_{on}) that is higher than that at negative applied voltage (C_{off}). This difference between C_{on} and C_{off} suggests that the electrons in the 20-nm-thick ITO channel are accumulated at positive applied voltage and depleted at negative applied voltage. To evaluate the degree of accumulation or depletion quantitatively, we define the effective capacitance area (*ECA*), which is deduced from the equation $ECA = C\,d_{PZT}/\varepsilon_0\varepsilon_r$, where C is the capacitance of the FGT device including C_{on} and C_{off}, d_{PZT} is the thickness of the PZT gate insulator, ε_{r} is the relative permittivity of the 225-nm-thick PZT film, and ε_0 is the vacuum permittivity. We calculated ε_{r} to be 172.7 at positive applying voltage (ε_{ron}) and 168.9 at negative applying voltage (ε_{roff}) from the saturated capacitance of the reference ITO/PZT/LNO capacitor, which is shown as the dotted *C-V* curve in Fig. 8(a). The parameters of C_{on} and ε_{ron} gave an ECA_{on} value of 4.51×10^{-5} cm^2, and C_{off} and ε_{roff} gave an ECA_{off} values of 3.24×10^{-5} cm^2. These effective capacitance areas then were compared with the actual capacitance areas in the FGT device prepared in this work. It can be assumed that the overlapping area (A_{overlap}) between source-drain electrodes and a gate electrode in a FGT always forms a capacitor, regardless of FGT's ON/OFF state. A_{overlap} was 3.29×10^{-5} cm^2 in the FGT used here. If the channel region is depleted at negative applying voltage, it behaves like an insulator. In that case, $\mathrm{ECA}_{\mathrm{off}}$ should be equal to A_{overlap}. The $\mathrm{ECA}_{\mathrm{off}}$ value of 3.24×10^{-5} cm^2 which was calculated here is almost equal to the measured A_{overlap} of 3.29×10^{-5} cm^2 with the difference of less than 2%. This result indicated that the total area of the ITO channel region (W/L_{SD}= 60μm/20μm) became non-conductive; that is, it was depleted. On the other hand, if the channel region is accumulated at positive applying voltage, it behaves like a conductor. In this case, the area between a channel region and a gate electrode (A_{channel}) could form a capacitor. A_{channel} was 1.18×10^{-5} cm^2 in the FGT prepared here. If an accumulation state gives enough conductivity to the channel, the source and drain electrodes would be electrically connected. Hence, $A_{\mathrm{overlap}}+A_{\mathrm{channel}}$ should be comparable to $\mathrm{ECA}_{\mathrm{on}}$, ideally. In the present experiment, $A_{\mathrm{overlap}}+A_{\mathrm{channel}}$ and $\mathrm{ECA}_{\mathrm{on}}$ were calculated to be 4.47×10^{-5} cm^2 and 4.51×10^{-5} cm^2, respectively. $A_{\mathrm{overlap}}+A_{\mathrm{channel}}$ is almost equal to $\mathrm{ECA}_{\mathrm{on}}$ with the difference of less than 1%, indicating that the total area of

the ITO channel region was clearly accumulated by PZT polarization. Thus, in a FGT device fabricated by total solution deposition process, we confirmed that the conductivity of ITO channel region was almost wholly controlled, which lead to high on/off current ratio.

4. Conclusions

In summary, we have fabricated a ferroelectric-gate thin film transistor (FGT) using only CSD processing for all its layers, including the gate electrode, gate insulator, source-drain electrodes and channel. This FGT exhibited equivalent or better transistor operation compared with FGTs prepared by means of vacuum processes.[4,5,23,24] In this study, we proposed that the "total solution process" could be used instead of conventional vacuum processes for fabrication of inorganic ferroelectric-gate thin-film transistors. Use of such a total solution process would represent advancement toward "total printing inorganic electronics" by using printing techniques such as screen printing, inkjet printing, imprinting technique, and so on, which could enable ultra-low-cost and low-energy fabrication of sophisticated inorganic TFTs and memories.

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Figure captions

Fig. 1. (a) Schematic diagram of the FGT structure and (b) top-view microscope image of FGT.

Fig. 2. (a) XRD spectrum obtained from a PZT/LNO/STO stacked structure and (b) cross-sectional TEM image and TED patterns of a PZT/LNO stacked structure.

Fig. 3. (a) Cross-sectional TEM image of the ITO-channel/PZT interfacial region and (b) TED patterns of ITO-channel.

Fig. 4. Resistivity of LNO films on STO(110) substrates as a function of annealing temperature.

Fig. 5. Resistivity and carrier density of ITO films as a function of annealing temperature.

Fig. 6. *P*-*V* hysteresis loops of an ITO/PZT/LNO capacitor.

Fig. 7. (a) I_D-V_G characteristics and (b) I_D-V_D characteristics of an FGT with a 20-nm-thick ITO channel.

Fig. 8. (a) *C*-*V* curves measured for an ITO/PZT/LNO capacitor (doted line) and FGT device (solid line) and (b) is the zoom image of solid line.

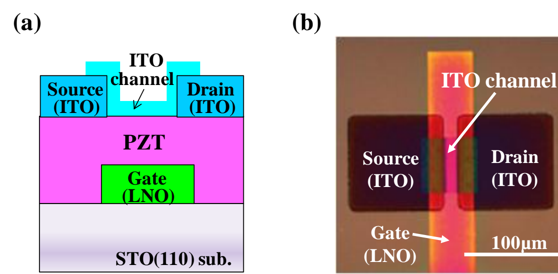

(a)
ITO
channel
Source
(ITO)
Drain
(ITO)
PZT
Gate
(LNO)
STO(110) sub.
(b)
ITO channel
Source
(ITO)
Drain
(ITO)
Gate
(LNO)
100μm

FIG. 2 T. Miyasako *et al.*

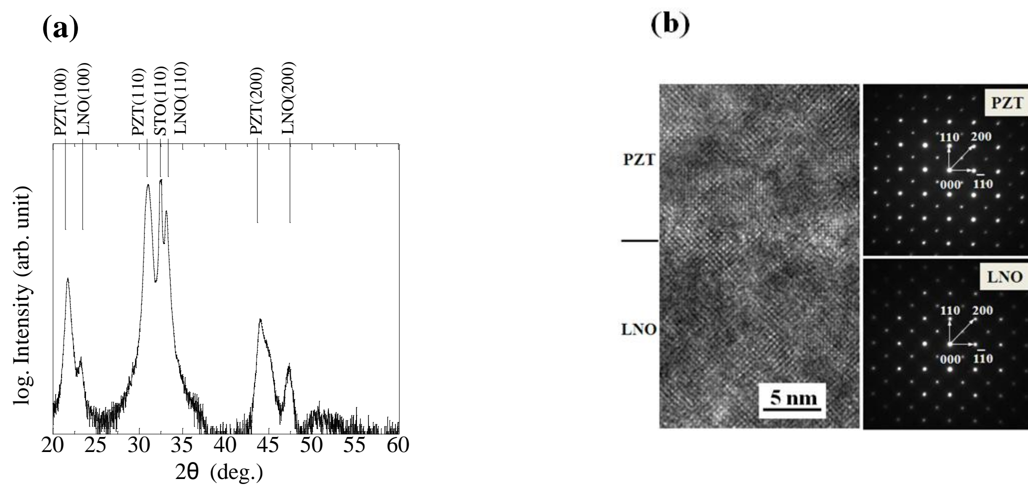


FIG. 3 T. Miyasako *et al.*

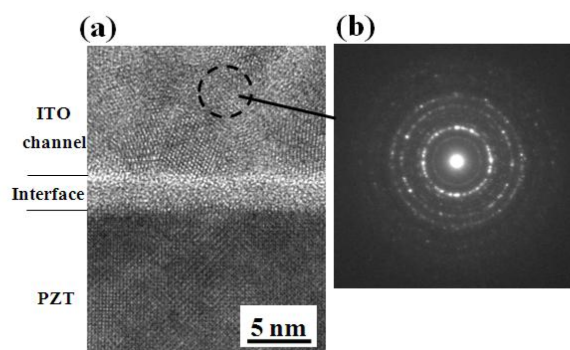
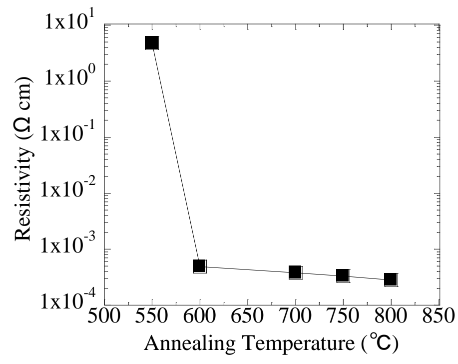


FIG. 4 T. Miyasako *et al.*



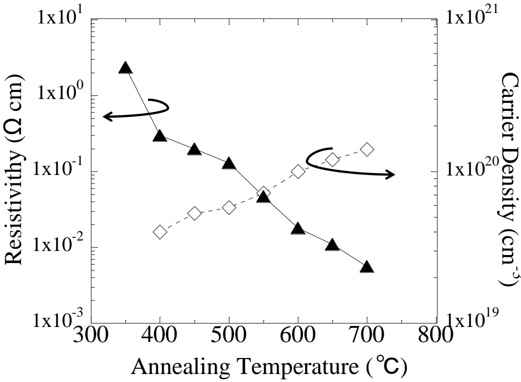

1x10^1
1x10^0
1x10^-1
1x10^-2
1x10^-3
Resistivithy (Ω cm)
1x10^21
1x10^20
1x10^19
Carrier Density (cm^-3)
300
400
500
600
700
800
Annealing Temperature (℃)

FIG. 6 T. Miyasako *et al.*

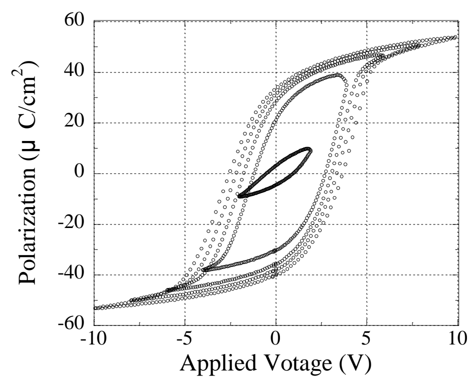
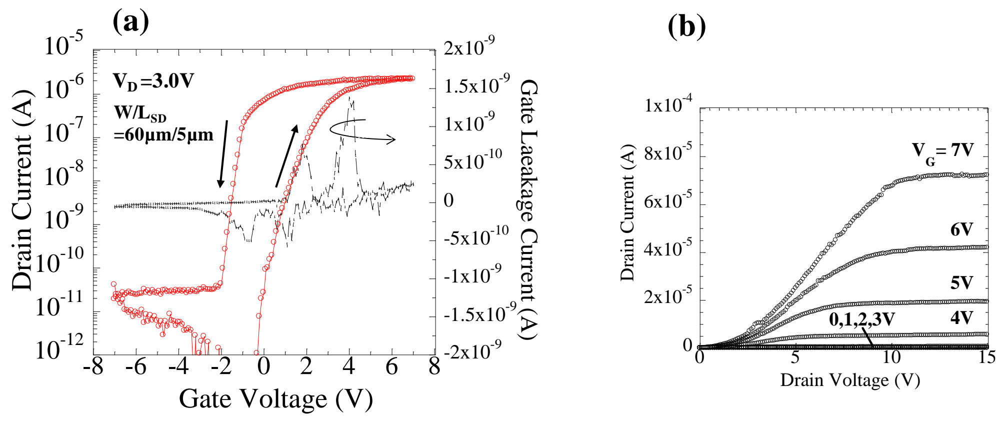
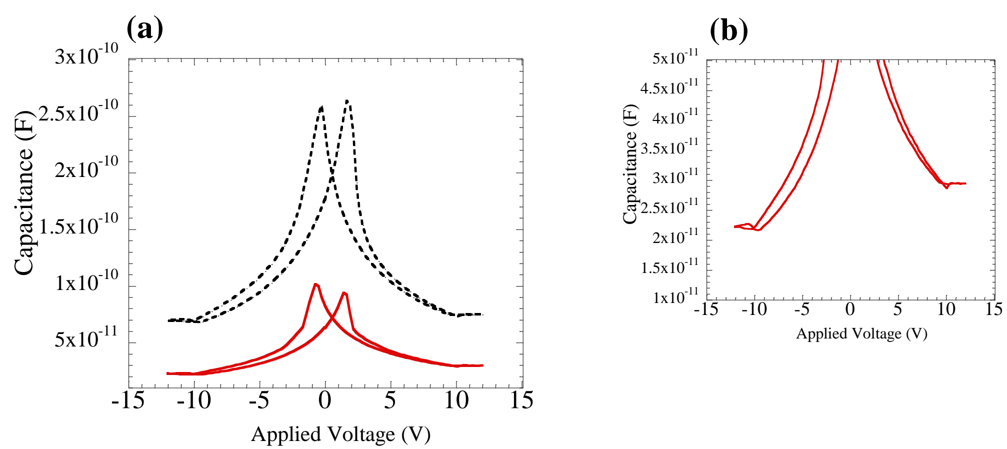


FIG. 7 T. Miyasako *et al.*




(a)
Capacitance (F)
3x10^-10
2.5x10^-10
2x10^-10
1.5x10^-10
1x10^-10
5x10^-11
-15 -10 -5 0 5 10 15
Applied Voltage (V)
(b)
Capacitance (F)
5x10^-11
4.5x10^-11
4x10^-11
3.5x10^-11
3x10^-11
2.5x10^-11
2x10^-11
1.5x10^-11
1x10^-11
-15 -10 -5 0 5 10 15
Applied Voltage (V)