Characterization method for wide-gap metal-insulator-semiconductor devices by using capacitance-frequency-temperature mapping

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DOCTORAL DISSERTATION

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Abstract

Wide-gap semiconductor GaN is anticipated for its potential to overcome the trade-off relation between speed and power in semiconductor devices. In particular, GaN-based metal-insulator-semiconductor heterojunction field-effect transistors (MIS-HFETs) have been investigated extensively owing to the merits of gate leakage reduction and passivation to suppress the current collapse. For both gate-insulator or passivation applications, controlling insulator-semiconductor interfaces is critical for device performances. Therefore, it is important to characterize and analyze the interface states. In fact, we observe frequency dispersion in C-V characteristics of MIS devices, attributed to electron trapping/detrapping at interface mid-gap states leading to gate-control impediment. Such mid-gap states in GaN-based devices have been characterized and analyzed by conductance method, Terman method, photo-assisted C-V method, and deep level transient spectroscopy. Although the conductance method is widely used, there are difficulties in the analysis of deep interface states with long trapping time constants in MIS devices based on wide-bandgap materials like GaN. Also, the analysis results obtained from the conductance method is affected by the assumed value of the insulator capacitance.

In this work, we proposed and developed a method using capacitance-frequency-temperature (C-f-T) mapping obtained from the temperature-dependent C-V-f characteristics for GaN-based MIS devices, based on the Lehovec equivalent circuit. From constant-capacitance contours, exhibiting a straight line behavior in the mapping, an activation energy E_{a} corresponding to an interface state energy level can be extracted for a wide range of gate biases without assuming any parameter. The gate bias dependence of the activation energies leads to many insights into the MIS devices. The effectiveness of the method is exemplified by application to AlN/AlGaN/GaN MIS devices. Through characterizing the activation energies modulated by the gate biases, we can obtain the gate-control efficiency of the MIS devices, i.e., the ratio of the bandbending change in the semiconductor to the total gate voltage change. Even though the Lehovec equivalent circuit is based on an AC small-signal model, we find that its DC limit, described by the insulator capacitance, the semiconductor capacitance, and the interface state density, gives the gate-control efficiency. Therefore, we can evaluate the interface state density from the experimentally obtained gate-control efficiency, using the values of insulator and semiconductor capacitances. From the activation energies corresponding to a wide range of gate biases, we can obtain the gate-control efficiency and the interface state density corresponding to deep interface states in comparison with the conductance method. Moreover, it is shown that the gate-control efficiency and the interface state density have

correlations with the linear-region intrinsic transconductance. In addition, we give characterization of the AlN-AlGaN interfaces by using X-ray photoelectron spectroscopy, in relation with the results of the analysis.

In summary, we have proposed and developed the C-f-T mapping method, a characterization method for wide-gap MIS devices. The method gives activation energies of electron trapping for a much extended range of gate biases, compared to the conventional conductance method. The effectiveness of the method is exemplified by applications to the AlN/AlGaN/GaN MIS devices, with evaluation of the gate-control efficiency, the interface state density, related to the intrinsic transconductance. The C-f-T mapping method provides the insights of deep interface states, being useful in the characterization of wide-gap MIS devices.

Keywords: wide-gap MIS devices, C-V characteristics, frequency dispersion, C-f-T mapping, interface states, AlGaN/GaN

Contents

Chapter 1

Introduction

1.1 Compound semiconductors and their applications

While silicon still dominates digital integration circuit applications, compound semiconductors are playing increasingly important roles in a number of cutting-edge wireless-communication and power-switching applications. For high-speed wireless-communication applications, the demand for exchange of high-quality contents is escalating through various forms of communication devices including cell phone, television, and satellite communications. The type of semiconductor material employed also depends on the speed and power requirements of each application. As shown in Fig. 1.1, cell phones in the mobile communication require a moderate frequency $\sim$ 1 GHz and a low output power $\sim$ 1 W, while a $\sim$ 100 W capability is necessary for base stations [1]. For satellite broadcasting, even higher frequency and output power are required. In the present time, Si-LDMOSFET (laterally diffused metal-oxide-semiconductor field-effect transistor) [2], GaAs-HBT (heterojunction bipolar transistor) [3], GaAs-HFET (heterojunction FET) [4], InP-HFET [5], and vacuum tube are employed for these applications according to the speed and power requirements. Realization of high-speed and high-power devices that function at frequency range from a few GHz to 100 GHz is a milestone for the future wireless communication system [6]. For power-switching applications shown in Fig. 1.2 [7], the frequency range is downscaled by 10^5 orders while the power range is upscaled by the similar orders, compared to those of the wireless-communication applications. The main role of the semiconductor devices in these applications is to handle the actual power consumed during operation. Hence the capability to handle a large power is a criterion. Depending on application, a moderate switching speed is sometimes required. Si-based materials have been employed for such device purposes. However, owing to the physical limits of Si-based materials, the energy loss during operation is a major issue. It should be noted that there is a trade-off relation between speed and power for both applications.

To understand this trade-off relation, we shall look into the physical properties of semiconductors employed for electronic devices such as field-effect transistors (FETs). First, as an indicator of the device speed, current-gain cut-off frequency f_{T} is employed, which can be expressed as

$$f_{\mathrm{T}} \simeq \frac{1}{2\pi\tau_{\mathrm{tr}}} = \frac{v}{2\pi L_{\mathrm{G}}}, \tag{1.1}$$

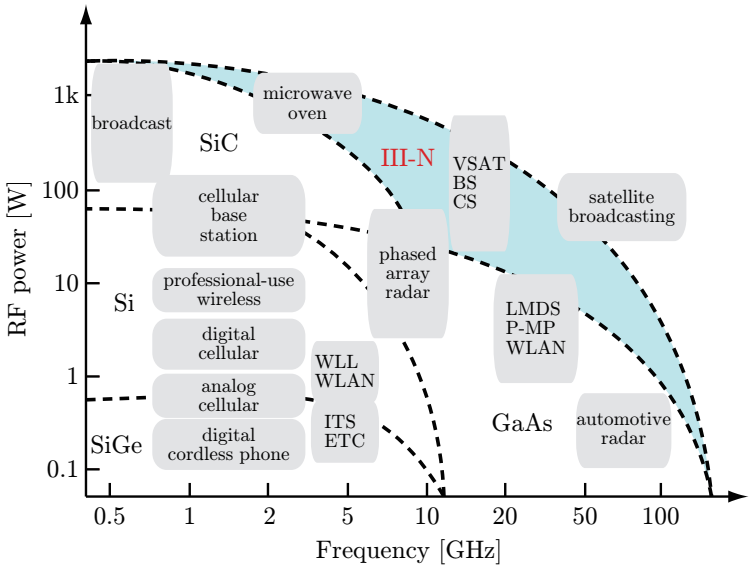

FIG. 1.1 Power and frequency in communication systems and related semiconductors [1].

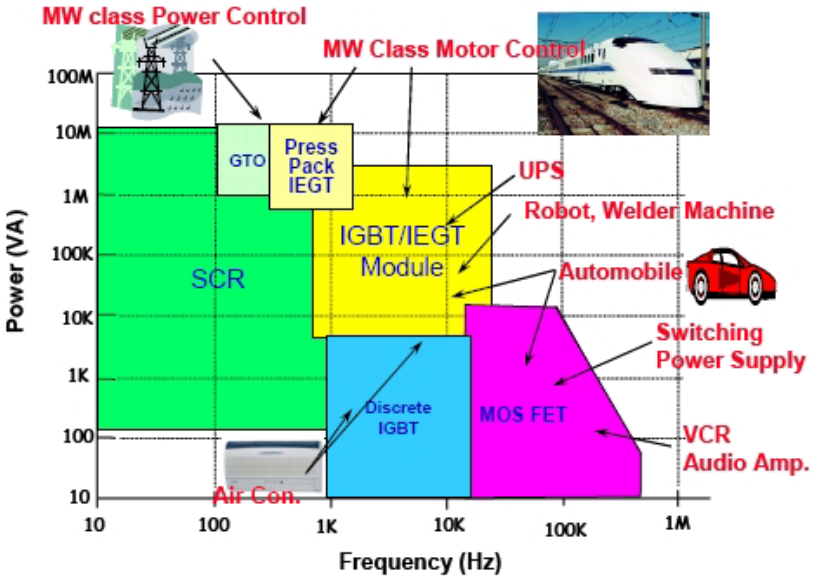

FIG. 1.2 Power and frequency in power-switching systems and related semiconductors [7].

where $\tau_{\rm tr}$ is the transition time, v is the carrier velocity, and $L_{\rm G}$ is the gate length. $f_{\rm T}$ is the cutoff frequency at which the current gain equals to 1. From Eq. 1.1, it is obvious that a high velocity and a short gate length increase $f_{\rm T}$. Up to present days, shrinkage of the gate length has led to continuous improvement of device performance. However, it is pushing the physical limit of Si systems. We have to look into the physical properties of other semiconductor materials with a high carrier velocity. Regarding the carrier velocity, mobility μ at low electric field and saturation velocity $v_{\rm sat}$ at high electric field should be taken into consideration. The mobility μ is expressed as

$$\mu = \frac{q\tau}{m^*}, \tag{1.2}$$

where q is the electron charge, m^* is the electron effective mass, and τ is the momentum

relaxation time. On the other hand, v_{sat} is given by

$$v_{\mathrm{sat}} \sim \sqrt{\frac{\hbar\omega_{\mathrm{op}}}{m^*}}, \tag{1.3}$$

where $\hbar\omega_{\mathrm{op}}$ is the optical phonon energy. This process is explained as below. By a given electric field, carriers are accelerated to gain a certain amount of energy. At a high field, when the energy of the carriers reaches $\hbar\omega_{\mathrm{op}}$, a phonon is emitted and the carrier velocity drops to zero. Repeating this process, the carrier velocity reaches the saturation velocity v_{sat} under an electric field. The common part of Eq. 1.2 and Eq. 1.3 is that they both have m^* in the denominators. Therefore, a small m^* is advantageous for the increase of μ and v_{sat}. For the power-handling aspect of FETs, increasing the source-drain voltage is effective to obtain a high power. However, owing to the shrinkage of the gate length, the electric field under the gate becomes stronger leading to the limitation of the applicable voltage range, considering the breakdown field of semiconductors. Therefore, semiconductors with high breakdown field is advantageous for high-power applications. The breakdown fields of semiconductors usually follow the relation

$$E_{\mathrm{B}} \propto E_{\mathrm{g}}^{\alpha} \quad (\alpha \simeq \text{1-3}), \tag{1.4}$$

which is a monotone increasing function of the energy bandgap E_{g} [8]. It is obvious that wide-gap semiconductor materials are advantageous for high-power applications. From the above discussion, we can conclude that small m^* and large E_{g} are advantageous for high-speed and high-power applications, respectively. However, large E_{g} materials with small lattice constants usually have large electron effective mass m_e^*, i.e.,

$$m_{\mathrm{e}}^* \propto E_{\mathrm{g}}, \tag{1.5}$$

unfavorable for the improvement of μ and v_{sat}. For these reasons, a trade-off between speed and power exists in general cases [9]; it is considered difficult to satisfy the two simultaneously. To overcome the current limitations on speed and power set by Si or GaAs, we need materials that have a higher v_{sat} and a larger E_{g}. If we take a look again at Eq. 1.3, there is an optical phonon energy term in the numerator indicating that wide-gap semiconductors possessing a large $\hbar\omega_{\mathrm{op}}$ may be available for high-speed and high-power device applications. GaN holds such physical properties giving possibilities to overcome the trade-off relation between speed and power.

1.2 GaN-based semiconductors and related devices

Most of the compound semiconductor device technologies are restricted by crystalline growth quality; lattice-mismatch with substrates leads to crystalline defects in device layers, unfavorable for the device performance. One of the major obstacles for high-quality GaN growth is the lack of a suitable lattice-matched substrate. Low temperature growth of a buffer layer possessing 16 % lattice-mismatch with sapphire substrate was realized by MOVPE(metal organic vapor phase epitaxy) [13]. The maturity of this technology has now made the crystal growth quality of GaN, AlN, InN, or their alloys, to the production level. III-group nitride semiconductors are commonly in Wurtzite crystal structure and

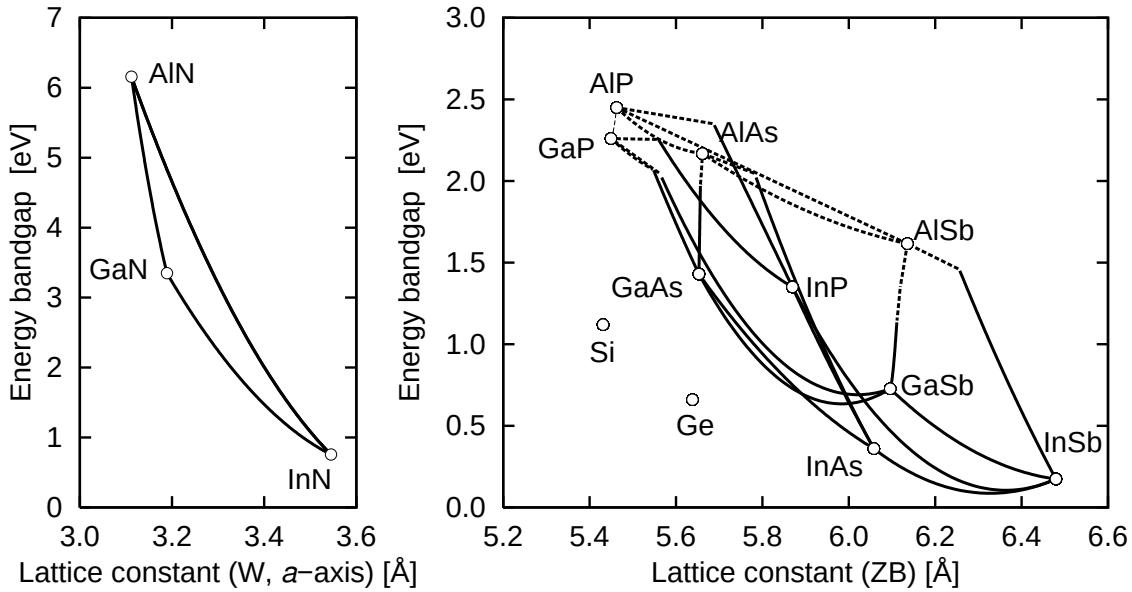

FIG. 1.3 Relation of energy gap and lattice constant in III-V compound semiconductors [10,11].

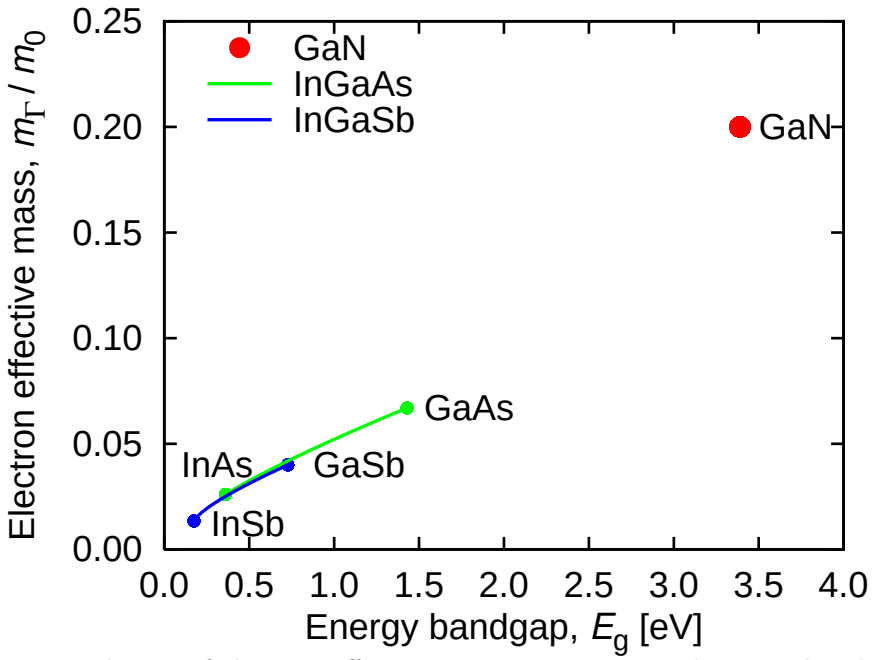

FIG. 1.4 Relation of electron effective mass at Γ point and energy band gap.

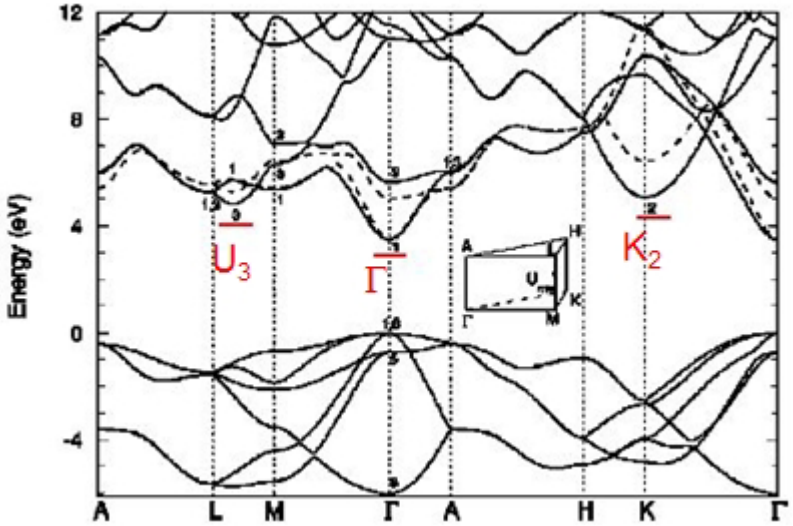

FIG. 1.5 Band structure of Wurtzite GaN [12].

are of direct bandgap materials. In principle, optical device applications are available from infra-red to ultra-violet region covered by the bandgaps of InN and AlN between 0.75 eV to 6.2 eV. In reality, green or blue light emitting diodes by InGaN are becoming more common in our daily life.

Figure 1.3 shows the relation between energy bandgap E_g and lattice constant a for III-V compound semiconductors. GaN has a small lattice constant with a large $E_g \sim 3.4$ eV leading to a very high breakdown field of 3.3×10^6 V/cm, favorable for high-power applications. However, from the relation between energy bandgap and electron effective mass shown in Fig. 1.4, it also has a large electron effective mass, unfavorable for high-speed device operation. As described earlier, high channel carrier velocity, which can be achieved by a large optical phonon energy or a small electron effective mass, is necessary for high-speed operation of FET. Despite the large electron effective mass, GaN has a small lattice constant with strong atomic bond energy that leads to a large optical phonon energy $\simeq 90$ meV. Also with a large valley-separation energy [12] shown in Fig. 1.5, GaN is anticipated to have a high saturation velocity. According to these properties, we obtain the electron transport properties of GaN by Monte Carlo simulation [14] as shown in Fig. 1.6. From the simulation result of the relation between electron drift velocity and electric field, it shows that GaN possesses $\geq 2.5 \times 10^7$ cm/s for electron peak velocity and $\geq 1.5 \times 10^7$ cm/s for electron saturation velocity, being an attractive material for electron transport. GaN possessing high saturation velocity and wide bandgap with high breakdown field, being attractive as the channel materials for high-speed and high-power electronic devices.

As a measure of suitability of a semiconductor material for high-speed and high-power transistor applications, we introduce two types of figure of merit (FoM) in the following. Based on the physical properties given in Tab. 1.1, we make comparison between some major semiconductors. In Fig. 1.7, we show the relation of f_T and the breakdown voltage

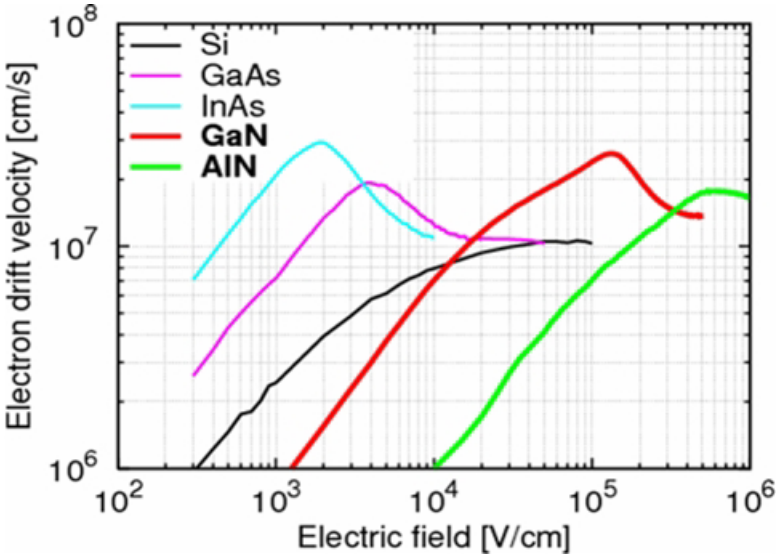

FIG. 1.6 Relation of drift velocity and electric field obtained by Monte Carlo simulation.

$V_{\rm B}$, given by

$$f_{\rm T} V_{\rm B} \leq \frac{E_{\rm B} v_{\rm sat}}{2\pi}, \tag{1.6}$$

where the square of the right side of the equation is known as Johnson's figure of merit [9] determined by the intrinsic properties of the materials. It is obvious that GaN is much superior than Si and GaAs from the aspects of $f_{\rm T}$ and $V_{\rm B}$. In Fig. 1.8, GaN-based HFET(HEMT) operated at freqency range $\geq$ 10 GHz and high-power output is expected to have wide applications such as power amplifiers for cellular base station, satellite communication, and automotive radar system [15–17].

Table 1.1 Physical properties of semiconductors [18, 19].

Mater.	Bandgap [eV]	Electron mobility [cm^2/Vs]	Electron saturation velocity [cm/s]	Breakdown field [V/cm]
Si	1.12	1500	1.0 $\times 10^7$	3.0 $\times 10^5$
GaAs	1.42	8500	2.0 $\times 10^7$	4.0 $\times 10^5$
InAs	0.36	33000	$\sim$ 4.0 $\times 10^7$	4.0 $\times 10^4$
SiC	3.33	900	2.0 $\times 10^7$	3.0 $\times 10^6$
GaN	**3.39**	**1100**	**2.7$\times 10^7$**	**3.3$\times 10^6$**

GaN-based III-V compound semiconductors also attract attentions as future power supply and switching devices. Such applications require moderate speed and higher power compared to those of wireless-communication applications. In Fig. 1.9, we show the relation of on-resistance $R_{\rm on}$ and breakdown voltage $V_{\rm B}$, given by

$$\frac{V_{\rm B}^2}{R_{\rm on}} \leq \frac{\epsilon \mu E_{\rm B}^3}{4}, \tag{1.7}$$

where $\epsilon \mu E_{\rm B}^3$ is known as Baliga's figure of merit [20] determined by the intrinsic properties

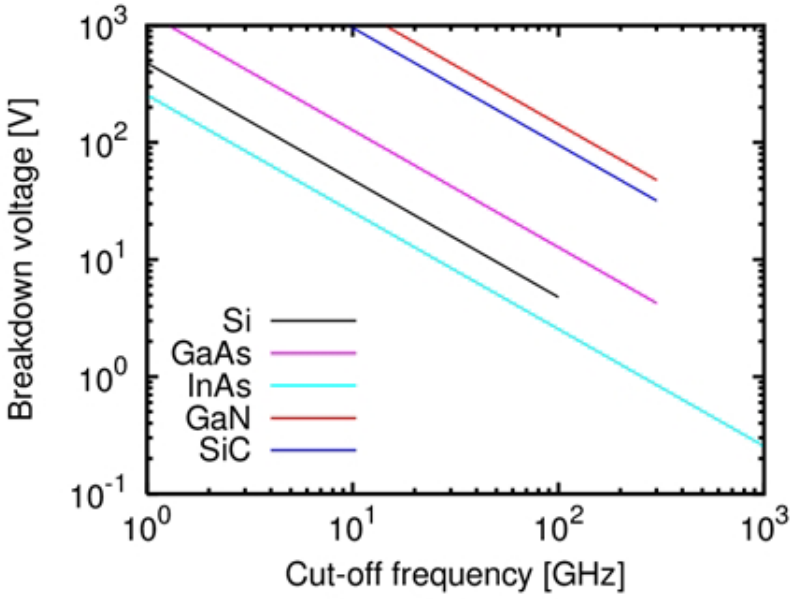

FIG. 1.7 Relation of f_T and V_B for several semiconductors.

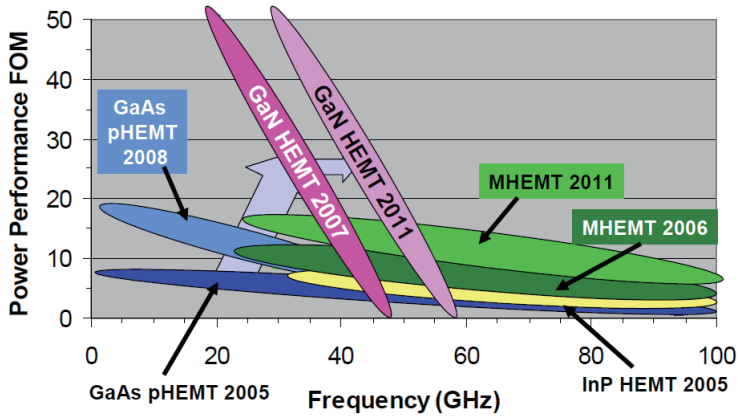

FIG. 1.8 Power performance FOM(figure of merit) and applicable frequency range of device applications. By International Technology Roadmap for Semiconductors, 2005 Edition [15].

of the materials. Here, we can also see the advantageous GaN with relatively low R_{on} at high V_B, being valuable for power electronics applications. Power electronics like Si-based vertical type MOSFETs used in power supply of server or personal computers, and Si-IGBT(insulated gate bipolar transistor) used in electric vehicle or hybrid cars, are expected to see appearance of GaN-based semiconductors [21], featuring both low on-resistance and high breakdown voltage with fast switching for substantial reduction of conduction and switching losses.

From the above discussion, GaN is expected to break through the trade-off relation in realization of high-speed and high-power electronic devices. Furthermore, it is possible for GaN to form heterojunction with heterogeneous material AlGaN for high-speed

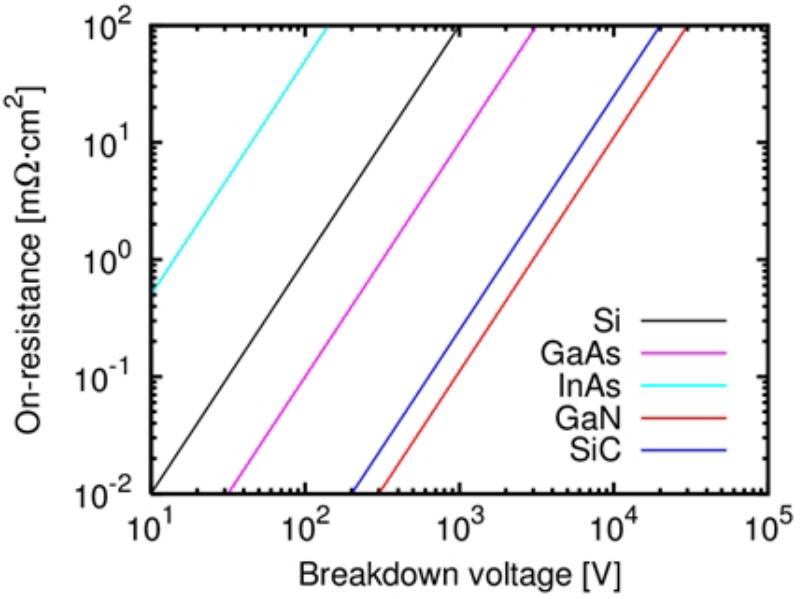

FIG. 1.9 Relation of R_{on} and V_B for several semiconductors.

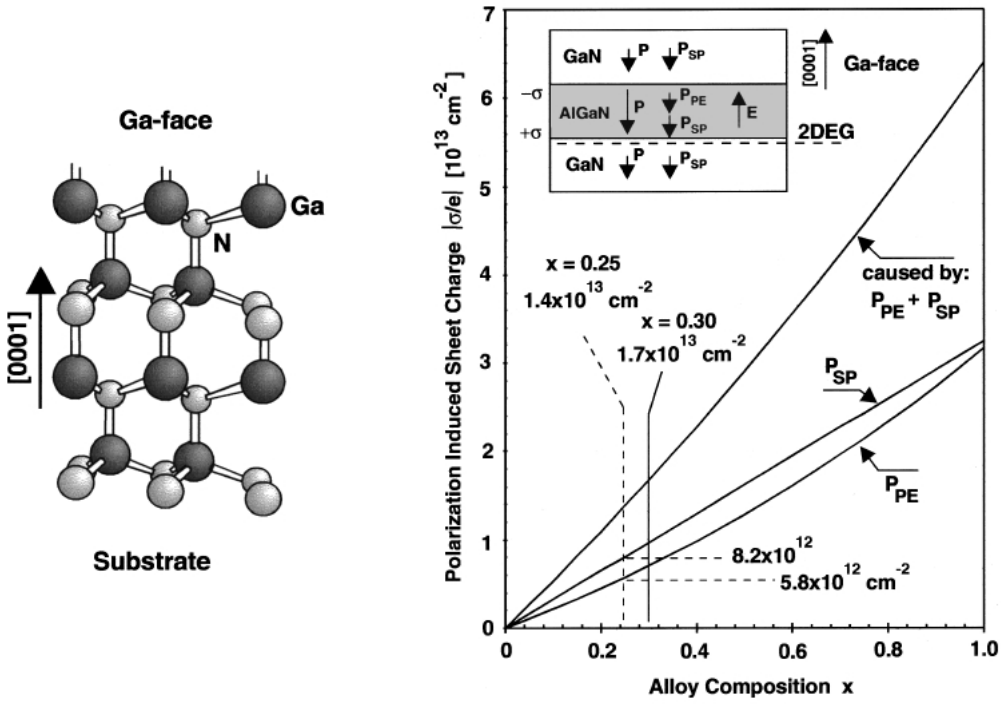

FIG. 1.10 Left: schematic drawing of the crystal structure of Wurtzite Ga-face GaN. Right: calculated sheet charge density caused by spontaneous and piezoelectric polarization of a GaN-face GaN/AlGaN/GaN heterostructure. [22]

operation. AlGaN is grown pseudomorphically with a tensile strain to match the lateral lattice constant of Ga-face GaN. The Ga polarity is used to form a two-dimensional elec-

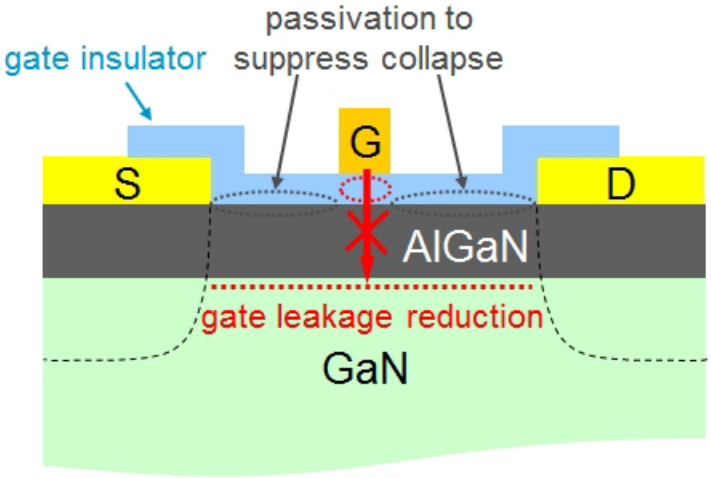

FIG. 1.11 Illustration of gate leakage reduction and passivation in AlGaN/GaN MIS-HFETs.

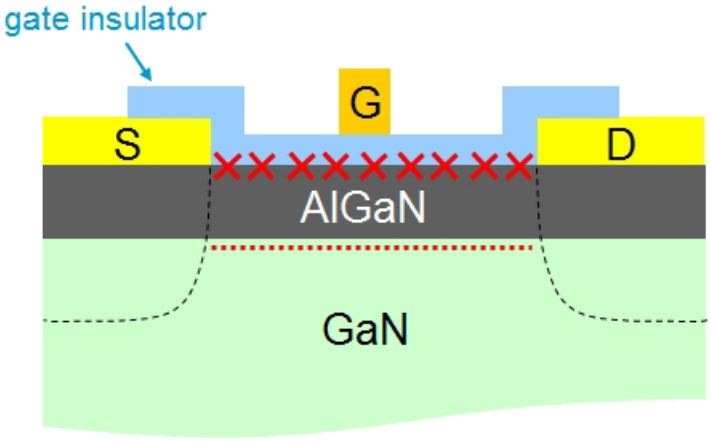

FIG. 1.12 Illustration of gate leakage current and interface states in AlGaN/GaN MIS-HFETs.

tron gas (2DEG) with high sheet carrier concentration by spontaneous and piezoelectric polarization at the AlGaN/GaN heterointerface as shown in Fig. 1.10 [22]. The concentration of 2DEG depends on the composition of III group materials and film thickness of AlGaN. Typically, Al composition of 20-30 % gives a 2DEG concentration $\simeq 10^{13}$ cm^{-2}. AlGaN/GaN heterojunction field-effect transistors [23] have been extensively developed as promising devices for high-speed and high-power applications. However, from the early stage of the development, AlGaN/GaN Schottky gate HFETs have been suffering from severe gate leakage current and current collapse. In order to solve these problems, AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors (MIS-HFETs) illustrated in Fig. 1.11, enabling effective reduction of the gate leakage current and current collapse, have been developed and studied. As a gate-insulator of the MIS devices, high-dielectric-constant (high-k) oxide materials, such as Al_2O_3 [24], HfO_2 [25,26], and also high-k nitride materials, such as AlN [27–31], BN [32,33], have been investigated. Owing to their high thermal conductivities, the nitride materials are favorable also for passivation of GaN-based devices, exhibiting good heat release properties [27,34–38]. Since controlling insulator-semiconductor interfaces is critical for both gate-insulator or passi-

vation applications, it is important to characterize and analyze the interface states. In fact, we observe frequency dispersion in C-V characteristics of MIS devices, attributed to electron trapping/detrapping at interface mid-gap states illustrated in Fig. 1.12, leading to gate-control impediment. Such mid-gap states in GaN-based devices have been characterized and analyzed by conductance method [28, 29, 39–44], Terman method [45, 46], photo-assisted C-V method [47, 48], and deep level transient spectroscopy [49–52]. Although the conductance method is widely used, there are difficulties in the analysis of deep interface states with long trapping time constants [53] in MIS devices based on wide-bandgap materials like GaN [29,30,54]. Also, the analysis results obtained from the conductance method is affected by the assumed value of the insulator capacitance.

In this work, we proposed and developed a method using capacitance-frequency-temperature (C-f-T) mapping [30, 55] obtained from the temperature-dependent C-V-f characteristics for GaN-based MIS devices, based on the Lehovec equivalent circuit [56]. From constant-capacitance contours, exhibiting a straight line behavior in the mapping, an activation energy E_{a} corresponding to an interface state energy level can be extracted for a wide range of gate biases without assuming any parameter. The gate bias dependence of the activation energies leads to many insights into the MIS devices. The effectiveness of the method is exemplified by application to AlN/AlGaN/GaN MIS devices. Through characterizing the activation energies modulated by the gate biases, we can obtain the gate-control efficiency of the MIS devices, i.e., the ratio of the bandbending change in the semiconductor to the total gate voltage change. Even though the Lehovec equivalent circuit is based on an AC small-signal model, we find that its DC limit, described by the insulator capacitance, the semiconductor capacitance, and the interface state density, gives the gate-control efficiency. Therefore, we can evaluate the interface state density from the experimentally obtained gate-control efficiency, using the values of insulator and semiconductor capacitances. From the activation energies corresponding to a wide range of gate biases, we can obtain the gate-control efficiency and the interface state density corresponding to deep interface states in comparison with the conductance method. Moreover, it is shown that the gate-control efficiency and the interface state density have correlations with the linear-region intrinsic transconductance. In addition, we give characterization of the AlN-AlGaN interfaces by using X-ray photoelectron spectroscopy, in relation with the results of the analysis.

1.3 Purpose of this study

We proposed and developed an analysis method for GaN-based MIS devices by using C-f-T mapping to evaluate the gate-control efficiency and the interface state density, both exhibiting correlations with the linear-region intrinsic transconductance. The effectiveness of the method is exemplified by application to AlN/AlGaN/GaN MIS devices to elucidate the properties of AlN-AlGaN interfaces depending on their formation processes. Using the C-f-T mapping, we extract the gate-bias-dependent activation energy with its derivative giving the gate-control efficiency, from which we evaluate the AlN-AlGaN interface state density through the Lehovec equivalent circuit in the DC limit. It is shown that the gate-

control efficiency and the interface state density have correlations with the linear-region intrinsic transconductance, all depending on the interface formation processes. The C-f-T method gives activation energies of electron trapping for a much extended range of gate biases, compared to the conventional conductance method. The method provides the insights of deep interface states, being useful in the characterization of wide-gap MIS devices.

1.4 Organization of the dissertation

- Chapter 1:
  Introduction of this research including the general background on compound semiconductors, the GaN-based semiconductors and related devices, and the purpose of this work are given.
- Chapter 2:
  Explanation of the principle of characterization method using C-f-T mapping
- Chapter 3:
  Application of C-f-T mapping method to AlN/AlGaN/GaN MIS devices is discussed. Firstly, we show the fabrication of the MIS devices including the in-depth characterization of the AlN thin films followed by the DC characterization. We then make comparison between the analysis results of that by the conductance method and the C-f-T mapping method. Furthermore, we discuss the gate-control efficiency and the interface state density characterized by the C-f-T mapping method. The effectiveness of the method is then demonstrated through the analysis of AlN/AlGaN/GaN MIS devices with different treatments for the AlN/AlGaN interfaces. The relations between the gate-control efficiency, the interface state density, and the intrinsic transconductance of the MIS devices are also discussed. Lastly, X-ray photoelectron spectroscopy analysis of AlN/AlGaN interfaces are investigated to explain the analysis results.
- Chapter 4:
  Conclusion and future perspective of this research are given.

Chapter 2

Principle of characterization method using capacitance-frequency-temperature (C-f-T) mapping

2.1 Conventional conductance method

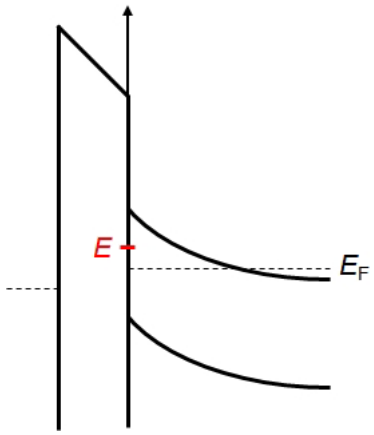

FIG. 2.1 An interface state energy level in the band diagram of a MIS structure.

For the insulator-semiconductor interface of a MIS device, the electron occupation probability P at an interface state shown in Fig. 2.1 is given by a time-dependent rate equation

$$\frac{\partial P}{\partial t} = \gamma(1-P)n - \alpha P, \tag{2.1}$$

where n is the semiconductor electron density at the interface, and γ, α are proportional constants. If we use the P, n, and surface potential V each separated into its DC and AC components given by

$$P = P_0 + \widetilde{P}\exp(j\omega t) \tag{2.2}$$

$$n = n_0 + \widetilde{n}\exp(j\omega t) \tag{2.3}$$

$$V = V_0 + \widetilde{V}\exp(j\omega t), \tag{2.4}$$

we can obtain

$$\widetilde{P} \simeq \frac{P_0(1-P_0)}{1+j\omega\tau P_0}\frac{\widetilde{n}}{n_0} = \frac{P_0(1-P_0)}{1+j\omega\tau P_0}\frac{q\widetilde{V}}{k_{\rm B}T}, \tag{2.5}$$

where P_0 is the Fermi-Dirac distribution using the Fermi level $E_{\rm F}$, and

$$\tau = \frac{1}{\gamma n_0} \tag{2.6}$$

is the time constant. Using the interface state density $D_{\rm i}(E)$, a function of energy E, the total small signal AC admittance owing to the interface states is expressed as

$$\begin{aligned} Y_{\rm i} &= G_{\rm i} + jC_{\rm i}\omega & (2.7)\\ &= \frac{j\omega q}{\widetilde{V}}\int D_{\rm i}(E)\widetilde{P}{\rm d}E & (2.8)\\ &= \frac{j\omega q^2}{k_{\rm B}T}\int \frac{D_{\rm i}(E)P_0(1-P_0)}{1+j\omega\tau P_0}{\rm d}E & (2.9)\\ &= j\omega q^2\int \frac{D_{\rm i}(E)}{1+j\omega\tau P_0}\left(-\frac{{\rm d}P_0}{{\rm d}E}\right){\rm d}E. & (2.10)\end{aligned}$$

For the low temperature limit, since $-{\rm d}P_0/{\rm d}E \simeq \delta(E-E_{\rm F})$, using $D_{\rm i}(E=E_{\rm F})$ and $P_0 = 1/2$, the admittance becomes

$$G_{\rm i} + jC_{\rm i}\omega \simeq \frac{j\omega q^2 D_{\rm i}(E_{\rm F})}{1+j\omega\tau/2}, \tag{2.11}$$

where

$$\frac{G_{\rm i}}{\omega} = \frac{\omega\tau q^2 D_{\rm i}}{2(1+\omega^2\tau^2/4)} \tag{2.12}$$

and

$$C_{\rm i} = \frac{q^2 D_{\rm i}}{1+\omega^2\tau^2/4}. \tag{2.13}$$

For a discrete interface state where

$$D_{\rm i}(E) = D_0\ \delta(E-E_0) \tag{2.14}$$

(note that the units of $D_{\rm i}(E)$ and D_0 are different), the admittance is expressed as

$$G_{\rm i} + jC_{\rm i}\omega = \frac{j\omega q^2 D_0}{1+j\omega\tau P_0(E_0)}\frac{\exp[(E_0-E_{\rm F})/k_{\rm B}T]}{k_{\rm B}T(1+\exp[(E_0-E_{\rm F})/k_{\rm B}T])^2}. \tag{2.15}$$

For the case $E_{\rm F} = E_0$, the admittance becomes

$$G_{\rm i} + jC_{\rm i}\omega = \frac{j\omega q^2 D_0}{4k_{\rm B}T(1+j\omega\tau/2)} \quad (E_{\rm F}=E_0), \tag{2.16}$$

where

$$\frac{G_{\rm i}}{\omega} = \frac{\omega\tau q^2 D_0}{8k_{\rm B}T(1+\omega^2\tau^2/4)} \tag{2.17}$$

and

$$C_{\rm i} = \frac{q^2 D_0}{4k_{\rm B}T(1+\omega^2\tau^2/4)}, \tag{2.18}$$

exhibits the same frequency dependence as that in Eqs. 2.11-2.13.

For general continuous interface states, since $P_0(1-P_0)$ only holds values near the Fermi level $E_{\rm F}$, using $D_{\rm i}(E=E_F)$, Eq. 2.10 can be approximated as

$$G_{\rm i}+jC_{\rm i}\omega \;\simeq\; j\omega q^2 D_{\rm i}\int \frac{1}{1+j\omega\tau P_0}\left(-\frac{{\rm d}P_0}{{\rm d}E}\right){\rm d}E. \tag{2.19}$$

Taking the integration of P_0 from 0 to 1, we can obtain [56]

$$\frac{G_{\rm i}}{\omega}=\frac{q^2 D_{\rm i}{\rm ln}(1+\omega^2\tau^2)}{2\omega\tau} \tag{2.20}$$

and

$$C_{\rm i}=\frac{q^2 D_{\rm i}{\rm atan}(\omega\tau)}{\omega\tau}, \tag{2.21}$$

being the basis of the conductance method.

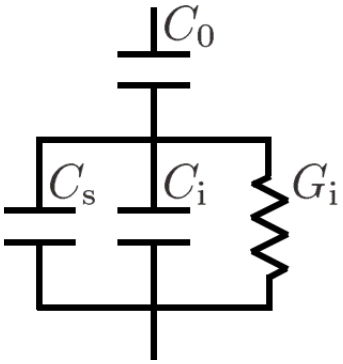

FIG. 2.2 The equivalent circuit of the MIS structure.

Based on the equivalent circuit of the MIS structures depicted in Fig. 2.2, with the insulator capacitance C_0, the semiconductor capacitance $C_{\rm s}$, the interface state capacitance $C_{\rm i}$, and the interface state conductance $G_{\rm i}$, $G_{\rm i}/\omega$ as a function of frequency exhibits a single-peaked behavior, with the peak frequency $\sim 1/\pi\tau$ and the peak value $\sim 0.4q^2D_{\rm i}$, as illustrated in Fig. 2.3. Therefore, we can obtain time constant τ from the peak frequency. From Eq. 2.6,

$$\tau=\frac{1}{\gamma n_0}=\frac{1}{\gamma N_{\rm C}}{\rm exp}[\beta(E_{\rm C}-E_{\rm F})]=\tau_0{\rm exp}(\beta E_{\rm a}), \tag{2.22}$$

where $n_0=N_{\rm C}{\rm exp}[-\beta(E_{\rm C}-E_{\rm F})]$ and $\tau_0=1/(\gamma N_{\rm C})$, activation energy $E_{\rm a}$ can be extracted from the Arrhenius plot of the temperature dependence of τ. However, accurate value of the insulator capacitance C_0 is required for this analysis, which may require extra experiments to determine the C_0 value. Furthermore, owing to the much longer time constants corresponding to the deeper energy levels in wide-bandgap devices, it is sometimes difficult to obtain peaks in the measured frequency and temperature range. Assuming $C_0=600$ nF/cm^2, $C_{\rm s}=300$ nF/cm^2, $D_{\rm i}=10^{14}$ cm^{-2}eV^{-1}, $\tau_0=1$ ns, and $E_{\rm a}=0.5$ eV, we obtain the calculation results shown in Fig. 2.4 based on the conductance method. We have a problem that the peaks are obtained only for a narrow range of gate biases, prohibiting analysis of deeper interface states.

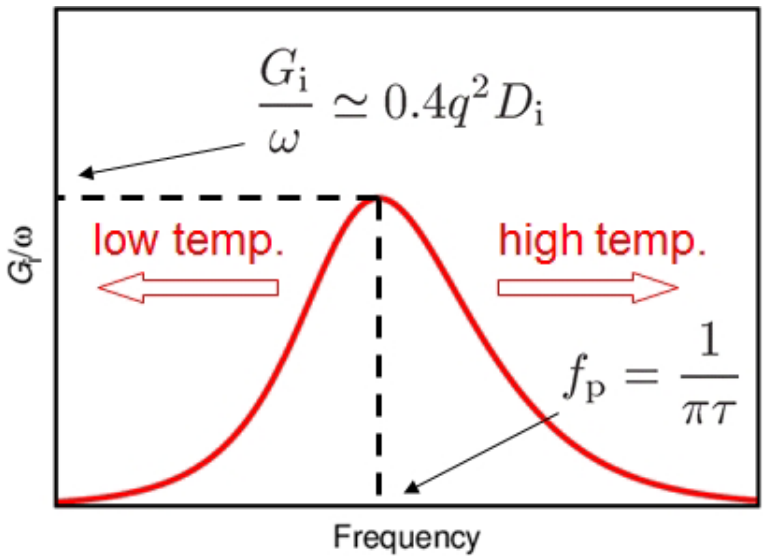

FIG. 2.3 Illustration of a single-peaked behavior of G_i/ω as a function of frequency.

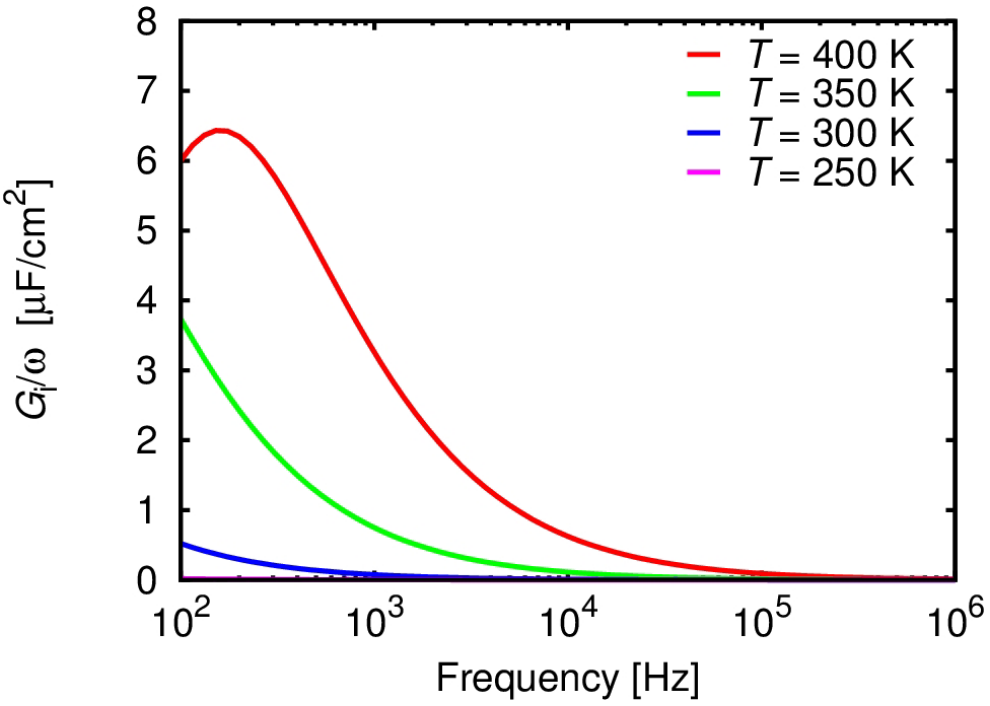

FIG. 2.4 Calculation results based on conductance method.

2.2 A novel frequency domain characterization method —— C-f-T mapping method

In order to solve the problem, we proposed an analysis method using C-f-T mapping obtained from the temperature-dependent C-V-f characteristics. In Fig. 2.5, we show a C-f-T mapping with a contour, which is obtained by the numerical calculation with the same assumption as that for the conductance method. The contour exhibits a straight line behavior, which can be explained by the equivalent circuit of the MIS structures with a total admittance

$$Y = \frac{1}{Z} = \left(\frac{1}{jC_0\omega} + \frac{1}{G_\mathrm{i} + jC_\mathrm{s}\omega + jC_\mathrm{i}\omega} \right)^{-1}. \tag{2.23}$$

Since C_i given by Eq. (2.21) and G_i/ω by Eq. (2.20) are functions of only $\omega\tau$, the measured capacitance $C = \mathrm{Im}Y/\omega$ is a function of only $\omega\tau$. Therefore, a contour in C-f-T mapping, i.e., C = constant leading to $\omega\tau = 2\pi f\tau$ = constant, exhibits a straight line behavior as expressed by $f \propto 1/\tau \propto \exp(-\beta E_\mathrm{a})$, from which the activation energy E_a corresponding to the interface state energy level can be extracted. Due to slow $\omega\tau$ dependence of Eqs. (2.21) and (2.20), even though the frequency is far from the peak position $\sim 1/\pi\tau$, change in the C-f-T mapping is detectable. Figure 2.5 shows the calculation results of the C-f-T mapping using the above parameters. The white line corresponds to the peaks in the conductance method; we can confirm that it is difficult to observe peaks in this frequency and temperature range. On the other hand, it is easy to find contours in the mapping, e.g., the black line, exhibiting a straight line behavior and giving the activation energy. The C-f-T mapping method gives E_a for a much extended range of the gate biases, providing many insights into the MIS devices.

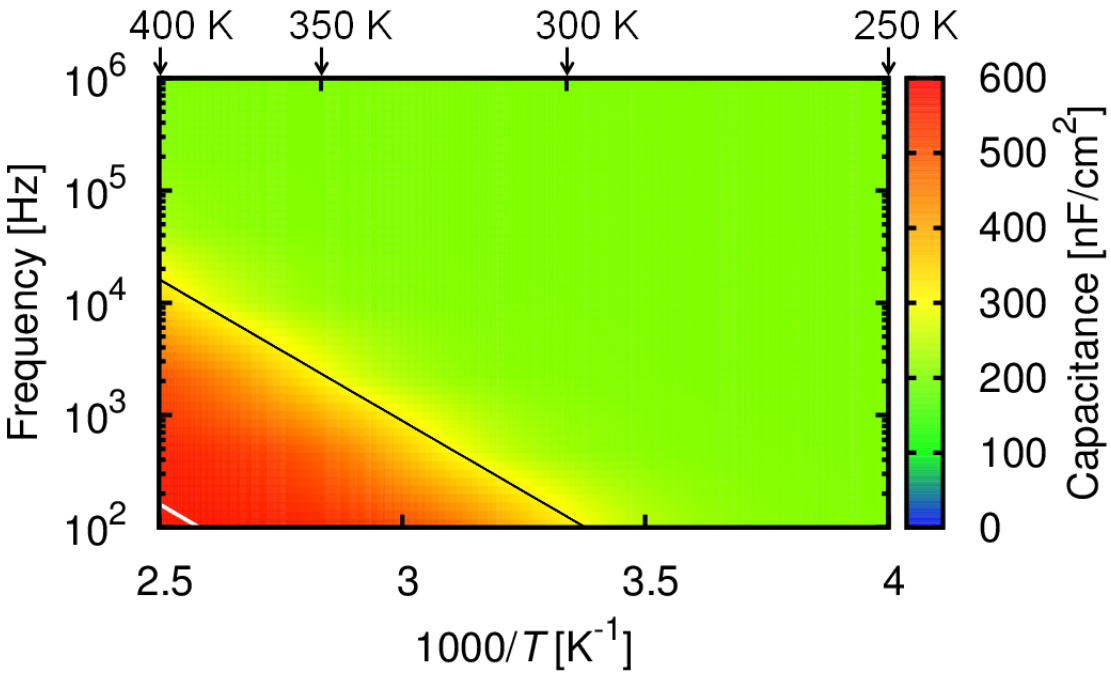

FIG. 2.5 Calculation results based on C-f-T mapping method.

Chapter 3

Application of C-f-T mapping method to AlN/AlGaN/GaN MIS devices

3.1 Device fabrication

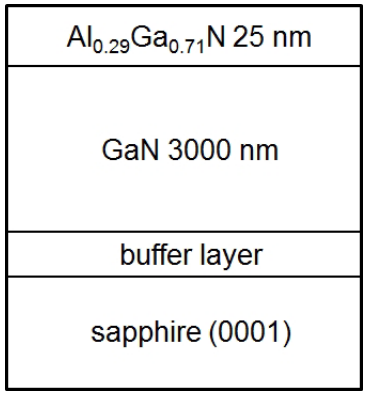

FIG. 3.1 An AlGaN/GaN heterostructure.

Device fabrication was carried out using an $Al_{0.29}Ga_{0.71}N$(25 nm)/GaN(3000 nm) heterostructure shown in Fig. 3.1, obtained by metal-organic vapor phase epitaxy on sapphire(0001). Hall measurements of the heterostructure show an as-grown electron mobility $\mu \simeq 1400$ cm^2/V-s and a sheet electron concentration $n_s \simeq 1.0 \times 10^{13}$ cm^{-2}. The following device processes were performed in order

1. marker formation
2. Ohmic electrode formation
3. device isolation
4. gate insulator deposition
5. gate electrode formation

Figure 3.2 illustrates the process flow of MIS device fabrication.

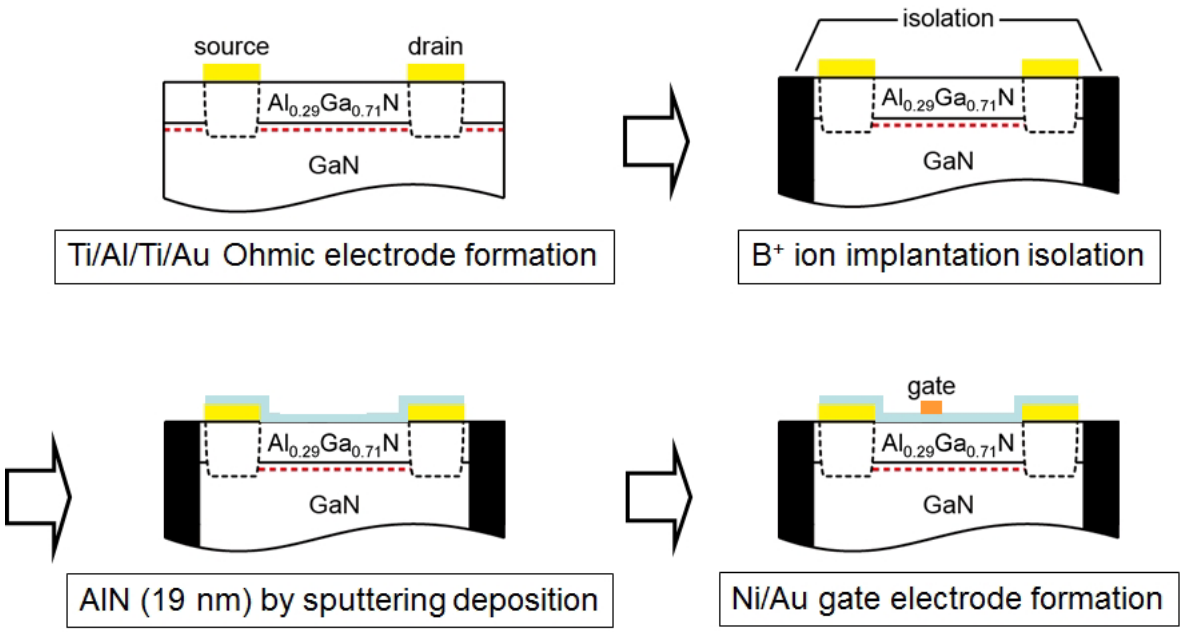

FIG. 3.2 Process flow of MIS device fabrication.

Marker formation

The purpose of marker formation is to provide a reference when aligning the gate electrode relative to the source and drain electrodes. The process flow is shown in Tab. 3.3.

Table 3.1 Process of marker formation

Processes	Conditions
surface treatment	acetone, methanol, DIW 3 min each
	O_2 plasma ashing 50 Pa 10 W 4 min
	Semico-clean 5 min, DIW 3 min
	baking 110 ℃ 3 min
resist coating	LOL2000(3000 rpm 60 s), bake(180 ℃ 180 s)
	TSMR-8900(4000 rpm 60 s), bake(110 ℃ 90 s)
patterning	exposure $\sim$ 12 mW/cm^2(405 nm) 6.2 s
	development NMD-W(60 s), DIW (180 s)
surface treatment	O_2 plasma ashing 50 Pa 10 W 10 s
	Semico-clean 5 min, DIW 3 min
deposition	Ti/Au=10/150 nm
lift-off	1165(60 ℃)
	acetone, methanol, DIW 3 min each

We employed a double layer structure, a lift-off layer LOL2000 (Rohm & Haas) and a positive resist TSMR-8900 (TOKYO OHKA KOGYO), for patterning. Also, Au was selected owing to its stability with temperature and easy emission of secondary electron during SEM observation in electron beam lithography process. The Ti is serving as a glue between AlGaN and Au layer to enhance their adhesion. An example of the completed marker is shown in Fig. 3.3.

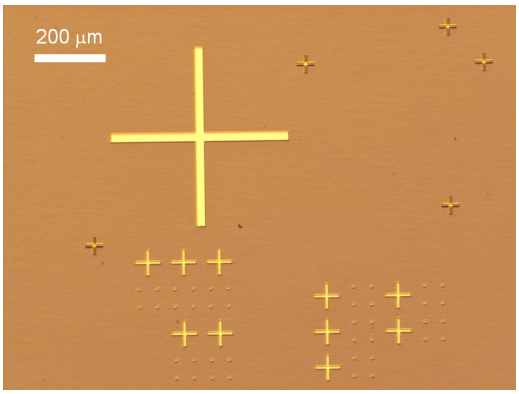

FIG. 3.3 Ti/Au marker.

Ohmic electrode formation

The purpose of forming Ohmic contacts is to provide an Ohmic-like access between the metal contacts (source and drain contacts) and the AlGaN/GaN 2DEG channel. In order to obtain such electrical property, proper metal selection and high-temperature annealing are important. Utilizing the gettering effect of Ti/Al layer, N-vacancy is induced in AlGaN/GaN layer during annealing, which is known to behave like donors [57, 58]. As a result, n-AlGaN and n-GaN form Ohmic contacts between the metal contacts (source and drain contacts) and the AlGaN/GaN 2DEG channel. The following Ti/Au metals are to cover the reactive Al surface from oxidation and etching during wet processes. Ti functions as a glue for Al and Au to enhance their adhesion.

The Ohmic contact is evaluated by transmission line model (TLM) measurement. Figure 3.4 shows an example of the TLM measurement result. The total resistance R_{tot} can be expressed as

$$R_{\mathrm{tot}} \simeq 2R_{\mathrm{c}} + R_{\square}, \tag{3.1}$$

where R_c is the contact resistance, and $R_{\square} = \rho_{\square} L$ is the sheet resistance given by the sheet resistivity $\rho_{\square}$ and the electrode spacing L. From the intercept and gradient of R_{tot}-L relation, we can evaluate R_{c} and $\rho_{\square}$, respectively.

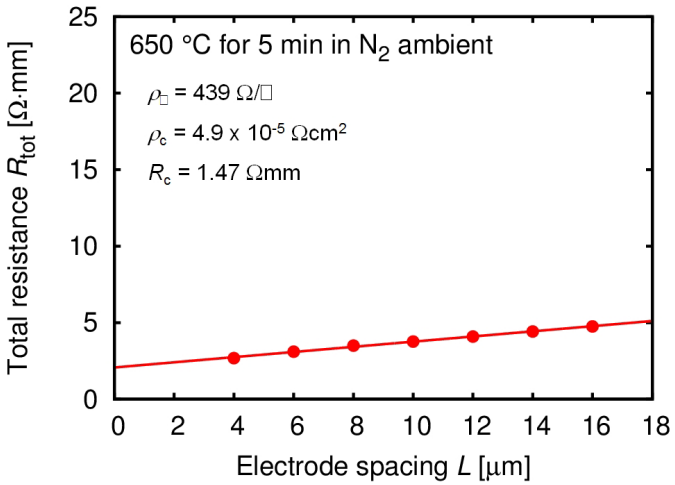

FIG. 3.4 An example of TLM measurement results.

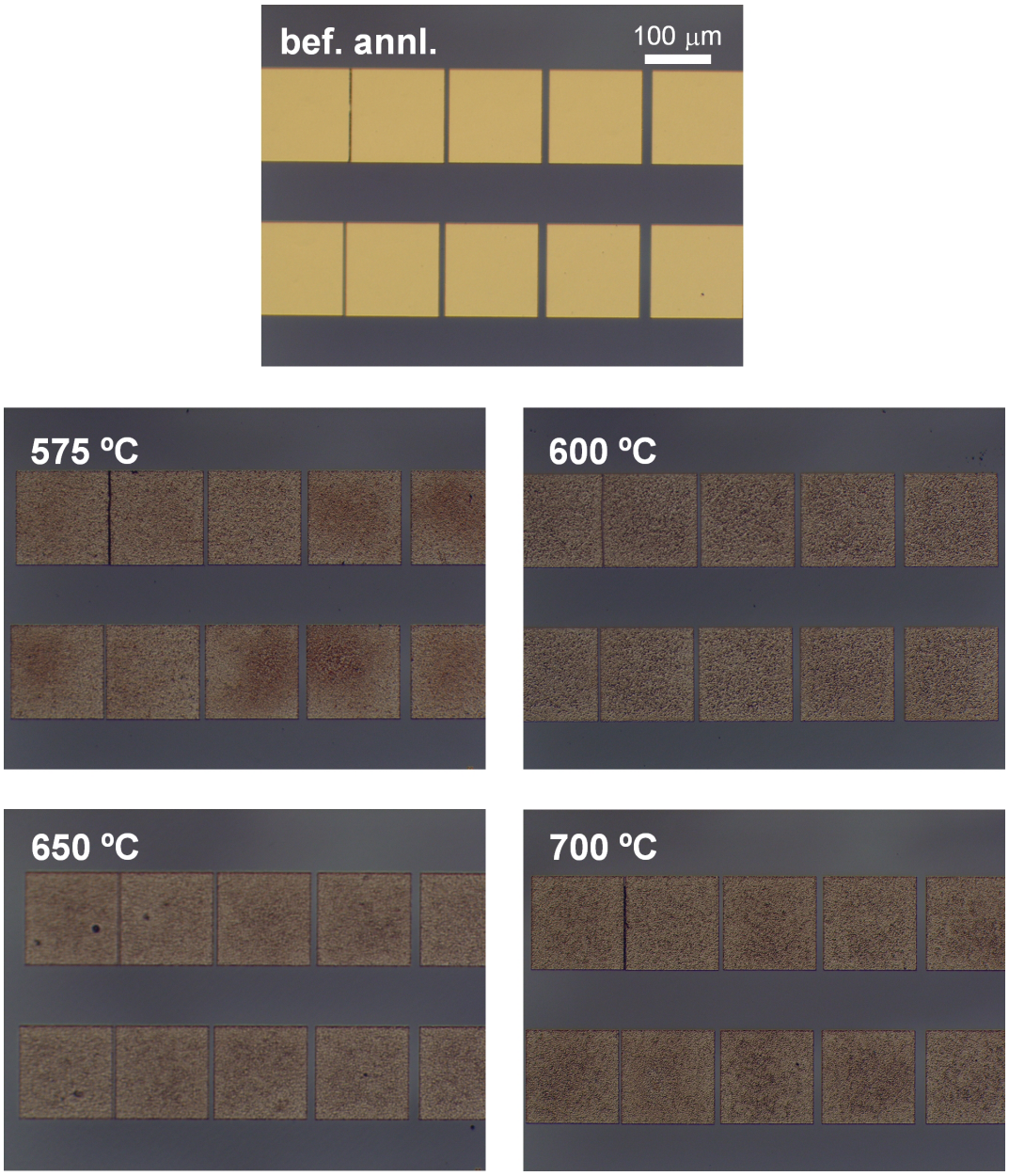

FIG. 3.5 Morphology of Ti/Al/Ti/Au after annealing at various temperatures for 5 minutes in N_2 ambient.

The experiment for temperature-dependence of R_c was carried out to find the optimum annealing temperature giving the lowest R_c. Figure 3.2 shows the morphology of Ti/Al/Ti/Au after annealing at various temperatures for 5 minutes in N_2 ambient. We can observe surface roughening due to the high temperature annealing as shown by the dull metal surfaces caused by irregular reflection.

The result of temperature dependence of R_c is shown in Fig. 3.6, in which 650 ℃shows the lowest R_c. This temperature is employed for Ohmic electrode formation as shown in the process flow described in Tab. 3.2.

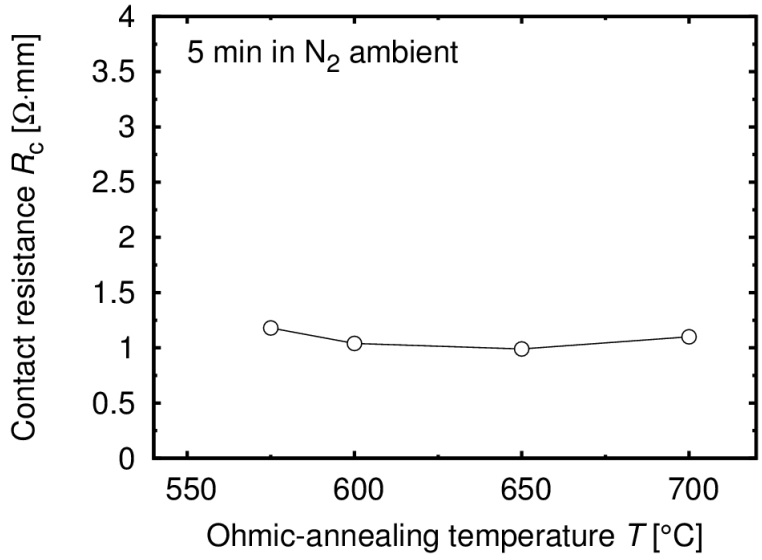

FIG. 3.6 Temperature dependence of contact resistance R_c.

Table 3.2 Process of Ohmic electrode formation

Processes	Conditions
surface treatment	acetone, methanol, DIW 3 min each
	O_2 plasma ashing 50 Pa 10 W 4 min
	Semico-clean 5 min, DIW 3 min
	baking 110 ℃ 3 min
resist coating	LOL2000(3000 rpm 60 s), bake(180 ℃ 180 s)
	TSMR-8900(4000 rpm 60 s), bake(110 ℃ 90 s)
patterning	exposure $\sim$ 12 mW/cm^2(405 nm) 6.2 s
	development NMD-W(60 s), DIW (180 s)
surface treatment	O_2 plasma ashing 50 Pa 10 W 10 s
	Semico-clean 5 min, DIW 3 min
deposition	Ti/Al/Ti/Au=10/200/100/50 nm
lift-off	1165(60 ℃)
	acetone, methanol, DIW 3 min each
annealing	N_2 atmosphere 650 ℃ 5 min

Device isolation

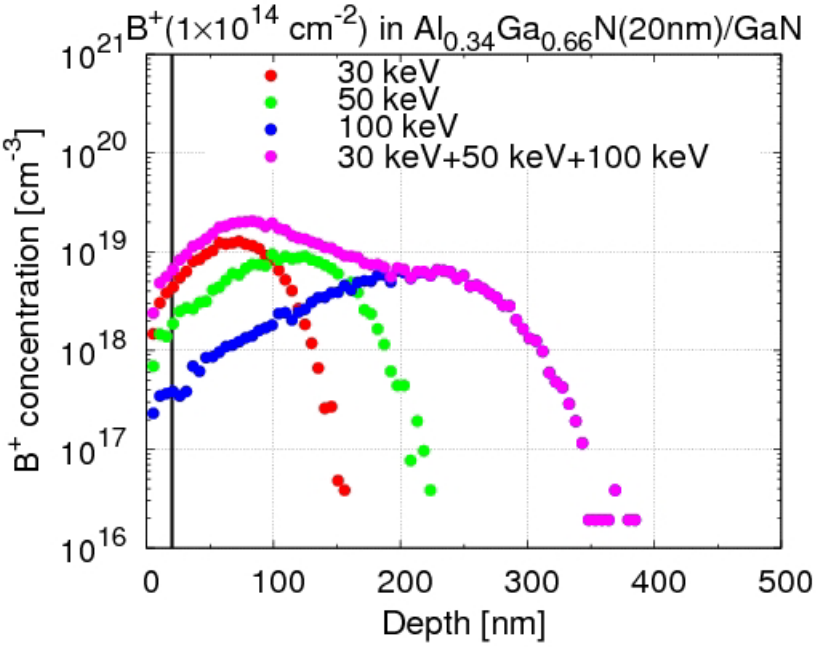

FIG. 3.7 B^+ concentration as a function of depth and acceleration voltage [59].

Implant isolation is a common method used in semiconductor device fabrication processes for inter-device isolation [60]. The generally applied ion implantation method causes damages in the semiconductor crystal, resulting the enhancement of electrical resistance in the defined area between the devices. It was reported that the implanted ion creates energy levels in or near mid-gap [61].

In our experiment, we employed LOL2000 and S1830 (Rohm & Haas) double layer for the ease of resist removal as the S1830 becomes impervious to resist remover 1165 (Shipley) after ion implantation. The patterning using the thick S1830 resist not only protects the device area but also defines the gate width. B^+ ion from BF_3 gas was induced and implanted into the sample by acceleration voltages of 30 keV, 50 keV, and 100 keV. The three-step implantation ensures uniform distribution of ions upto a certain depth in GaN from the AlGaN surface. Figure 3.7 obtained by SRIM/TRIM [59] simulator shows the B^+ concentration distribution as functions of depth and acceleration voltage. It is shown that $\sim$ 300 nm from the AlGaN surface can be ion-implanted. The substitutional or interstitial B^+ ion can cause Al, Ga, N vacancies which create deep levels that trap the carriers as illustrated in Fig. 3.8. As a result, the implanted area has high electrical resistance. Such deep levels can absorb and emit visible light with corresponding energy, causing the slightly yellowish look of the wafer after the ion implantation. The ion applied for implantation is not limited to B^+ only but also O^+ and Fe^+ are possible options [62,63]

Figure 3.9 shows the TLM results before and after the ion implantation. The latter shows the true sheet resistivity because the sheet resistance is correctly normalized by

the defined gate width after the ion implantation. Device isolation process is described in Tab. 3.3.

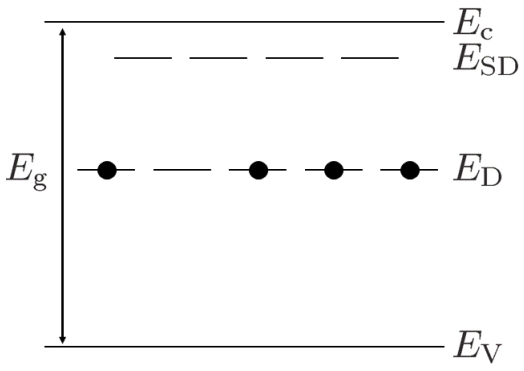

FIG. 3.8 Deep levels created by ion implantation.

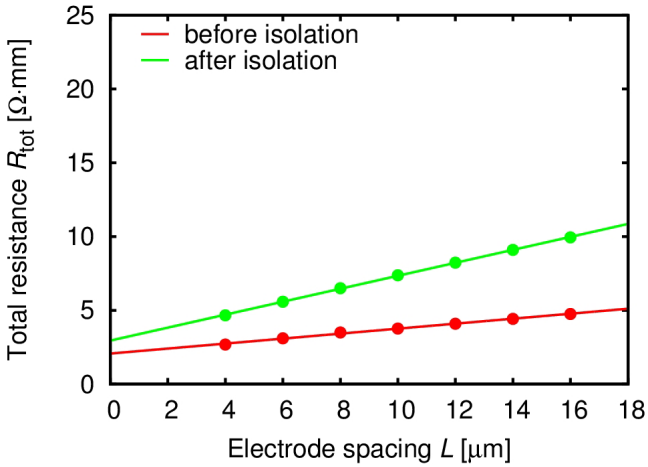

FIG. 3.9 TLM results before and after the isolation.

Table 3.3 Process of device isolation

Processes	Conditions
surface treatment	acetone, methanol, DIW 3 min each
	O_2 plasma ashing 50 Pa 10 W 4 min
resist coating	LOL2000(3000 rpm 60 s), bake(180 ℃ 180 s)
	S1830(4000 rpm 60 s), bake(110 ℃ 90 s)
patterning	exposure $\sim$ 12 mW/cm^2(405 nm) 30 s
	development NMD-W(50 s), DIW(180 s)
	bake 140 ℃ 5 min
ion implantation	B^+ 30 keV(1×10^{14} cm^{-2}) + 50 keV(1×10^{14} cm^{-2})
	+100 keV(1×10^{14} cm^{-2})
resist removal	1165(60 ℃) + O_2 plasma ashing 50 Pa 30 W 10 min

Gate insulator deposition

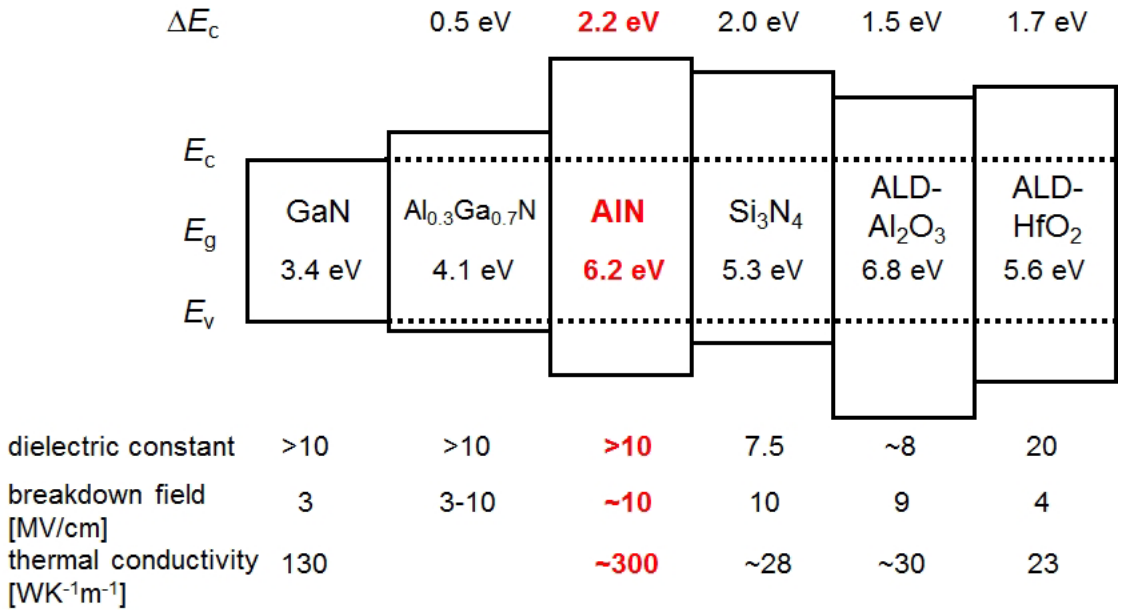

FIG. 3.10 Band lineup of GaN, AlGaN, and various insulators, including basic physical parameters. [64–67]

The gate insulator selection is critical for the device performance of MIS transistors. The band lineup of GaN, AlGaN, and various insulators is shown in Fig. 3.10 [64–67]. In particular, high-dielectric-constant (high-k) oxide materials, such as Al_2O_3 [24] or HfO_2 [25, 26], have been investigated as a gate dielectric insulator of the MIS transistors. However, for such oxide insulators, there are difficulties in controlling the interface between the oxide and the nitride [68]. On the other hand, AlN is an important non-oxide high-k insulator, with a possible suitability for III-V device processing [69]. Previously, sputtering deposition of AlN on AlGaN/GaN, in which we expect a more controllable interface, was applied to passivation of AlGaN/GaN HFETs [27,34–37,70]. The AlN-passivated HFETs exhibit good heat release properties due to the high thermal conductivity of AlN [71] ($\sim$ 10 times higher than that of Al_2O_3), and also effective suppression of current collapse. Since AlN has a possible high breakdown field $\gtrsim$ 10 MV/cm [72,73] and a high dielectric constant $\sim$ 10 [74], which are comparable to those of Al_2O_3, the sputtering-deposited AlN can be a favorable gate dielectric for AlGaN/GaN MIS transistors, with the merits of a more controllable interface and better heat release properties. Although AlGaN/GaN MIS transistors with a sputtering-deposited AlN gate dielectric [27, 28], as well as an AlN/GaN MIS-FET obtained by metal-organic vapor phase epitaxy (MOVPE) growth of AlN/GaN and regrowth of an n^+-GaN Ohmic region [75], have been reported, sufficient device performance has not been shown, in particular, for forward gate leakage properties. In this work, we carried out characterization of sputtering-deposited AlN films and their applications to AlGaN/GaN MIS transistors as a gate dielectric, including suppressed forward gate leakage properties [29].

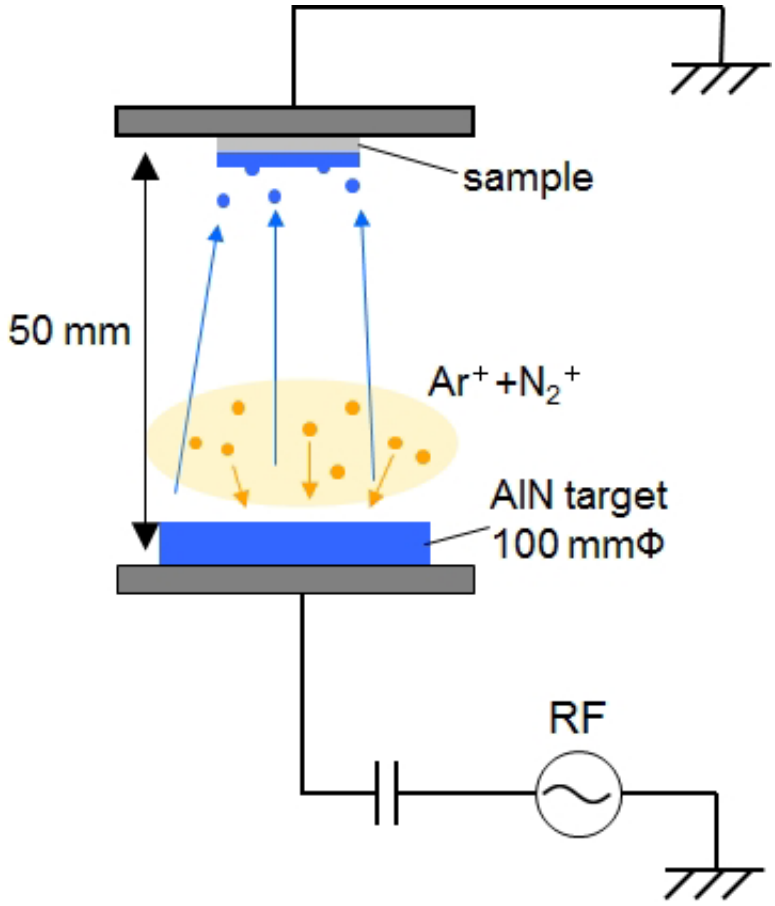

FIG. 3.11 Illustration of RF magnetron sputtering.

On the $Al_{0.29}Ga_{0.71}N$(25 nm)/GaN(3000 nm) heterostructure, AlN thin films were deposited at room temperature by RF magnetron sputtering using an AlN target in Ar-N_2 ambient with a working pressure of 0.2 Pa and a plasma power of 40 W. The illustration of sputtering process is shown in Fig. 3.11. On the AlGaN surface cleaned by organic solvents, deionized water, and oxygen plasma ashing to remove surface organic contaminants, followed by oxide removal using Semicoclean (ammonium-based etchant), an AlN gate insulator of $\sim$ 19 nm thickness was deposited.

The AlN films do not show X-ray diffraction peaks in Fig. 3.12, suggesting their amorphous nature. In addition, by ellipsometry, we measured refractive indices of the AlN films obtained by this sputtering deposition condition. As shown in Fig. 3.13, a refractive index of 1.94 at 630 nm wavelength is obtained, indicating the dense nature of the deposited AlN films.

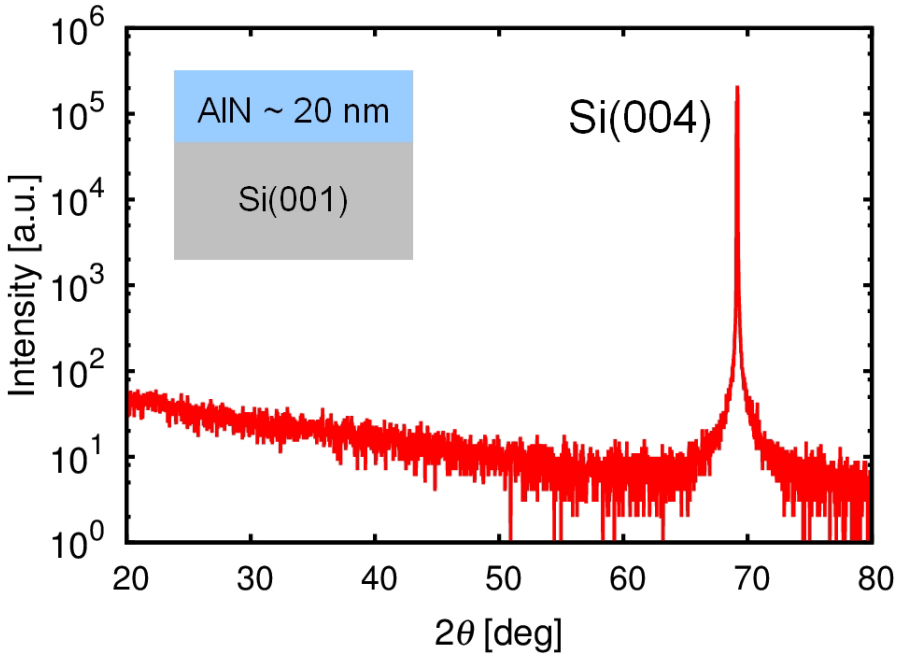

FIG. 3.12 XRD measurement of a sputtered AlN thin film.

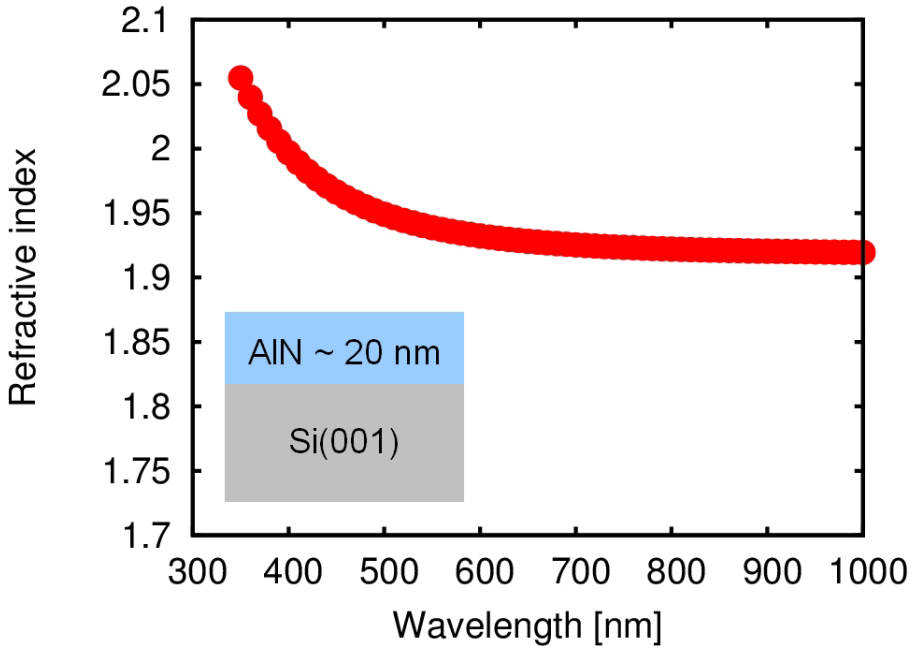

FIG. 3.13 Ellipsometry measurement of a sputtered AlN thin film.

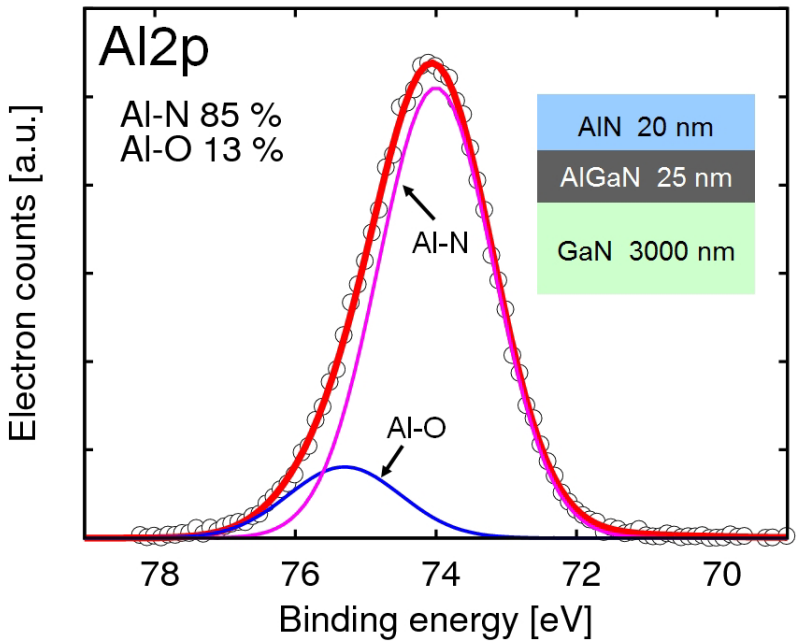

FIG. 3.14 Al2p peak of an AlN film by XPS measurement.

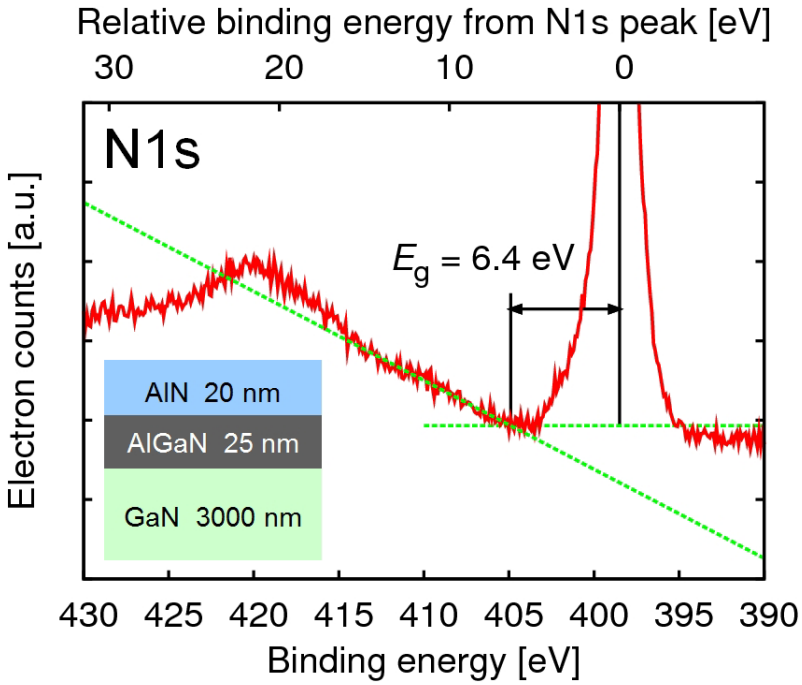

FIG. 3.15 N1s electron energy loss spectroscopy of an AlN film by XPS measurement.

The AlN films have also been investigated by X-ray photoelectron spectroscopy (XPS) with a take-off angle of 35°. Figure 3.14 shows an Al2p peak for an AlN film of $\sim$ 20 nm thickness. The Al2p signal is dominated by Al-N bonding, though the Al-O bonding was detected, which can be attributed to the residual oxygen in the film and the surface oxidation. Furthermore, the bandgap of the AlN was estimated by N1s electron energy loss spectroscopy, as shown in Fig. 3.15. We obtain the bandgap $E_g \sim 6.4$ eV, which is similar to the literature value of 6.2 eV [76].

Gate electrode formation

Gate electrode formation uses a high resolution positive electron beam resist ZEP520A-7 (ZEON Corp.). The single layer resist was employed without LOL2000 layer to prevent the etching of AlN insulator by the developer NMD-W (TOKYO OHKA KOGYO). Electron Beam Lithography System (ELIONIX ELS-7500) supplies a 30 keV electron beam for patterning. Figure 3.16 shows the optical image of the gate electrode in completion. In Fig. 3.17, we show the SEM images; the MIS transistors have the gate length of 250 nm, the source-gate spacing of 2 μm, the gate-drain spacing of 3 μm, and the gate width of 50 μm. For the MIS capacitors, the 100 μm $\times$ 100 μm gate electrode is surrounded by the Ohmic electrode as shown in Fig. 3.18. Gate electrode formation process is described in Tab. 3.4.

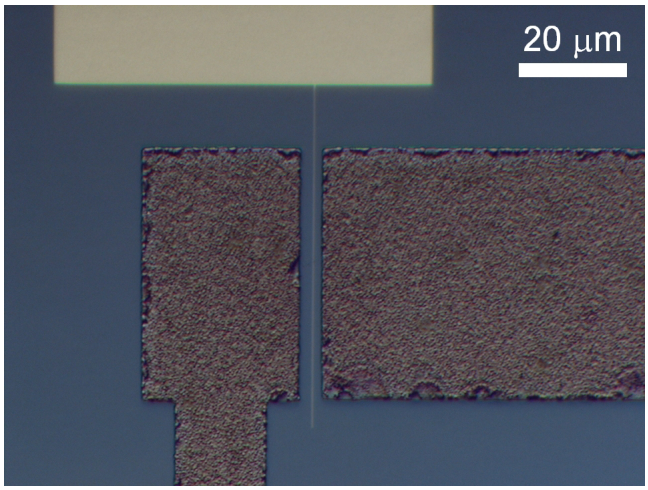

FIG. 3.16 Optical image of the gate electrode of the MIS transistor.

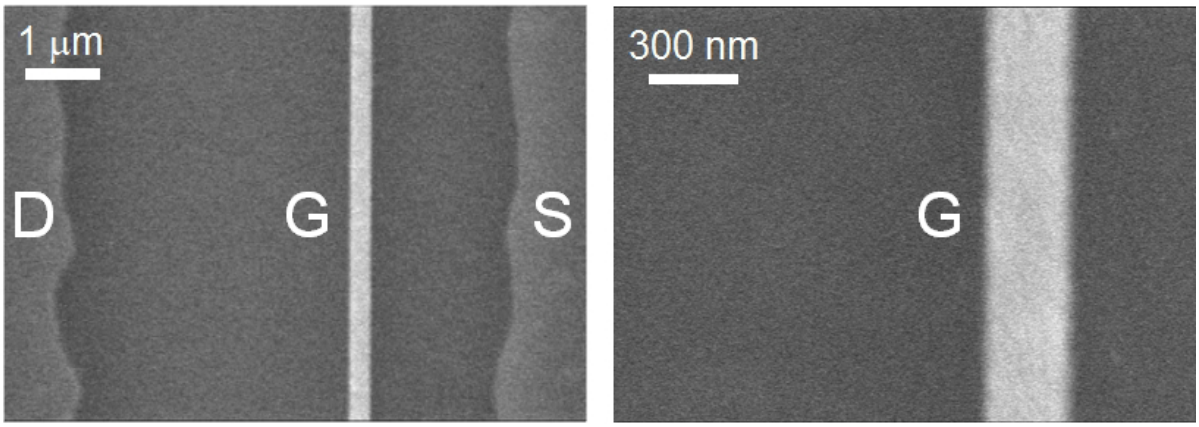

FIG. 3.17 Optical image of the gate electrode of the MIS transistor.

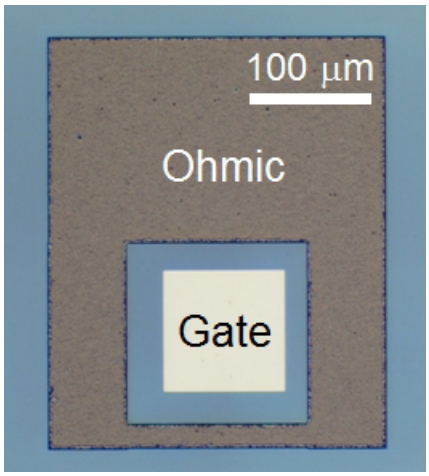

FIG. 3.18 Optical image of the MIS capacitor.

Table 3.4 Process of gate electrode formation

Processes	Conditions
baking	bake(180 ℃ 5 min)
resist coating	ZEP520-A7(4000 rpm 60 s), bake(120 ℃ 180 s)
	Espacer(1500 rpm 60 s), bake(100 ℃ 180 s)
patterning	exposure (gate) 50 keV 50 pA pitch1 2.7 μs($\sim$ 135 μC/cm^2)
	exposure (pad) 50 keV 50 pA pitch3 9.0 μs($\sim$ 150 μC/cm^2)
	Espacer removal: DIW(60 s)
	development ZED-N50(60 s), ZMD-B(30 s), N_2 blow
surface treatment	O_2 plasma ashing 50 Pa 10 W 10 s
deposition	Ni/Au=5/35 nm
lift-off	1165(60 ℃)
	acetone, methanol, DIW 3 min each

Device dimensions

The completed MIS devices have dimensions shown in Fig. 3.19.

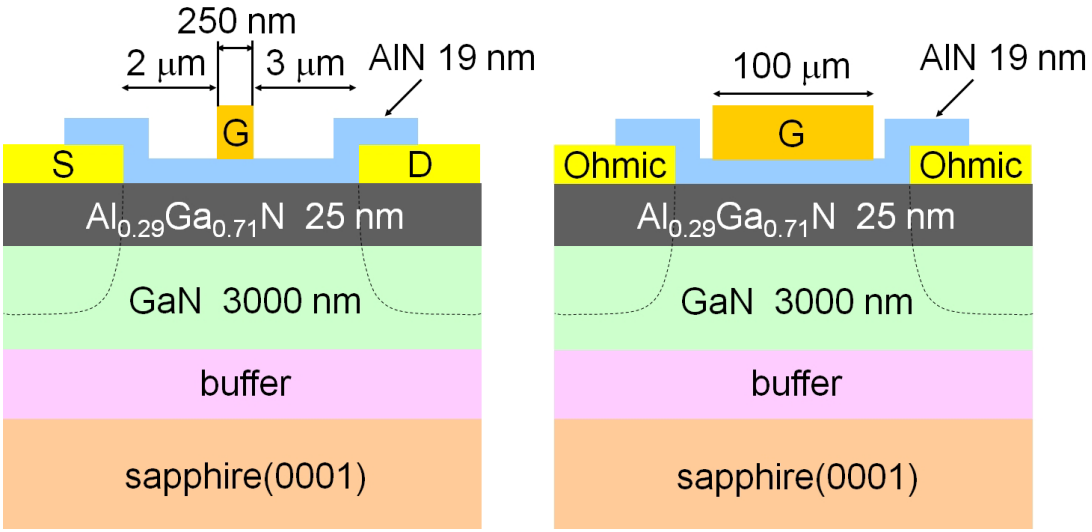

FIG. 3.19 Device dimensions of the fabricated MIS devices.

3.2 DC characterization

We carried out DC characterization for the fabricated AlN/AlGaN/GaN MIS devices. In Fig. 3.20(top), we show the output characteristics of the fabricated MIS transistor, which exhibits no kink effect. Although we observed a slightly high on-resistance of $\sim$ 15 $\Omega \cdot$ mm, a current drivability with a drain current of 550 mA/mm is obtained. There is almost no negative conductance, suggesting good heat release properties. Figure 3.20(bottom) shows the transfer characteristics under the gate voltage sweep of -18 V $\rightarrow +6$ V $\rightarrow -18$ V. According to the insertion of the AlN gate dielectric between the gate metal and the AlGaN, the transconductance is not so high; the maximum transconductance is 100 mS/mm. Moreover, we observe a rapid decrease in the transconductance towards forward gate biases, suggesting poor AlN/AlGaN interface properties, which will be analyzed later. It should be noted that, owing to the good insulating properties of the AlN gate dielectric, the gate leakage currents are significantly small, 10^{-9} A/mm range or less, for both reverse and forward biases. The small leakage currents lead to the small drain off-currents, which exhibit more than 4 orders reduction in comparison with those of Schottky HFETs fabricated from the same AlGaN/GaN heterostructure.

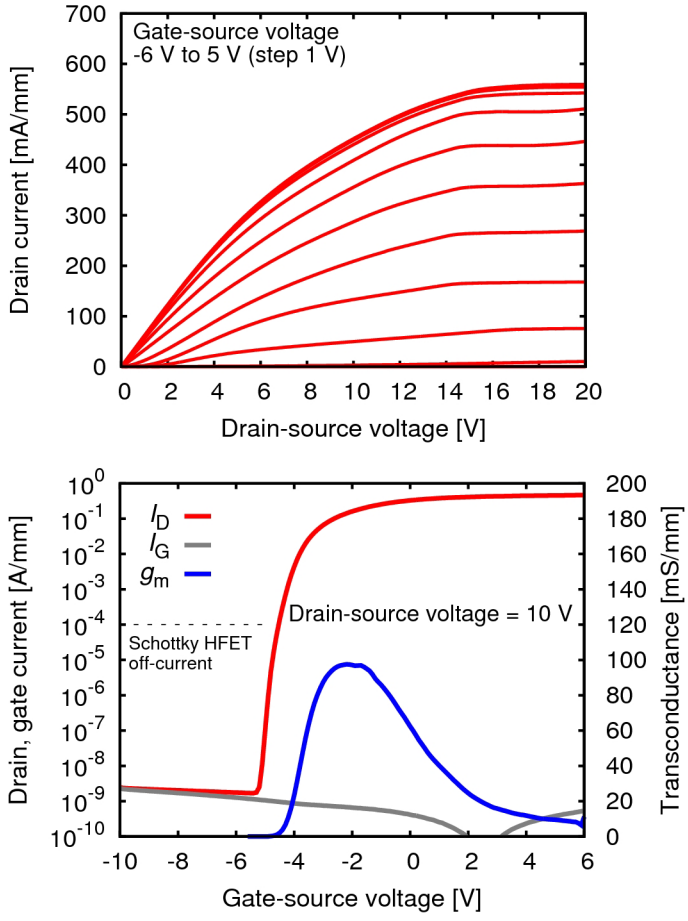

FIG. 3.20 Output (top) and transfer (bottom) characteristics of the AlN/AlGaN/GaN MIS transistor.

Figure 3.21 shows the gate-source two-terminal (drain open) I-V characteristics; we observe the gate current of 1×10^{-9} A/mm at a reverse voltage of -18 V, and 6×10^{-10} A/mm even at a forward voltage of $+5$ V, showing one of the most significant suppressions of forward gate leakage currents in AlGaN/GaN MIS transistors. Figure 3.22 shows the I-V characteristics of the fabricated MIS capacitor; we observe the current of 10^{-8} A/cm^2 range for both forward and reverse biases.

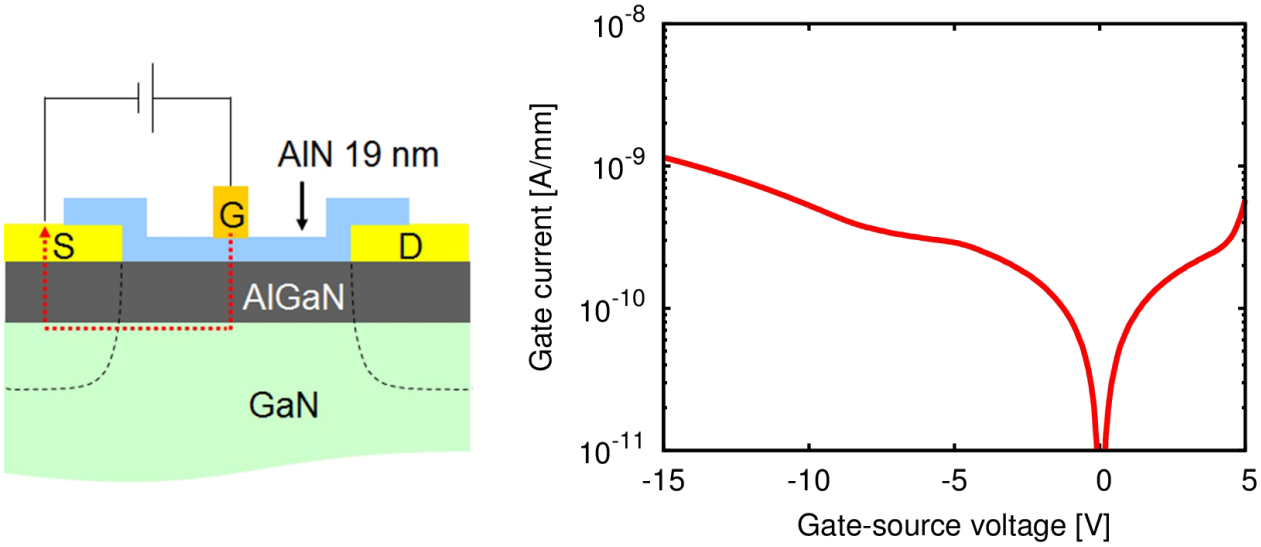

FIG. 3.21 Gate-source two-terminal (drain open) I-V characteristics.

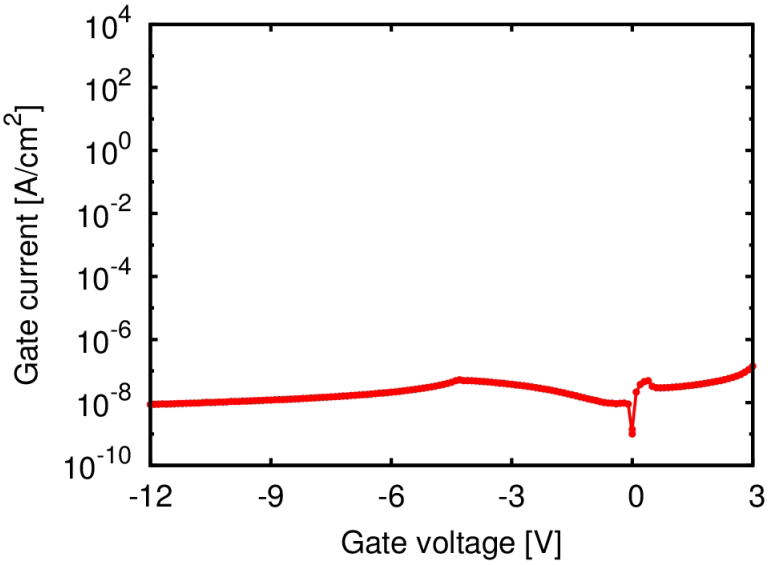

FIG. 3.22 I-V characteristics of the fabricated MIS capacitor.

3.3 Characterization by using C-f-T mapping method: A comparison with conventional conductance method

We investigated the AlN/AlGaN/GaN MIS capacitors to analyze the AlN-AlGaN interface states. We measured C-V-f characteristics between the gate electrode and the grounded Ohmic electrode surrounding the gate of the MIS capacitors at temperatures from 150 K to 393 K. The measurement system is illustrated in Fig. 3.23.

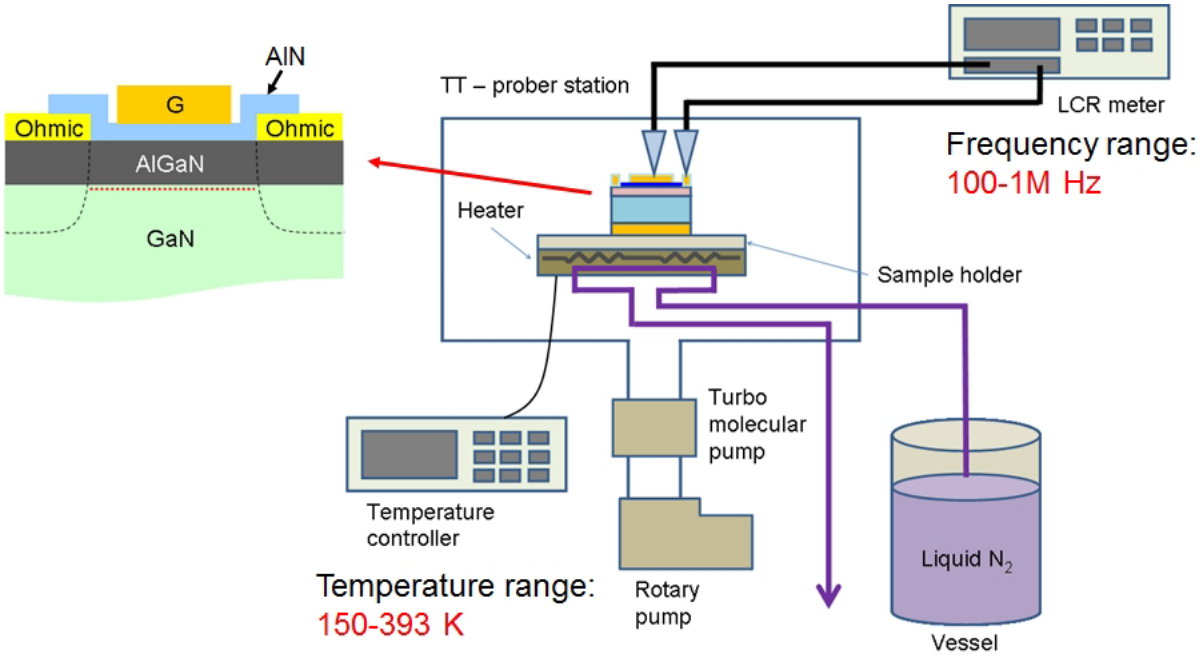

FIG. 3.23 Prober system for temperature-dependence measurement of C-V-f characteristics.

Figure 3.24 shows the C-V-f characteristics at 150 K, 300 K, and 393 K. At 393 K, we observe a significant frequency dispersion for forward gate biases, which is attributed to electron trapping/detrapping at interface states, while the frequency dispersion disappears at 150 K because of much longer electron trapping time constants. To characterize the interface states quantitatively, we carried out an analysis using the conductance method described previously.

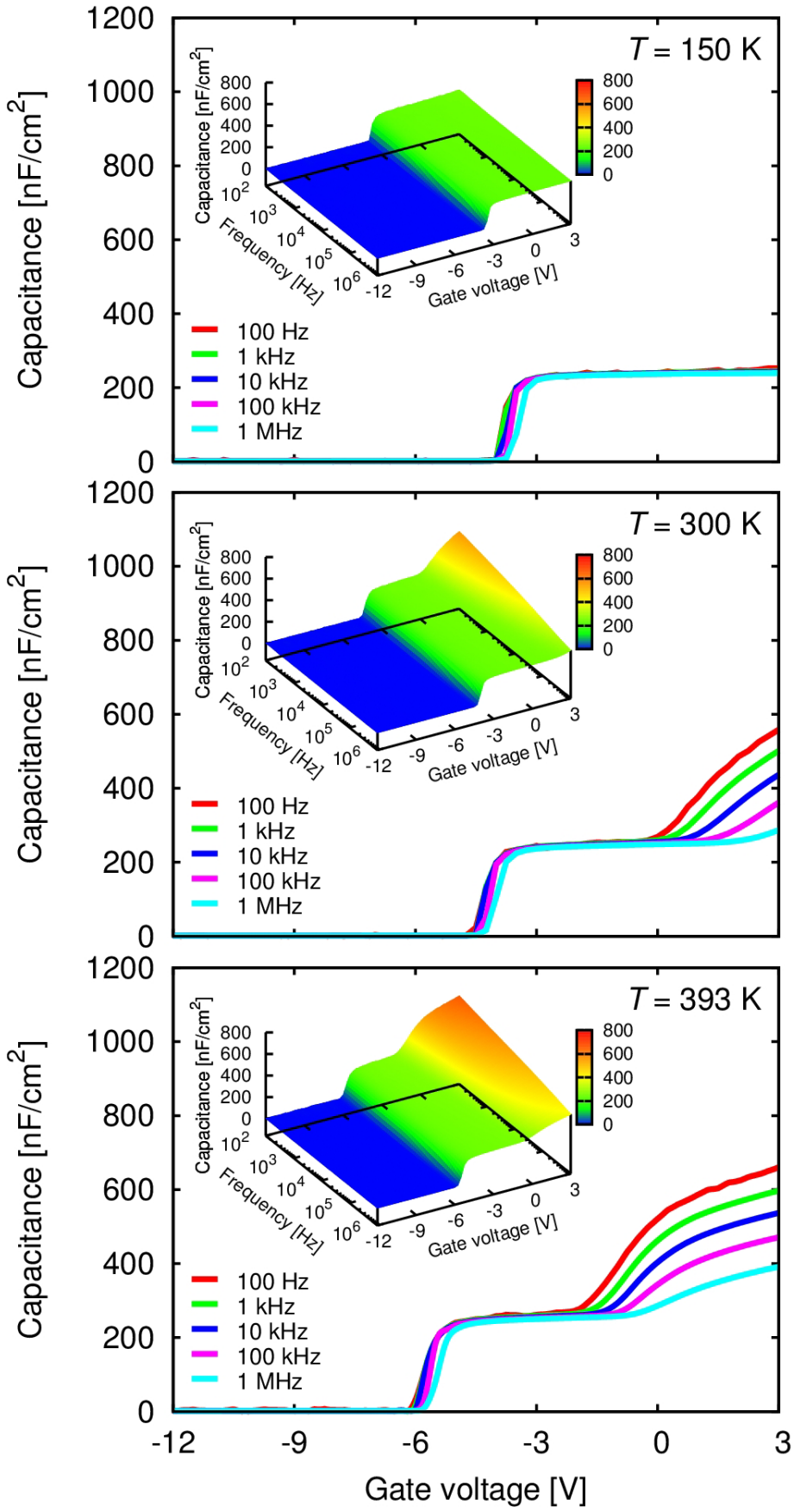

FIG. 3.24 C-V-f characteristics of the AlN/AlGaN/GaN MIS capacitor at 150 K, 300 K, and 393 K.

Assuming the designed value of the insulator capacitance $C_0 = 610$ nF/cm^2, we show frequency dependence of G_i/ω, for several temperatures and gate voltages of 0 V, 1.5 V, and 3 V, in Fig. 3.25. As the gate voltage decreases, the number of peaks decreases due to longer time constants for deeper interface state energy levels. Thus, only a narrow range of the gate biases gives peaks in the measured frequency and temperature range; most peaks are below 100 Hz due to significantly long time constants for the wide bandgap of AlGaN/GaN systems.

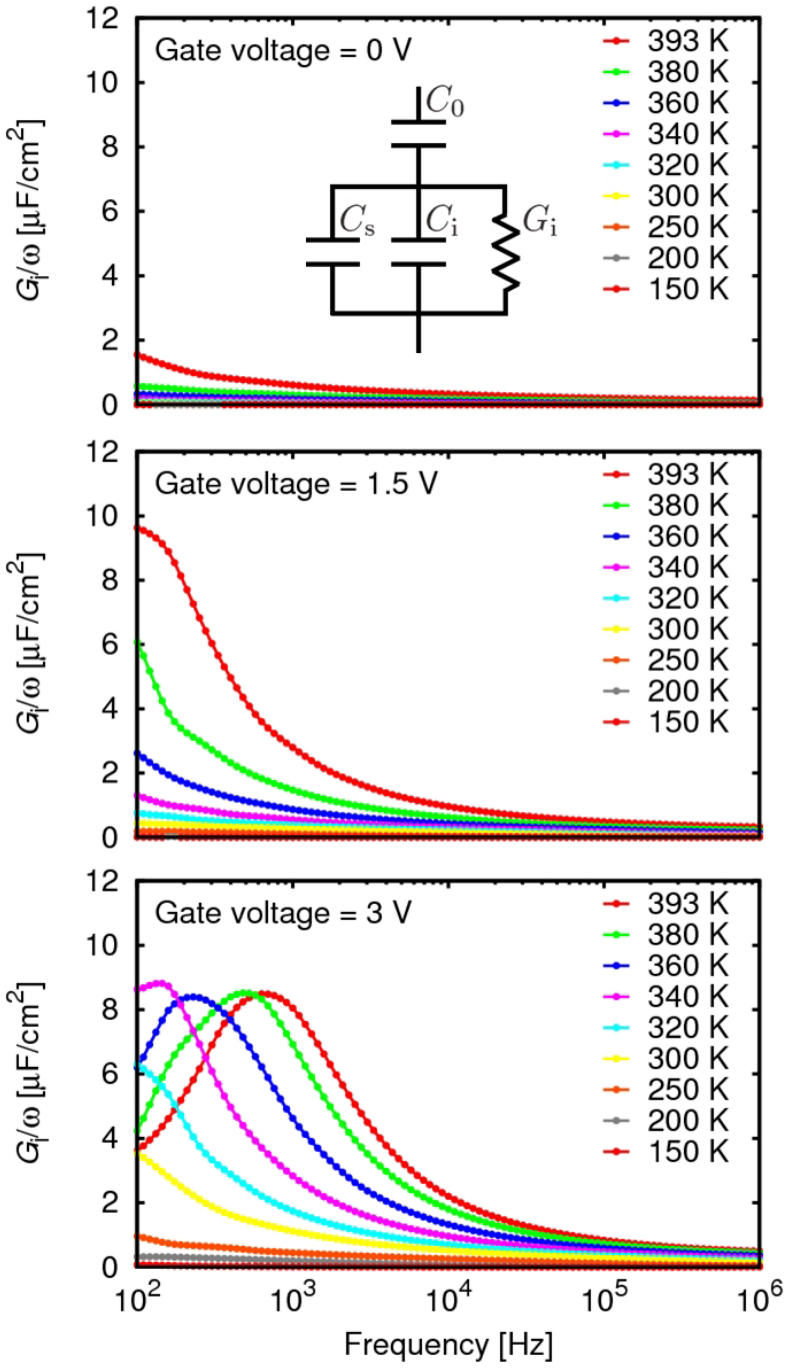

FIG. 3.25 Frequency dependence of G_i/ω for temperatures from 393 K to 150 K at gate voltages of 0 V, 1.5 V, and 3 V. Top inset: the equivalent circuit of the MIS capacitor.

From the few peak positions and values, $D_{\rm i}$ and τ for temperatures of 340-393 K are obtained as shown in Fig. 3.26 (a) and (b), respectively, where $D_{\rm i} \sim 10^{14}$ cm^{-2}eV^{-1} and $\tau \sim$ ms. From the Arrhenius plot of the temperature dependence of τ shown in Fig. 3.26 (c), given by $\tau = \tau_0 \exp\left(E_{\rm a}/k_{\rm B}T\right) = \tau_0 \exp(\beta E_{\rm a})$, we extracted the activation energy $E_{\rm a}$ shown in Fig. 3.26 (d) and estimated $\tau_0 \sim 10$ ns. However, the conventional conductance method to investigate interface states is available only for a narrow range of gate biases, prohibiting the analysis of deeper interface states.

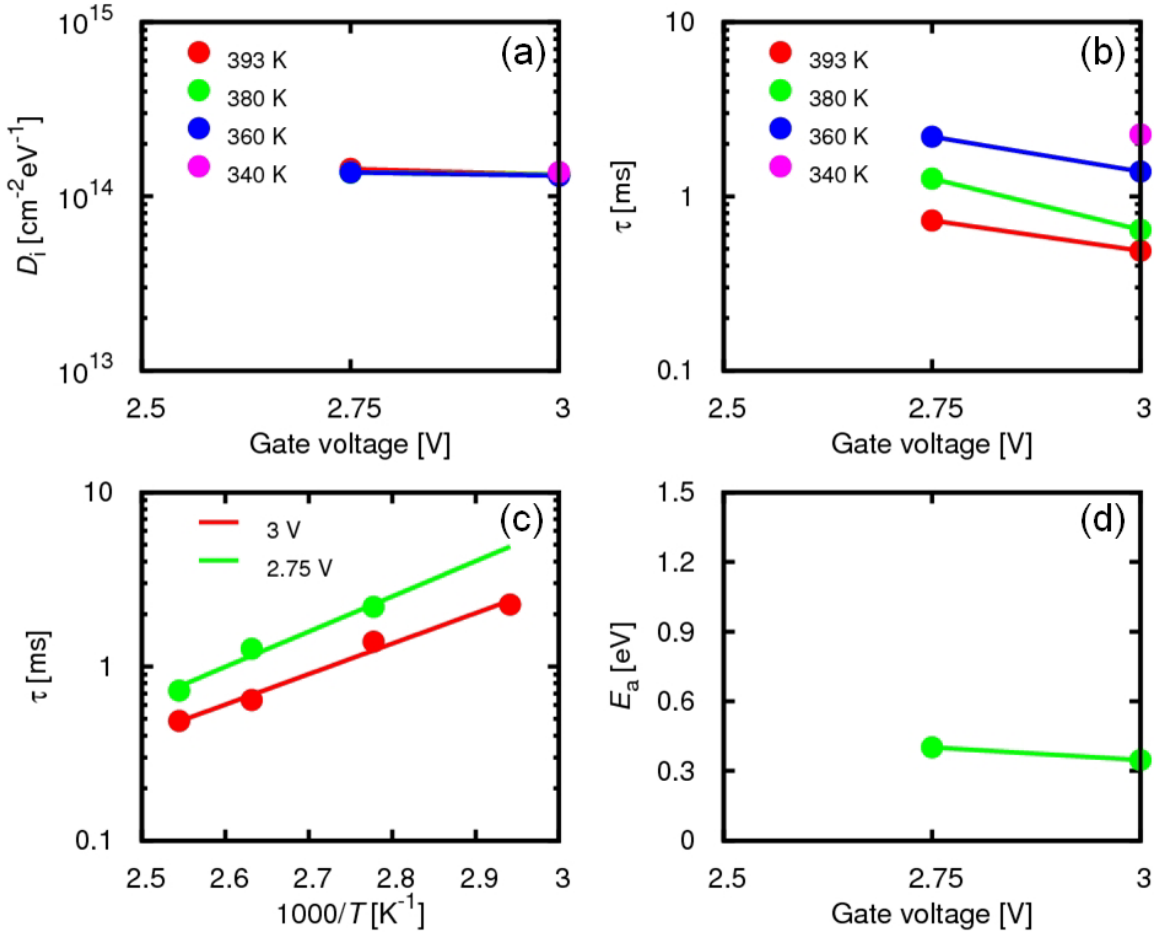

FIG. 3.26 (a) Interface state density $D_{\rm i}$ and (b) electron trapping time constant τ, obtained from the peak values and positions of the frequency-dependent $G_{\rm i}/\omega$ based on the conductance method. (c) The Arrhenius plot of the temperature-dependent τ. (d) The activation energy $E_{\rm a}$ as a function of gate voltage, obtained from the Arrhenius plot (c).

Using the proposed C-f-T mapping method, we carried out an analysis using the C-f-T mapping obtained from the temperature-dependent C-V-f characteristics. In Fig. 3.27, we show the C-f-T mappings at gate voltages of 0 V, 1 V, 2 V, and 3 V, with contours. The contours exhibit the straight line behavior as explained previously, from which the activation energy $E_{\rm a}$ corresponding to the interface state energy level can be extracted.

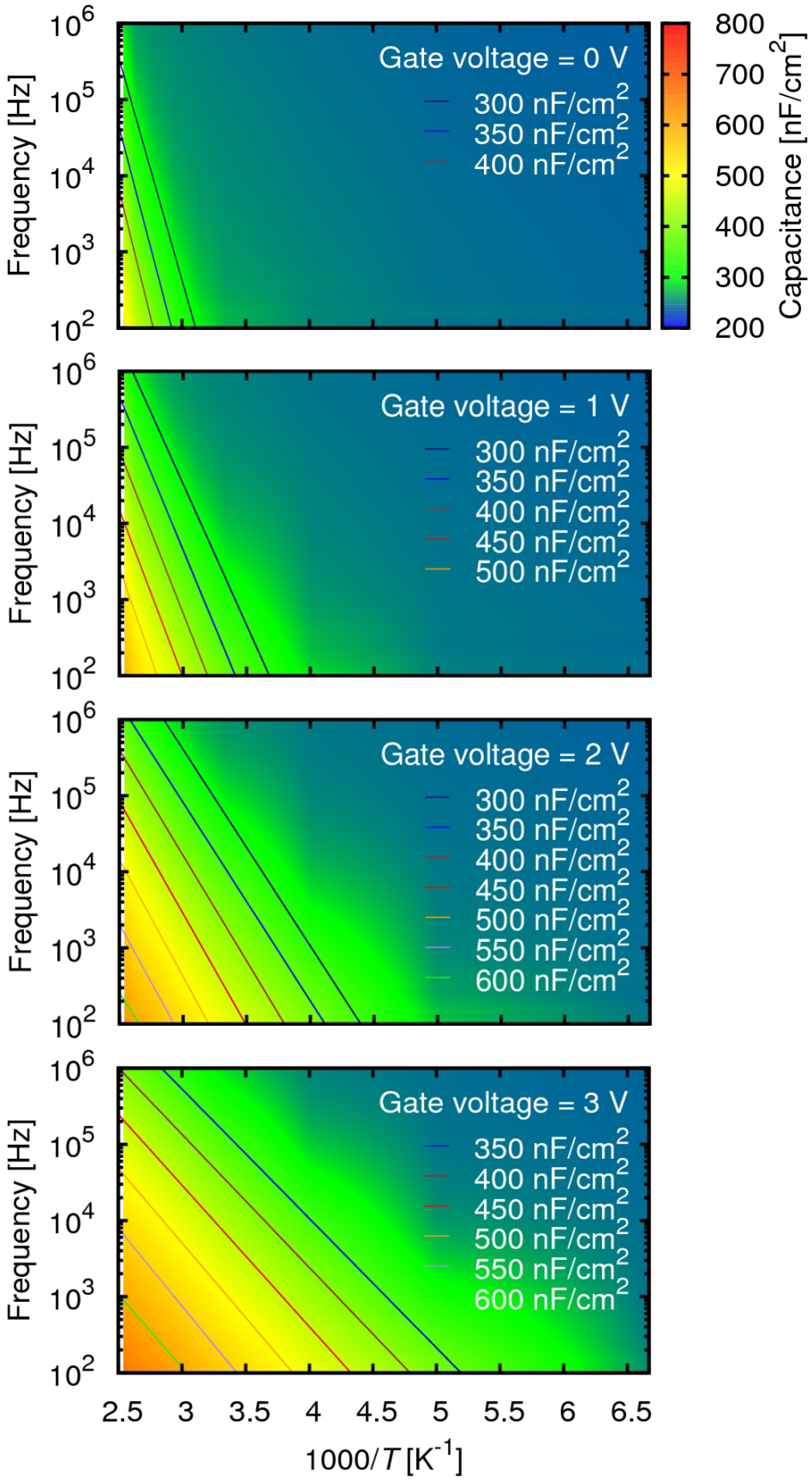

FIG. 3.27 C-f-T mappings with contours at gate voltages of 0 V, 1 V, 2 V, and 3 V.

Figure 3.28 shows the gate voltage V_G dependence of E_a extracted from the contours in the C-f-T mappings, with the inset illustrating the bandbending and E_a. In addition to the fact that the obtained values of E_a for the gate voltage ≥ 2.75 V are in good agreement with those obtained by the conductance method, we find that E_a can be obtained for a much extended range of the gate biases. This is due to slow $\omega\tau$ dependence of Eqs. (2.20) and (2.21); even though the frequency is far from the peak position $\sim 1/\pi\tau$, change in the C-f-T mapping is detectable.

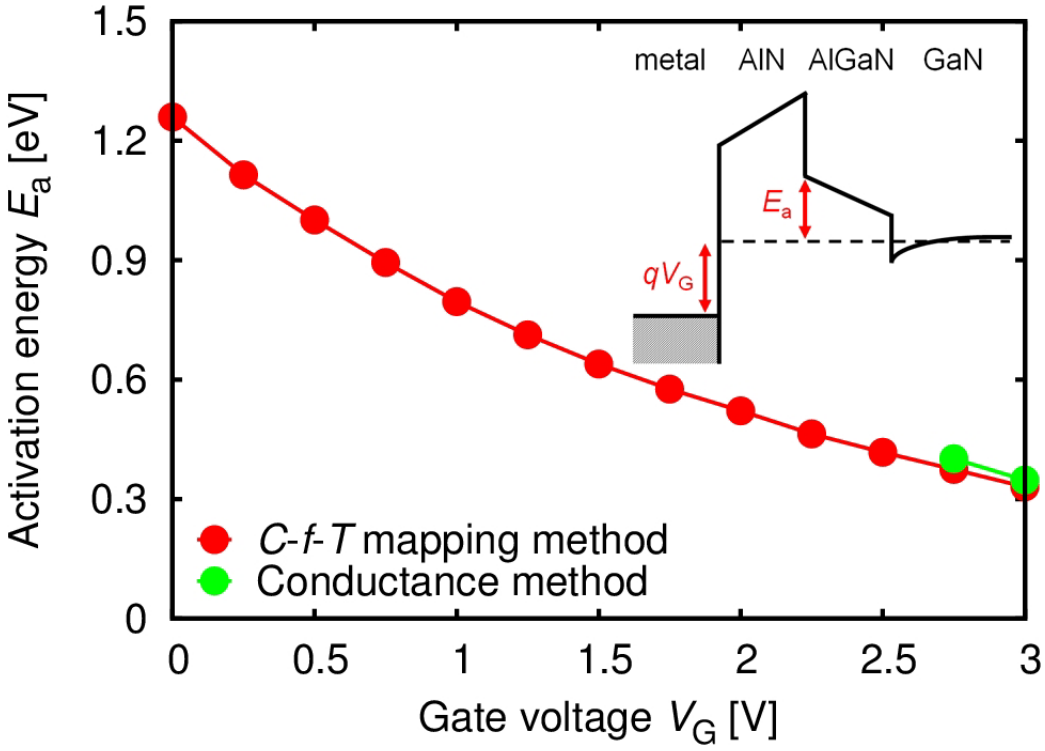

FIG. 3.28 Gate voltage V_G dependence of activation energy E_a obtained by C-f-T mapping method and conductance method. Inset: illustration of the bandbending and E_a.

3.4 Application of C-f-T mapping method to device process comparison

To exemplify the effectiveness of the analysis method, we employed AlN/AlGaN/GaN MIS devices with two types of the AlN-AlGaN interface formation processes, by using two types of surface treatments of the AlGaN before the AlN gate insulator deposition. The first type surface treatment includes an organic cleaning by organic solvents and oxygen plasma ashing, and an additional cleaning by an ammonium-based solution, ABS (with cleaning by ABS). The second one includes only the organic cleaning, without the additional cleaning (without cleaning by ABS). The organic solvents and the oxygen plasma ashing were used for removing organic contaminants, whereas the ABS was used with the intention to avoid oxidation and nitrogen vacancy [77]. While the devices without cleaning by ABS were transferred to the sputtering chamber within 15 min after the treatment, the ones with cleaning by ABS were transferred within 5 min after the treatment to prevent surface re-oxidation. An AlN gate insulator of $\simeq$ 19 nm thickness was then deposited on the AlGaN surfaces by RF magnetron sputtering at room temperature with an AlN target in Ar-N_2 ambient. From Hall-effect measurements after the AlN deposition, we obtain electron mobilities $\mu \simeq 900$ cm^2/V-s and 1100 cm^2/V-s with sheet electron concentrations $n_s \simeq 6.5 \times 10^{12}$ cm^{-2} and 7.0×10^{12} cm^{-2}, for the devices with and without cleaning by ABS, respectively, suggesting that the cleaning by ABS leads to further sputtering damage. The formation of Ni/Au gate electrodes completed the device fabrication. The MIS transistors have the gate length of 250 nm, the source-gate spacing of 2 μm, the gate-drain spacing of 3 μm, and the gate width of 50 μm, while the MIS capacitors have the 100 μm $\times$ 100 μm gate electrode surrounded by the Ohmic electrode. The process flow is illustrated in Fig. 3.29.

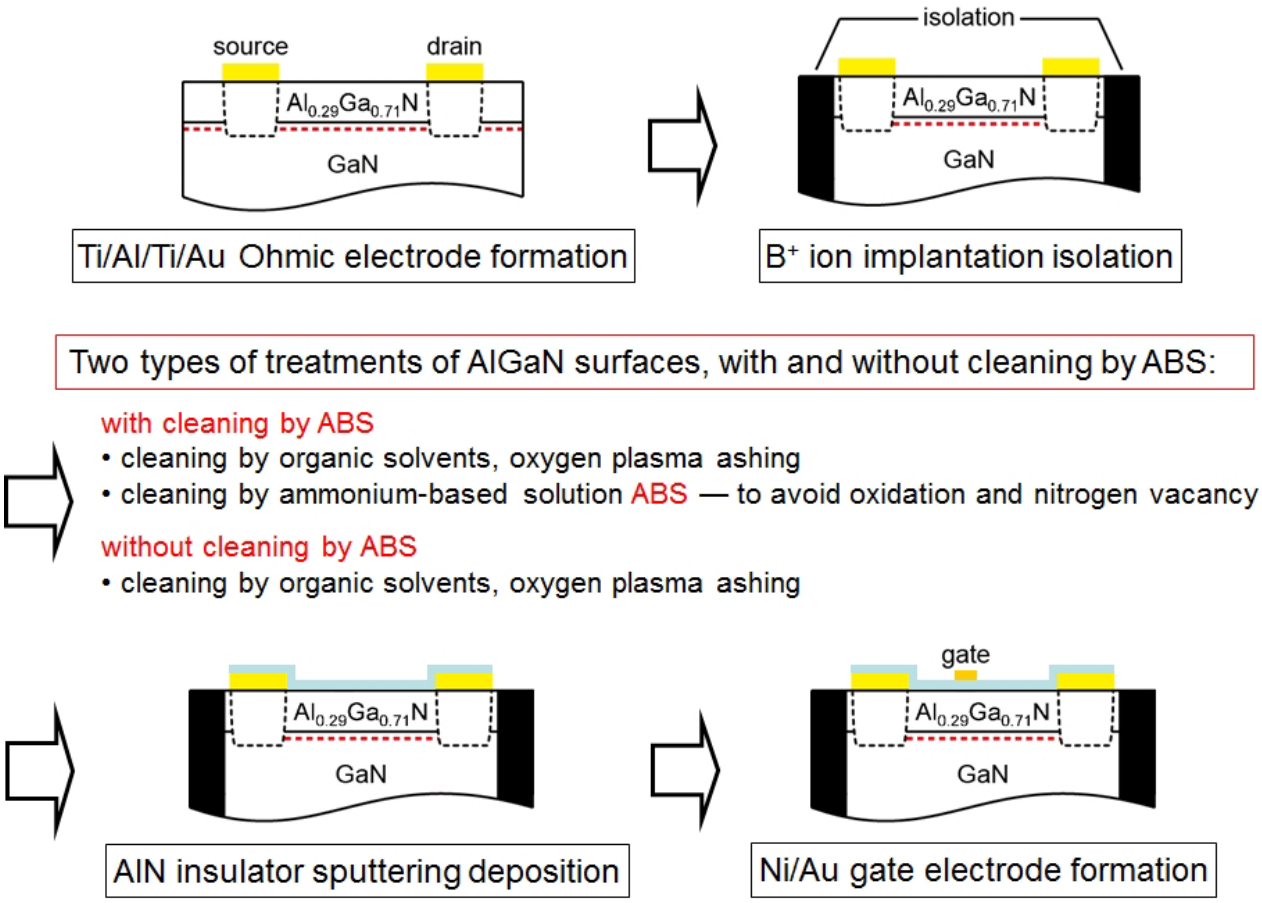

FIG. 3.29 Flow chart for device process comparison: two types of AlGaN surface treatments.

In Fig. 3.30 and 3.31, we show output and transfer characteristics of the fabricated MIS transistors, respectively, for the first type surface treatment (with cleaning by ABS) and the second one (without cleaning by ABS). Owing to the high thermal conductivity of AlN, there is almost no negative conductance even at high source-drain voltage V_{D}, suggesting good heat release properties of the MIS transistors. The maximum drain current I_{D} is lower for the MIS transistor with the cleaning by ABS than for the MIS transistor without the cleaning by ABS, suggesting that the cleaning leads to further sputtering damage. For both surface treatments, owing to good insulating properties of the AlN, gate leakage currents are significantly small, 10^{-9} A/mm range or less, for both reverse and forward gate biases. The small gate leakage currents lead to small drain off-currents shown in Fig. 3.31. However, we observe rapid decreases in the transconductances g_{m} towards forward gate biases, suggesting high-density AlN/AlGaN interface states. In particular, the MIS transistor without surface cleaning by ABS exhibits a more suppressed transconductance behavior at forward biases than the MIS transistor with the cleaning by ABS. We also investigated the gate leakage currents with the drain open for both treatments as shown in Fig. 3.32. The current levels are at the order of nA/mm not only for the reverse biases but also the forward biases, which means significant suppression of gate leakage currents is achieved. Figure 3.33 shows the I-V characteristics of the fabricated MIS capacitors; we observe the current levels of less than 10^{-6} A/cm^2 range for both forward and reverse biases.

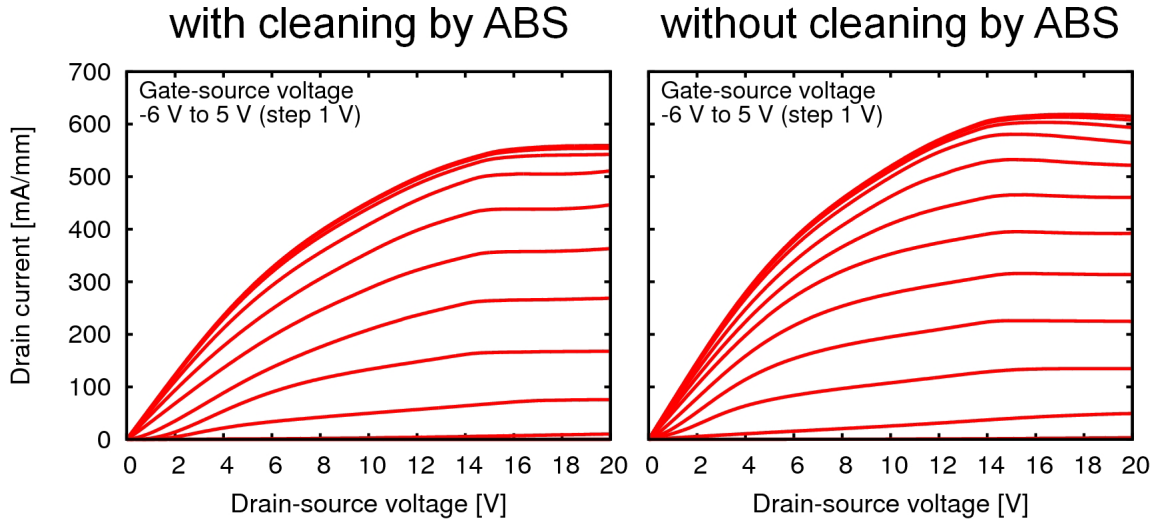

FIG. 3.30 (Process comparison) Output characteristics of the AlN/AlGaN/GaN MIS transistors.

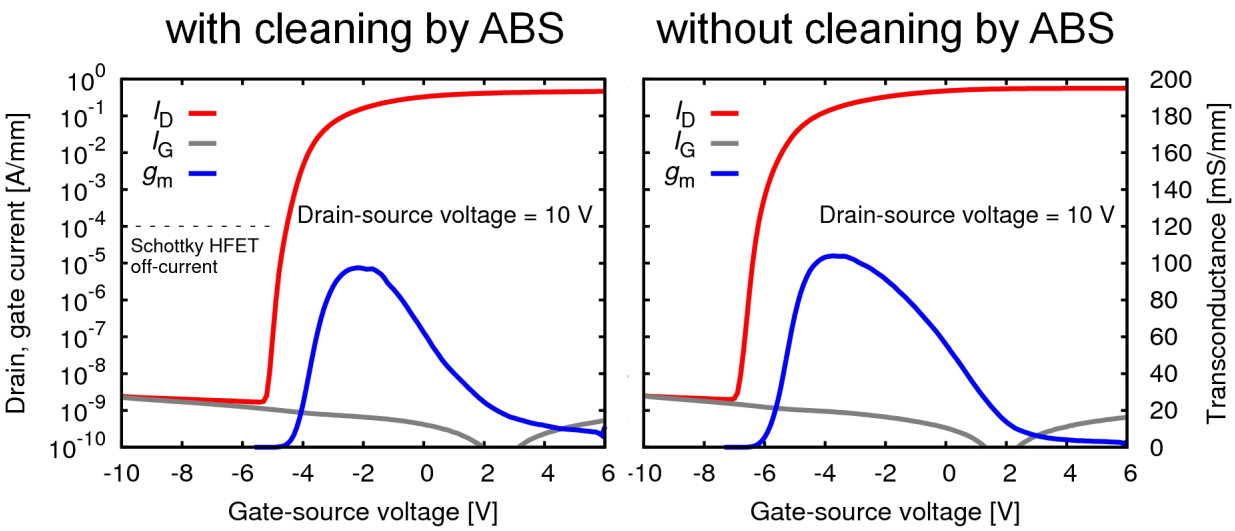

FIG. 3.31 (Process comparison) Transfer characteristics of the AlN/AlGaN/GaN MIS transistors.

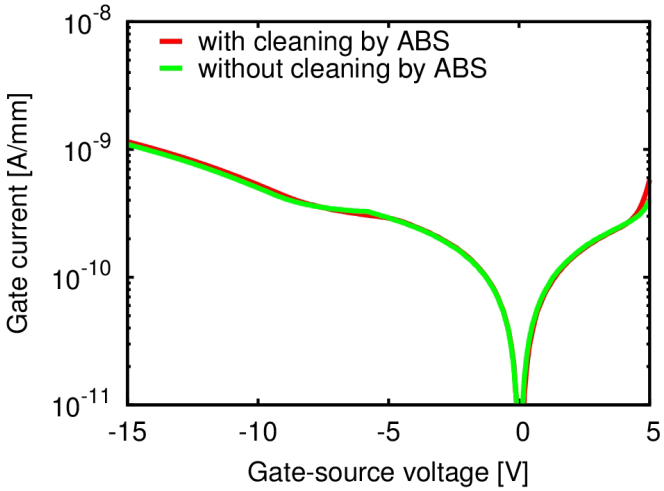

FIG. 3.32 (Process comparison) Gate-source two-terminal (drain open) I-V characteristics of the fabricated MIS transistors.

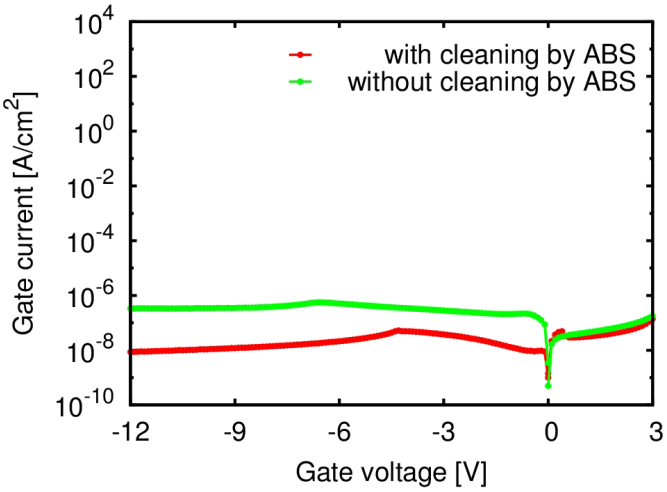

FIG. 3.33 (Process comparison) I-V characteristics of the fabricated MIS capacitors.

We investigated the AlN/AlGaN/GaN MIS capacitors to analyze the AlN-AlGaN interface states. We measured C-V-f characteristics between the gate electrode and the grounded Ohmic electrode surrounding the gate of the MIS capacitors at temperatures from 150 K to 393 K. Figure 3.34 shows the C-V-f characteristics at 150 K, 300 K, and 393 K for the devices with and without cleaning by ABS. At 393 K, for both surface treatments, we observe frequency dispersions at forward gate biases, which are attributed to electron trapping/detrapping at interface states, while the frequency dispersions disappear at 150 K because of long trapping time constants. The device with cleaning by ABS exhibits smaller frequency dispersions at forward biases than the device without the cleaning, suggesting that the cleaning is effective to suppress the frequency dispersions caused by the interface states.

From the temperature-dependent C-V-f characteristics, we obtain C-f-T mappings with contours for the devices with and without cleaning by ABS as shown in Fig. 3.35, where the gate voltages V_{G} are 0 V, 1 V, 2 V, and 3 V.

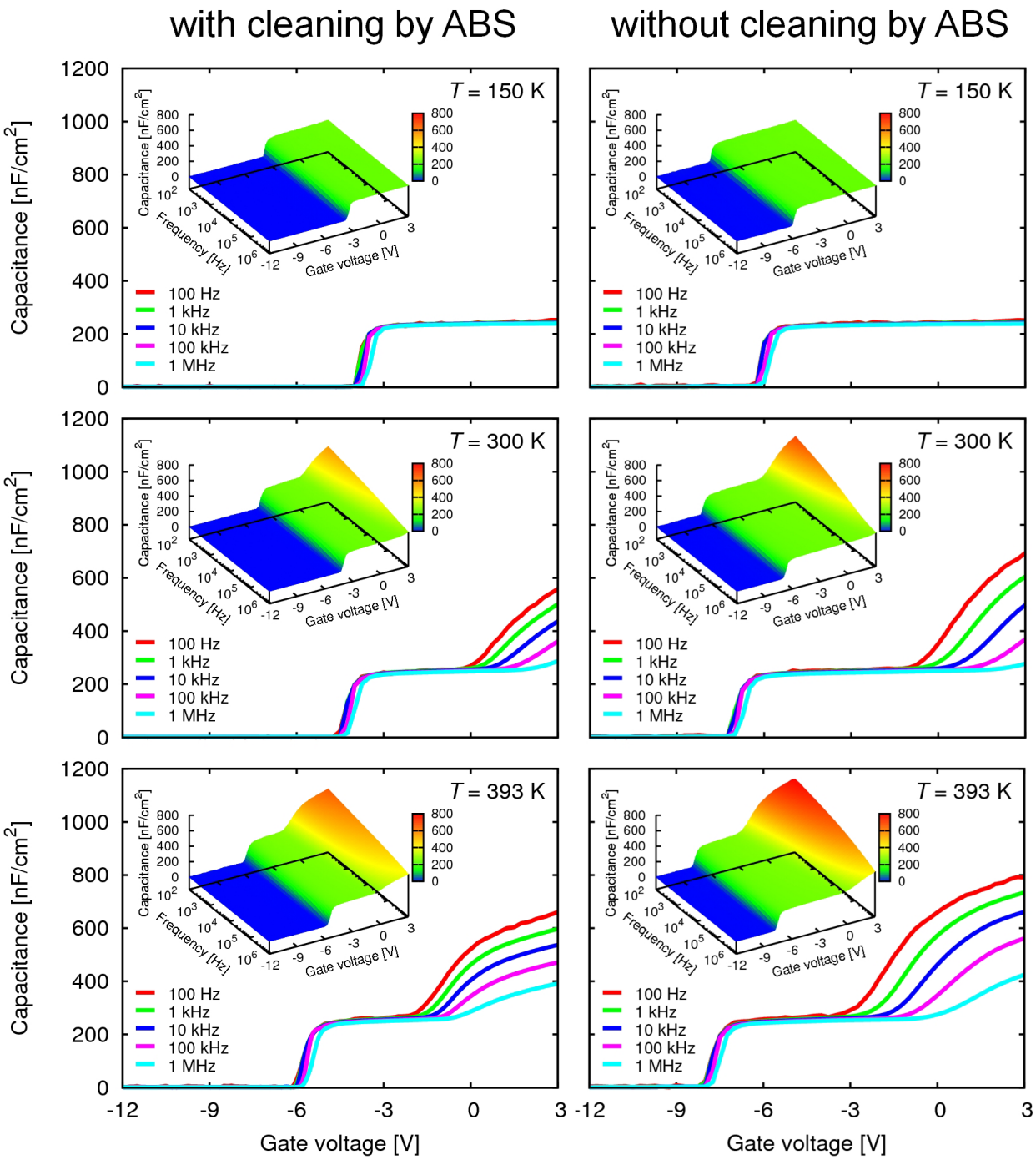

FIG. 3.34 (Process comparison) C-V-f characteristics of the AlN/AlGaN/GaN MIS capacitors at 150 K, 300 K, 393 K.

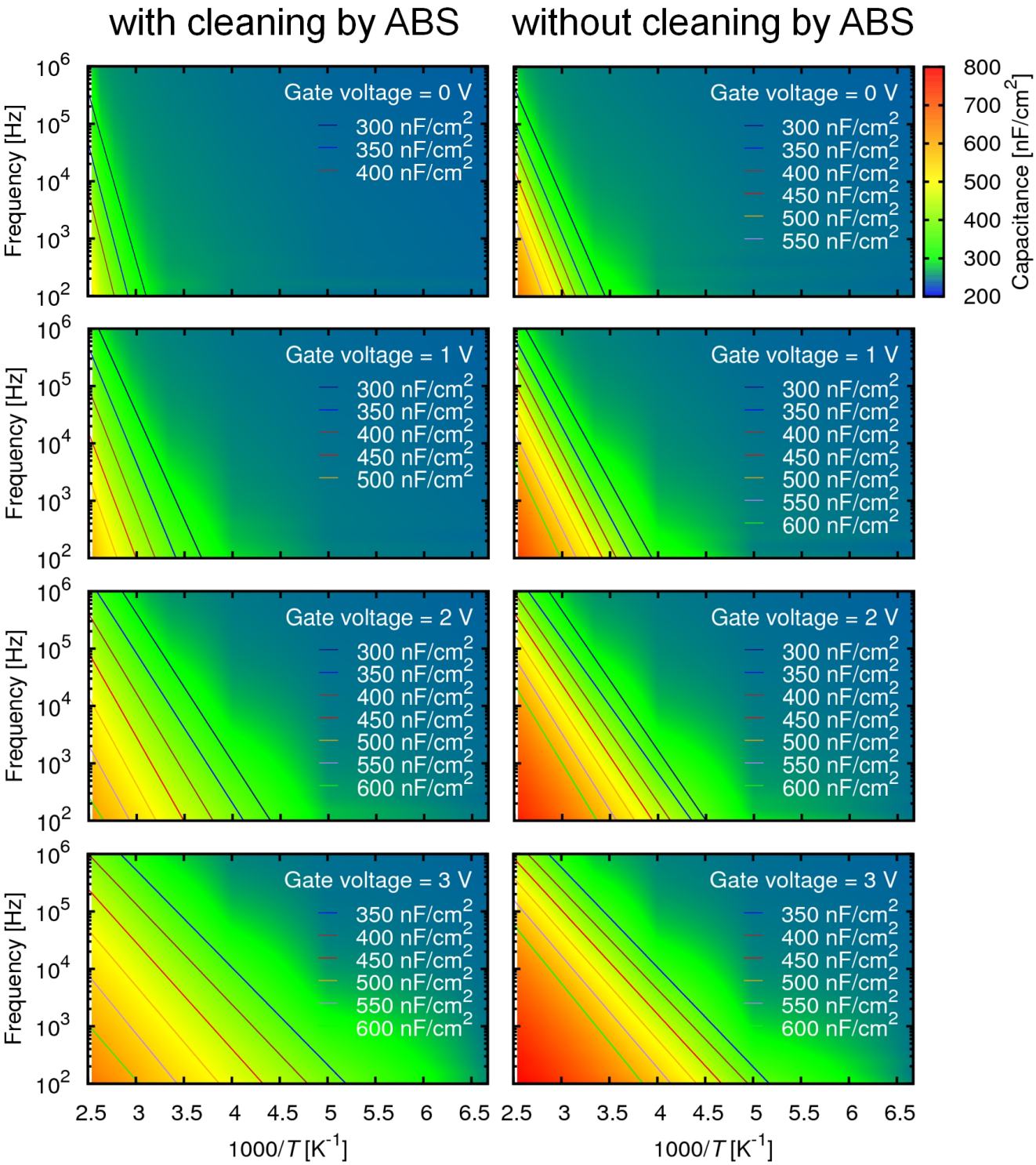

FIG. 3.35 (Process comparison) C-f-T mappings with contours at gate voltages of 0 V, 1 V, 2 V, and 3 V.

Figure 3.36 shows the gate voltage dependence of E_a extracted from the contours in the C-f-T mappings. For both surface treatments, the C-f-T mappings give activation energies for a wide range of gate biases, being effective for characterization of deep interface states. Even though peaks of G_i/ω as functions of the frequency used in the conductance method are often not detectable because of being located in the very low-frequency region due to long trapping time constants, we can obtain the activation energies from the contours in the C-f-T mappings. It is obvious that the activation energy is modulated by the gate voltage more effectively for the devices with cleaning by the ABS.

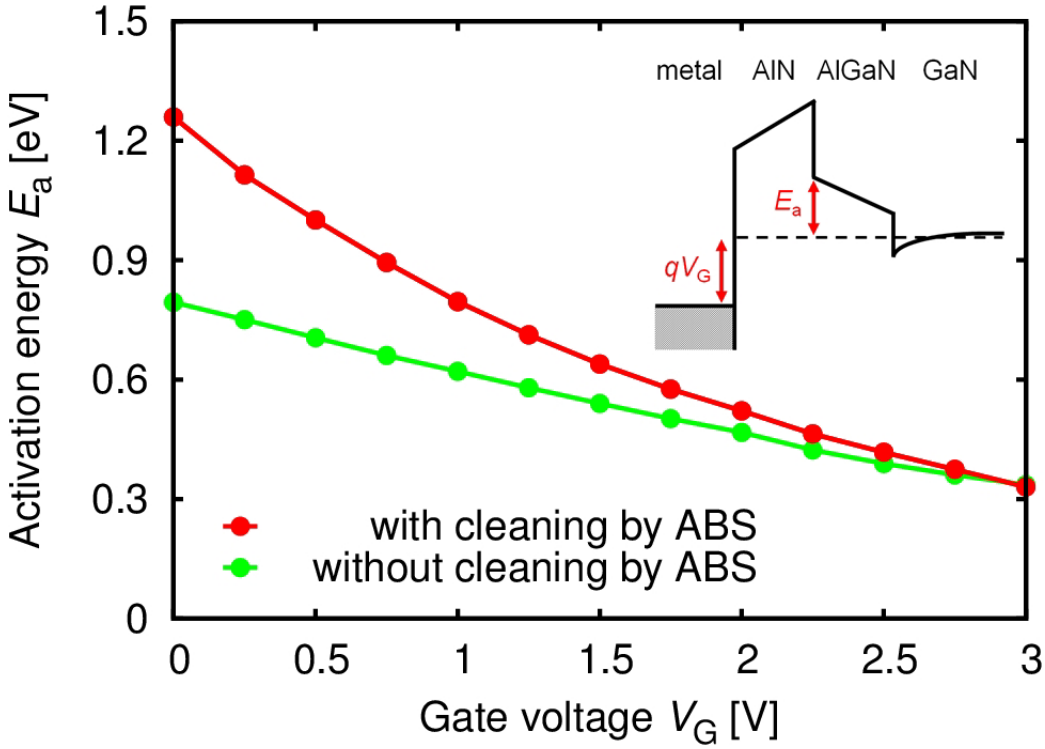

FIG. 3.36 (Process comparison) Gate voltage V_G dependence of E_a obtained by the C-f-T mappings.

3.4.1 Gate-control efficiency and interface state density

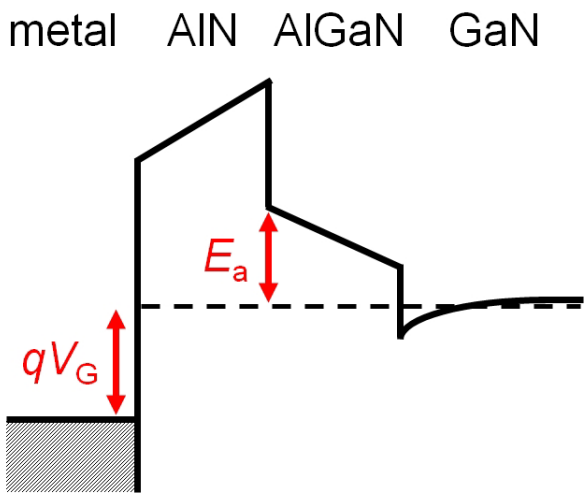

FIG. 3.37 Illustration of the bandbending and E_a.

As shown in Fig. 3.37, since the small gate-voltage change ΔV_G is divided into the bandbending change in the gate insulator AlN, ΔV_{AlN}, and that in the semiconductor AlGaN/GaN, $-\Delta E_a/q$, namely $\Delta V_G \simeq \Delta V_{AlN} - \Delta E_a/q$, we obtain

$$\frac{\Delta V_{AlN}}{\Delta V_G} - \frac{\Delta E_a}{\Delta(qV_G)} \simeq 1. \tag{3.2}$$

From the activation energies E_a depending on the gate voltage V_G given in Fig. 3.36, we obtain the gate-control efficiencies $\xi = -\Delta E_a/\Delta(qV_G)$ as shown in Fig. 3.38, i.e., the ratio of the bandbending change in the semiconductor to the total gate voltage change. In the AC case, a small-signal gate voltage Δv_G is divided into the bandbending in the gate insulator AlN, Δv_{AlN}, and that in the semiconductor AlGaN/GaN according to the equivalent circuit shown in Fig. 3.39(left). The ratio $\Delta v_{AlN}/\Delta v_G$ is given by the ratio between the impedance $Z_{AlN} = (jC_0\omega)^{-1}$ where C_0 is the AlN capacitance, and the total impedance $Z_{total} = Z_{AlN} + [G_i + j(C_s + C_i)\omega]^{-1}$ where C_s is the AlGaN capacitance, expressed as

$$\frac{\Delta v_{AlN}}{\Delta v_G} = \frac{Z_{AlN}}{Z_{total}} = \frac{G_i/\omega + j(C_s + C_i)}{G_i/\omega + j(C_0 + C_s + C_i)}. \tag{3.3}$$

In the DC limit $\omega \to 0$, we obtain $C_i \to q^2 D_i$ and $G_i/\omega \to 0$ as shown in Fig. 3.40, leading to the equivalent circuit shown in Fig. 3.39(right), and

$$\frac{\Delta v_{AlN}}{\Delta v_G} \to \frac{\Delta V_{AlN}}{\Delta V_G} = \frac{C_s + q^2 D_i}{C_0 + C_s + q^2 D_i} = 1 - \xi \tag{3.4}$$

or

$$\xi = \frac{C_0}{C_0 + C_s + q^2 D_i}. \tag{3.5}$$

Using the designed values of AlN capacitance $C_0 \simeq 610$ nF/cm^2 and AlGaN capacitance $C_s \simeq 325$ nF/cm^2 (by separate experiments, it is confirmed that frequency dependence of them is insignificant), gate-control efficiency $\xi \simeq 0.65$ is obtained in the ideal limit of

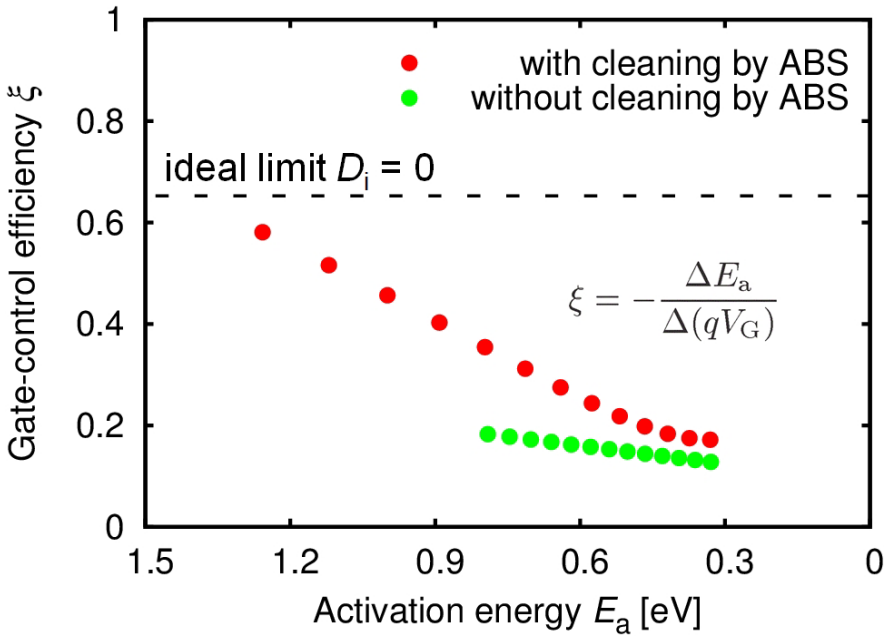

FIG. 3.38 (Process comparison) Gate-control efficiencies $\xi = -\Delta E_a/\Delta(qV_G)$ as functions of E_a.

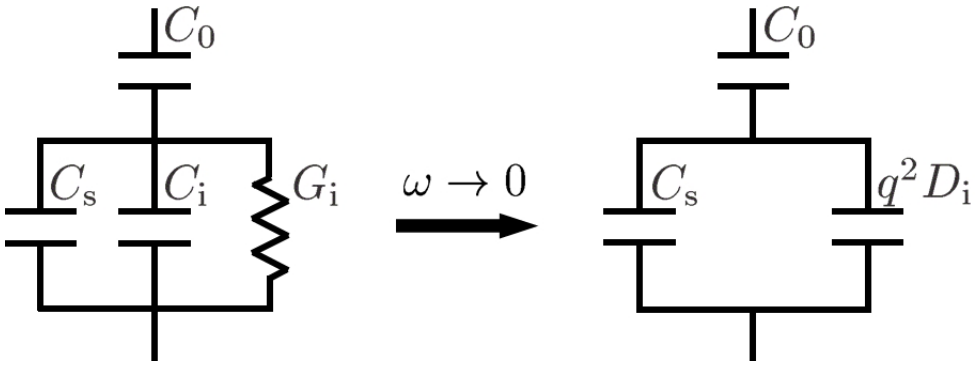

FIG. 3.39 Equivalent circuit of the MIS capacitor in AC and DC limit.

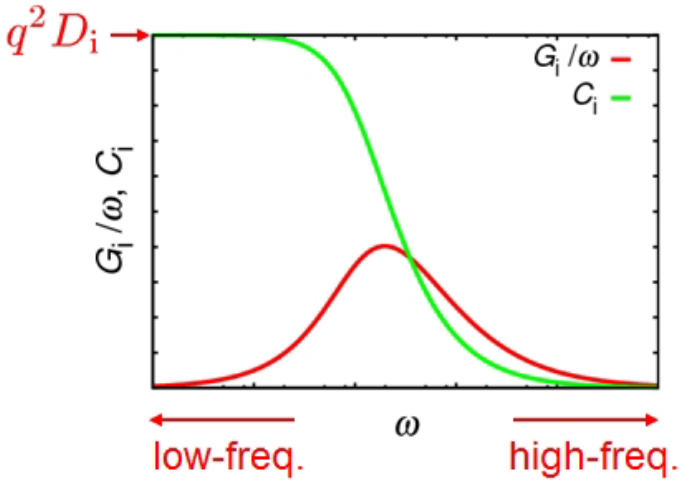

FIG. 3.40 Numerical calculation result of G_i/ω and C_i as a function of frequency.

$D_{\rm i} = 0$, as indicated by the broken line in Fig. 3.38. However, in reality, ξ is smaller than the ideal value $\simeq 0.65$ as shown in Fig. 3.38 owing to the non-zero $D_{\rm i}$. Figure 3.41 shows the calculated ξ as a function of $D_{\rm i}$ using Eq. (3.5). From the experimentally obtained gate-control efficiencies ξ in Fig. 3.38, we can evaluate the interface state densities $D_{\rm i}$ as shown in Fig. 3.42. We obtain $D_{\rm i} \sim 10^{12}$-10^{13} cm^{-2}eV^{-1} and $\gtrsim 10^{13}$ cm^{-2}eV^{-1} for the devices with and without cleaning by ABS, respectively, for interface state energy levels $\lesssim$ 1 eV below the AlGaN conduction band edge. While the conductance method was available only for interface state energy levels $\lesssim$ 0.4 eV below the AlGaN conduction band edge [30], the C-f-T mapping method enables us to analyze deeper interface states in wide-bandgap MIS devices. Although the obtained $D_{\rm i}$ for $\lesssim$ 0.4 eV below the AlGaN conduction band edge is smaller than that by the conductance method, we suppose an overestimation by the conductance method with a leakage conductance. Since the real part of the admittance of the equivalent circuit is modified by the leakage conductance [78], the result of the conductance method, which mainly utilizes the real part, is significantly influenced, whereas the present method based on the imaginary part has immunity to the influence.

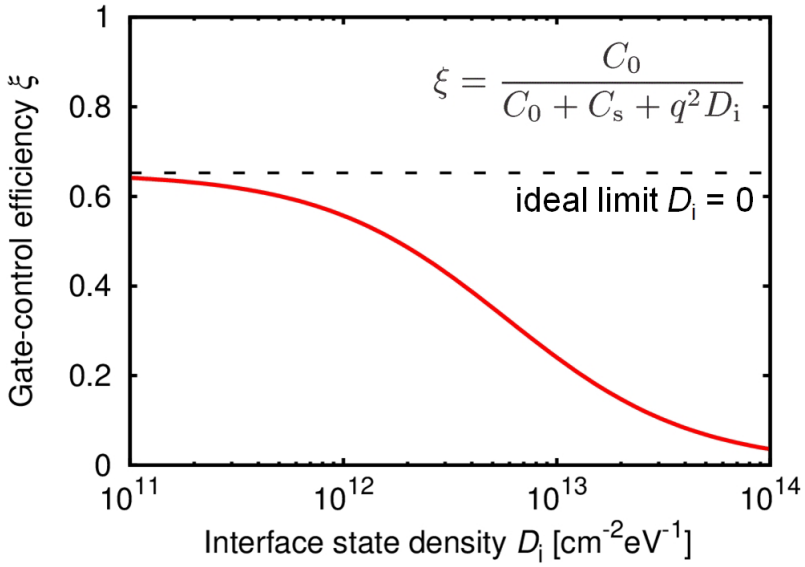

FIG. 3.41 Numerical calculation result of gate-control efficiency as a function of frequency.

As shown in Fig. 3.42, the interface state densities increase with the decrease in $E_{\rm a}$, corresponding to the shallower interface state energy levels near the AlGaN conduction band edge. According to this, the gate-control efficiencies in Fig. 3.38 decrease with decrease in $E_{\rm a}$, owing to the high-density interface states. The device with cleaning by ABS exhibits a better gate-control efficiency and a lower interface state density than the device without the cleaning; the cleaning is effective for reduction of the interface state density and improvement of the gate-control efficiency.

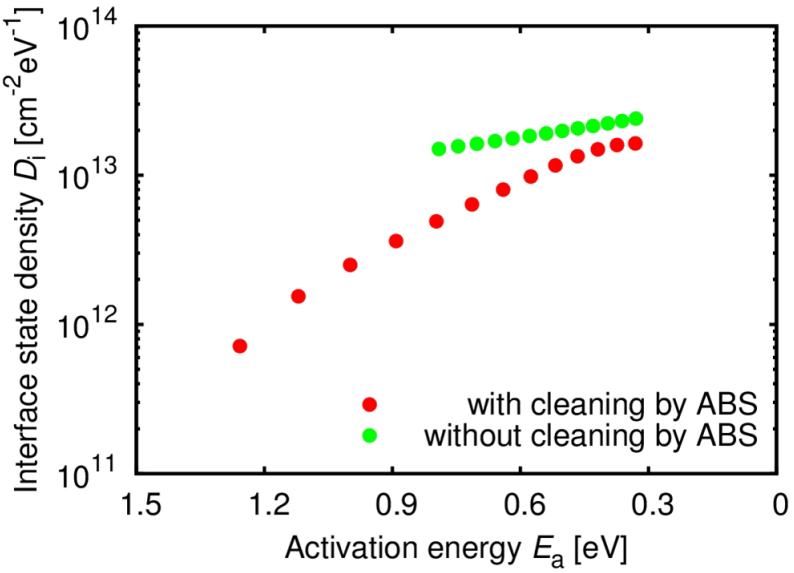

FIG. 3.42 (Process comparison) Interface state densities $D_{\rm i}$ as functions of $E_{\rm a}$.

3.4.2 Relations with intrinsic transconductance

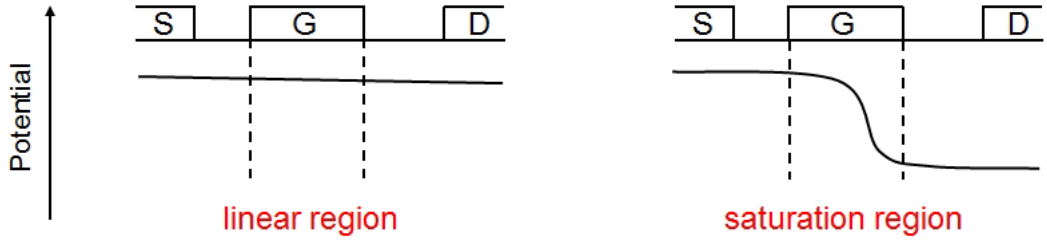

FIG. 3.43 Potential conditions in linear and saturation regions.

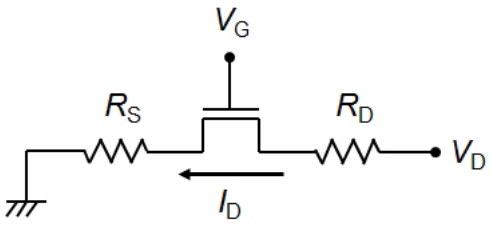

FIG. 3.44 Illustration of extrinsic resistances in a transistor.

We consider transconductances of the AlN/AlGaN/GaN MIS transistors in relation with the gate-control efficiencies and the interface state densities. We focus on the linear-region transconductances of the MIS transistors because the gate-control efficiencies and the interface state densities are obtained from the MIS capacitors, whose electric potential conditions are close to those in the linear region of the MIS transistors as shown in Fig. 3.43. Moreover, it is necessary to investigate the intrinsic transconductances of the MIS transistors excluding the effects of source resistance R_S and drain resistance R_D. As illustrated in Fig. 3.44, with the source grounded, we define the intrinsic gate voltage $V_{G0} = V_G - R_S I_D$ and the intrinsic drain voltage $V_{D0} = V_D - (R_S + R_D) I_D$, where I_D is the drain current and V_D is the drain voltage. We show linear-region I_D-V_D characteristics of the MIS transistors in Fig. 3.45. Figure 3.46 shows $\partial I_D / \partial V_{D0}$ as functions of V_{G0} in the linear region of the MIS transistors. In Fig. 3.47, we plot

$$\Gamma = \frac{\partial^2 I_D}{\partial V_{D0} \partial V_{G0}} = \frac{\partial g_{m0}}{\partial V_{D0}} \tag{3.6}$$

depending on V_{G0}, as an indicator of the linear-region intrinsic transconductance g_{m0}. The device with cleaning by ABS exhibits a lower peak Γ than the device without the cleaning, owing to the larger sputtering damage, which reduces the electron mobility and sheet electron concentration, leading to the large sheet resistance. The shallower threshold voltage for the device with cleaning by ABS is also attributed to the larger damage. However, for the forward biases, the device with cleaning by ABS exhibits higher Γ, owing to the better gate-control efficiency and the lower interface state density.

Regarding V_{G0} as the gate voltage in Fig. 3.36, we obtain Γ as functions of E_a for the MIS transistors with and without cleaning by ABS, as shown in Fig. 3.48. We find that the intrinsic transconductances decrease with the decrease in E_a, owing to the high-density interface states near the AlGaN conduction band edge. The device with cleaning

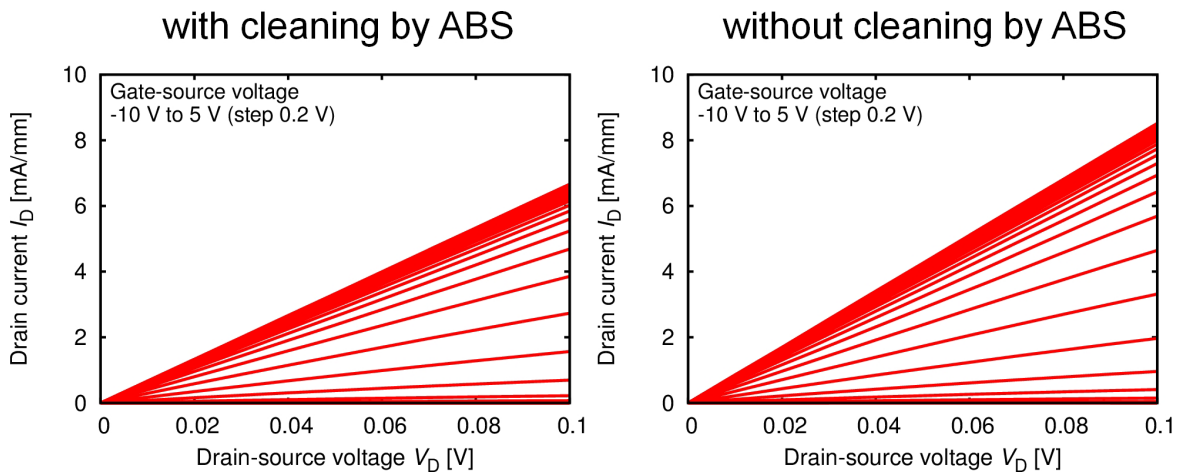

FIG. 3.45 (Process comparison) Linear-region I_D-V_D characteristics of the MIS transistors.

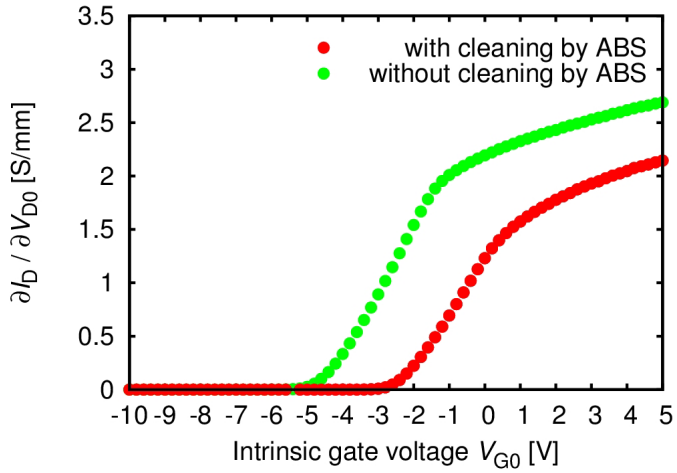

FIG. 3.46 (Process comparison) Linear-region $\partial I_D/\partial V_{D0}$ as functions of V_{G0}.

by ABS exhibits a larger Γ than the device without the cleaning; the cleaning is effective for improvement of the intrinsic transconductance. The behaviors of the intrinsic transconductances in Fig. 3.48 have a close resemblance to those of the gate-control efficiencies ξ in Fig. 3.38. From the E_a-dependence of ξ and Γ, we obtain the correlation shown in Fig. 3.49; the intrinsic transconductances increase as the gate-control efficiencies increase. For the low-Γ (low-ξ) regime, a linear relation between Γ and ξ is obtained by fitting, as shown by the solid line in Fig. 3.49. Assuming a constant mobility μ, from its definition of Eq. (3.6), Γ is given by

$$\Gamma = \frac{\mu}{L_G}\frac{\partial(qn_s)}{\partial V_{G0}} = \frac{\mu}{L_G}\frac{C_s C_0}{C_0 + C_s + q^2 D_i} = \frac{\mu}{L_G} C_s \xi, \tag{3.7}$$

where L_G is the gate length. From this and the linear relation between Γ and ξ obtained by the fitting, we extract the mobility $\mu \sim 580$ cm^2/V-s using the values of C_{AlGaN} and L_G. Applying this mobility, we can reproduce the relation between Γ and ξ for low-Γ regime as shown in Fig. 3.50. This mobility is lower than $\mu \sim 1000$ cm^2/V-s obtained by the Hall-effect measurements after the AlN deposition, owing to significant AlGaN-GaN interface roughness scattering [79] at high sheet electron concentrations corresponding to

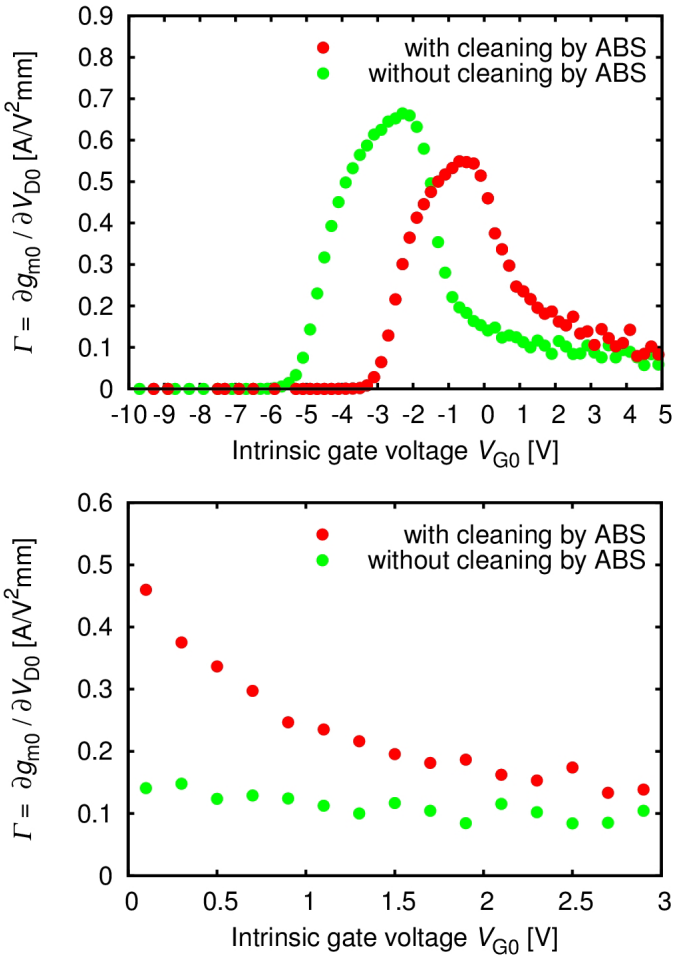

FIG. 3.47 (Process comparison) η as an indicator of the linear-region intrinsic transconductance g_{m0}.

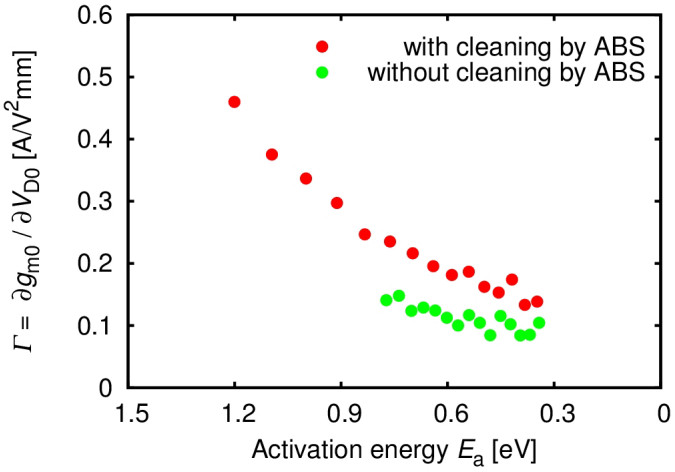

FIG. 3.48 (Process comparison) η as functions of activation energy for the MIS transistors.

forward gate biases. Moreover, the intrinsic transconductances are correlated with the interface state densities D_{i} in Fig. 3.42; from the E_{a}-dependence of Γ and D_{i}, we obtain the correlation shown in Fig. 3.51, where the intrinsic transconductances decrease with increase in the interface state densities.

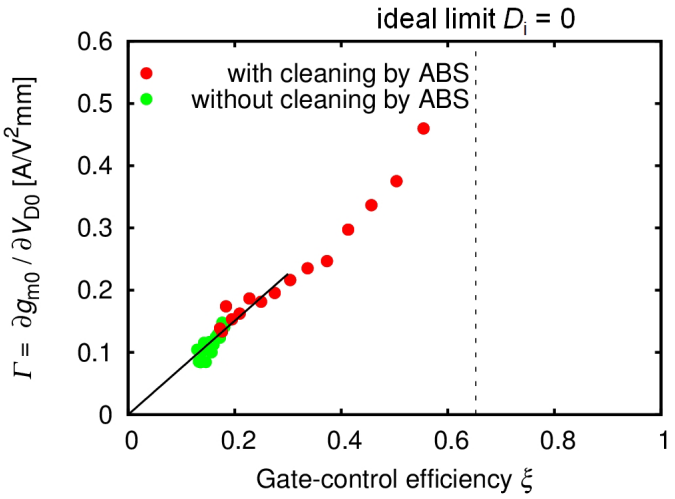

FIG. 3.49 The relation between the gate-control efficiencies ξ and the linear-region intrinsic transconductances g_{m0}.

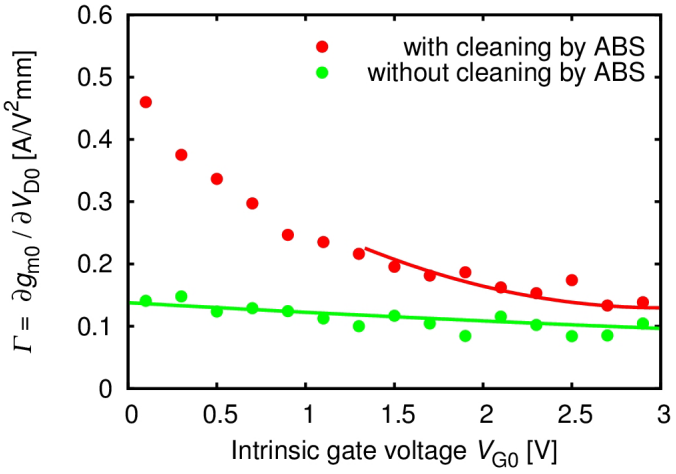

FIG. 3.50 η reproduced from ξ using the extracted mobility.

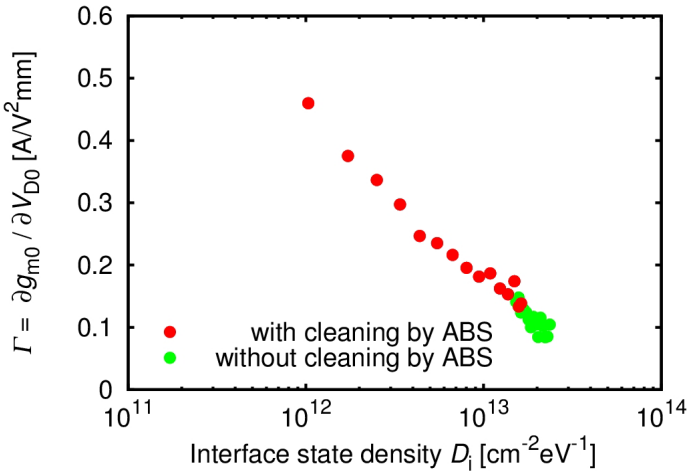

FIG. 3.51 The relation between the interface state density D_i and the linear-region intrinsic transconductances g_{m0}.

3.4.3 Relations with X-ray photoelectron spectroscopy analysis

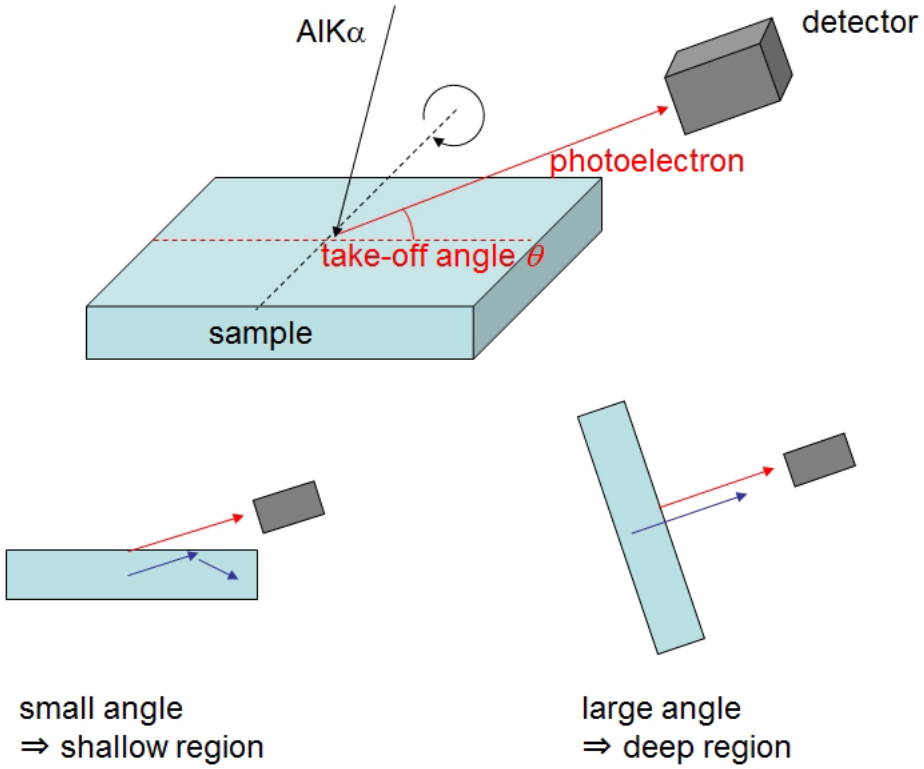

FIG. 3.52 Illustration of the XPS measurement.

We employed XPS measurements illustrated in Fig. 3.52 to analyze the AlN-AlGaN interfaces. To investigate the origin of the properties depending on the AlN-AlGaN interface formation processes, revealed by the above analysis, we employed four samples illustrated in the insets of Fig. 3.53, for XPS characterization of the AlGaN surfaces and the AlN-AlGaN interfaces. The four samples were prepared according to the device fabrication processes. Samples (a) (AlGaN with ABS) and (b) (AlGaN without ABS) are the AlGaN/GaN heterostructures treated by organic cleaning with and without the additional cleaning by ABS for the AlGaN surfaces, respectively. Samples (c) (AlN/AlGaN with ABS) and (d) (AlN/AlGaN without ABS) are obtained by AlN $\sim$ 1 nm deposition on the AlGaN surfaces treated by the processes of samples (a) and (b), respectively. The samples (a) and (b) are for investigation of the AlGaN surfaces with different treatments. On the other hand, the samples (c) and (d) are for investigation of the AlN-AlGaN interfaces formed by the AlN deposition on the AlGaN surfaces with different treatments, their XPS spectra including information of not only the AlN surfaces but also the AlN-AlGaN interfaces owing to the thin AlN. All samples were introduced to the XPS chamber within 20 min after they were prepared, followed by XPS measurements using take-off angles $\theta = 25$-$75°$. Figure 3.53 shows Ga3d, N2s, and O2s peaks measured at $\theta = 35°$. The O2s peak intensities increase for the samples (c) and (d) compared to those for the samples (a) and (b), respectively, owing to natural oxidation of the AlN. The Ga3d peaks are decomposed into the Ga-O and Ga-N bondings. We obtain the ratio of the integrated

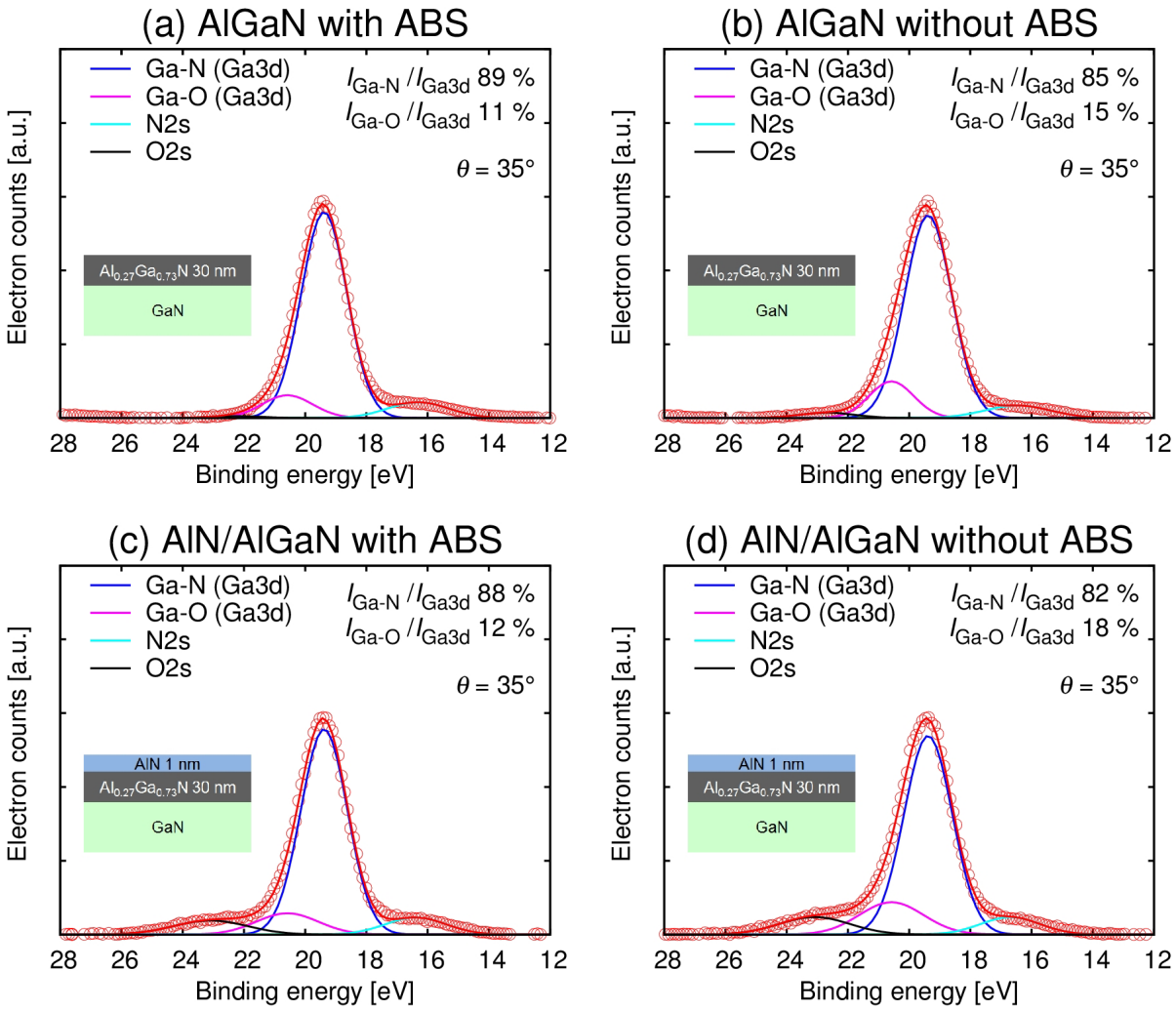

FIG. 3.53 Ga3d, N2s, and O2s peaks measured at a take-off angle $\theta = 35°$ for the samples (a) AlGaN with ABS, (b) AlGaN without ABS, (c) AlN/AlGaN with ABS, and (d) AlN/AlGaN without ABS, where $I_{\text{Ga-O}}/I_{\text{Ga3d}}$ ($I_{\text{Ga-N}}/I_{\text{Ga3d}}$) is the ratio of the integrated peak intensity of Ga-O (Ga-N) bonding component to that of the total Ga3d peak. Insets: illustration of the samples for XPS characterization.

peak intensity of the Ga-O (Ga-N) bonding component to that of the total Ga3d peak, $I_{\text{Ga-O}}/I_{\text{Ga3d}}$ ($I_{\text{Ga-N}}/I_{\text{Ga3d}}$). Although the Ga-N bonding components dominate the Ga3d peaks, we can observe differences in $I_{\text{Ga-O}}/I_{\text{Ga3d}}$ depending on the treatments; the samples (a) and (c) exhibit smaller $I_{\text{Ga-O}}/I_{\text{Ga3d}} \simeq$ 11-12 %, than $I_{\text{Ga-O}}/I_{\text{Ga3d}} \simeq$ 15-18 % of the samples (b) and (d). In Fig. 3.54, we show $I_{\text{Ga-O}}/I_{\text{Ga3d}}$ for other take-off angles also exhibiting smaller values for the samples (a) and (c) than for the samples (b) and (d), respectively. The AlGaN surface cleaning by ABS before the AlN deposition removes the initial oxide layer, leading to less Ga-O bonding and the lower interface state density, giving the better gate-control efficiency and the higher intrinsic transconductance of the MIS devices. These results indicate that, Ga-O bonding plays an important role in the AlN-AlGaN interfaces, similarly to the importance of Ga-O bonding in Al_2O_3-AlGaN interfaces [80].

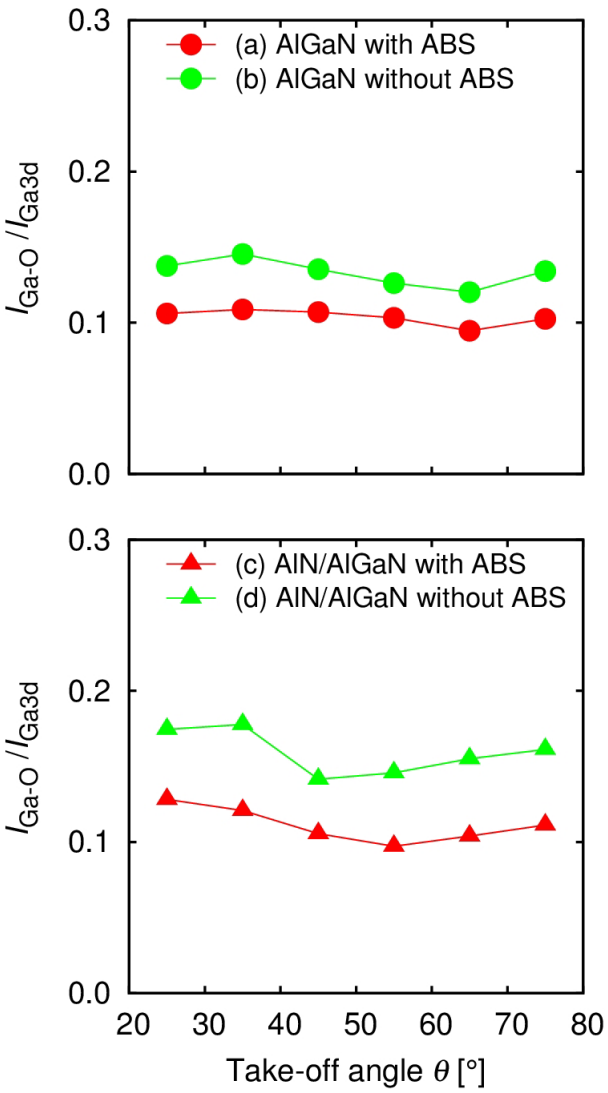

FIG. 3.54 $I_{\text{Ga-O}}/I_{\text{Ga3d}}$ and $I_{\text{Ga-N}}/I_{\text{Ga3d}}$ at θ = 25-75° for the samples (a) AlGaN with ABS, (b) AlGaN without ABS, (c) AlN/AlGaN with ABS, and (d) AlN/AlGaN without ABS.

Chapter 4

Conclusion and future perspective

4.1 Conclusion

In this work, we proposed and developed a method using C-f-T mapping obtained from the temperature-dependent C-V-f characteristics for GaN-based MIS devices, based on the Lehovec equivalent circuit. From constant-capacitance contours, exhibiting a straight line behavior in the mapping, an activation energy E_{a} corresponding to an interface state energy level can be extracted for a wide range of gate biases without assuming any parameter. The gate bias dependence of the activation energies leads to many insights into the MIS devices. The effectiveness of the method was exemplified by application to AlN/AlGaN/GaN MIS devices. Through characterizing the activation energies modulated by the gate biases, we can obtain the gate-control efficiency of the MIS devices, i.e., the ratio of the bandbending change in the semiconductor to the total gate voltage change. Even though the Lehovec equivalent circuit is based on an AC small-signal model, we find that its DC limit, described by the insulator capacitance, the semiconductor capacitance, and the interface state density, gives the gate-control efficiency. Therefore, we can evaluate the interface state density from the experimentally obtained gate-control efficiency, using the values of insulator and semiconductor capacitances. From the activation energies corresponding to a wide range of gate biases, we can obtain the gate-control efficiency and the interface state density corresponding to deep interface states in comparison with the conductance method. Moreover, it is shown that the gate-control efficiency and the interface state density have correlations with the linear-region intrinsic transconductance. In addition, we give characterization of the AlN-AlGaN interfaces by using X-ray photoelectron spectroscopy, in relation with the results of the analysis. The C-f-T mapping method is useful and important for developments of MIS devices, based on not only wide-gap GaN-related semiconductors, but also other wide-gap semiconductors.

4.2 Future perspective

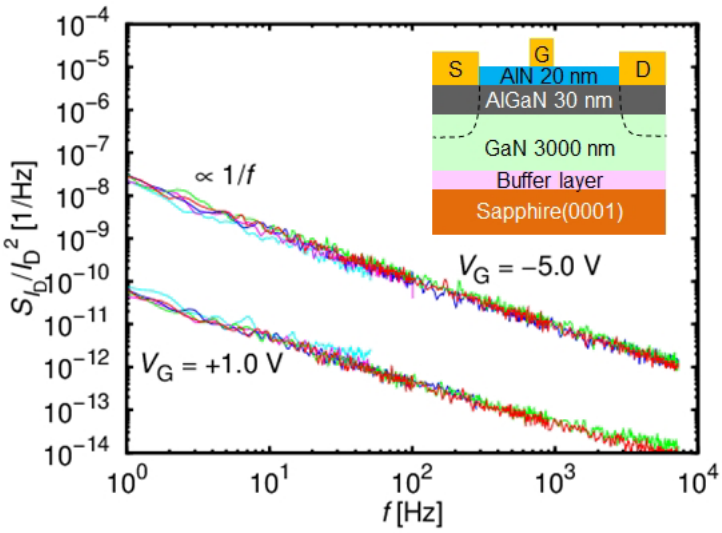

FIG. 4.1 Drain current power spectrum density $S_{I_D}/{I_D}^2$ as functions of f for AlN/AlGaN/GaN MIS devices [31].

We have investigated low frequency noise (LFN) of the AlN/AlGaN/GaN MIS devices shown in the inset of Fig. 4.1 [31]. The LFN exhibits the $1/f$ behavior without bumps or peaks corresponding to the trapping time constants, as shown in Fig. 4.1. We need deeper insights into the relation between the LFN and interface states.

Appendix A Algorithm of obtaining contours in C-f-T mapping

The algorithm of obtaining contours in C-f-T mapping is explained below using a set of artificial data.

Contour points within a mapping

As shown in the left of Fig. 4.2, we have 1/X in horizontal axis, Y in vertical axis, and Z in lateral axis, each corresponds to the reverse temperature, frequency, and measured capacitance in C-f-T mapping, respectively. The red points indicate data points while the blue points do the contours points of Z=20. The mapping of the artificial data with a contour of Z=20 is shown in the right of Fig. 4.2.

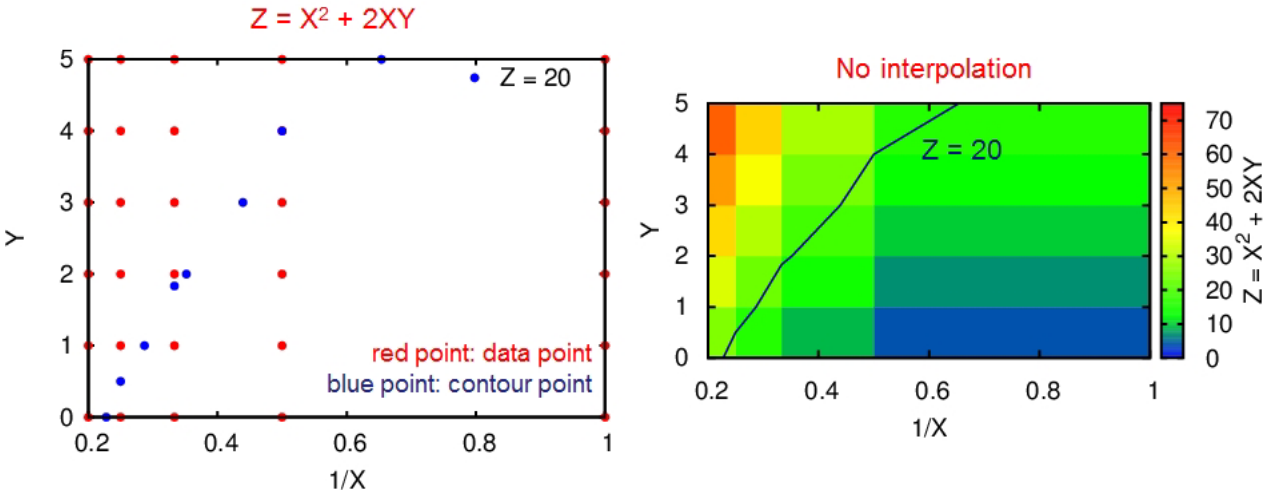

FIG. 4.2 Contour points (left) and a mapping of the data (right).

Algorithm of obtaining contour points

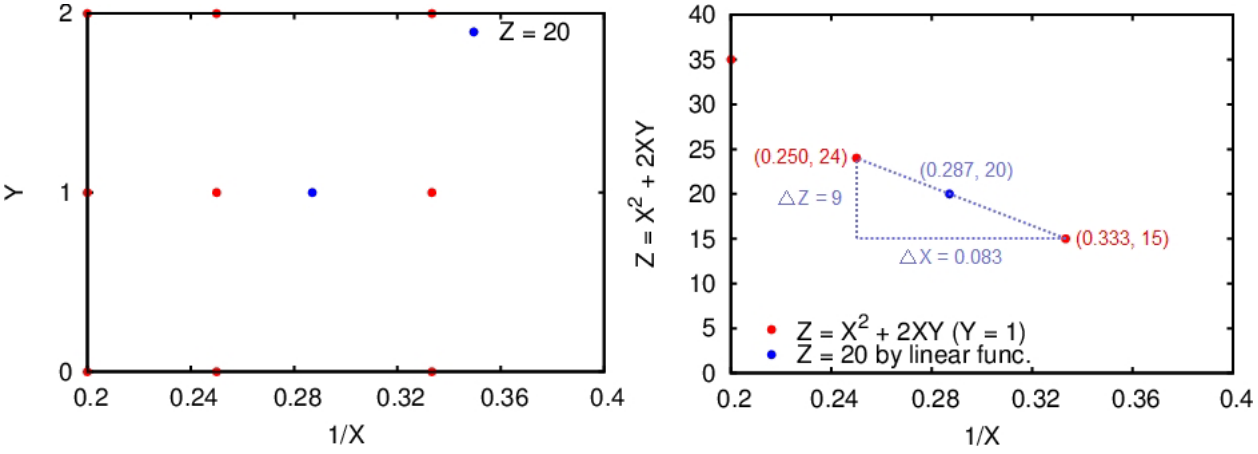

FIG. 4.3 A contour point between two data points (left) and its evaluation through a cross-section view at Y=1 (right).

We first look into a point with parameters $0.24 < 1/X < 0.32$, Y=1, and Z=20, as shown in the blue point in the left of Fig. 4.3. Taking a cross-section view across Y=1, we show Z-value as a function of 1/X, as shown in the right of Fig. 4.3.

The algorithm to obtain contour points: 1. search for two data points with values closest to the designated Z-value, then 2. connect the two data points using a linear function and calculate the 1/X at designated Z-value. However, by definition of function Z, Z=19.1 when 1/X=0.287, Y=1, being different from the designated Z-value of 20. This discrepancy is from the non-linear behavior of the Z-value as shown in Fig. 4.4. If the step between the two data points are large and the non-linear behavior of Z-value is significant, the described algorithm to obtain contour points is not accurate. We should examine the experimental data to confirm whether such discrepancy exists in our analysis.

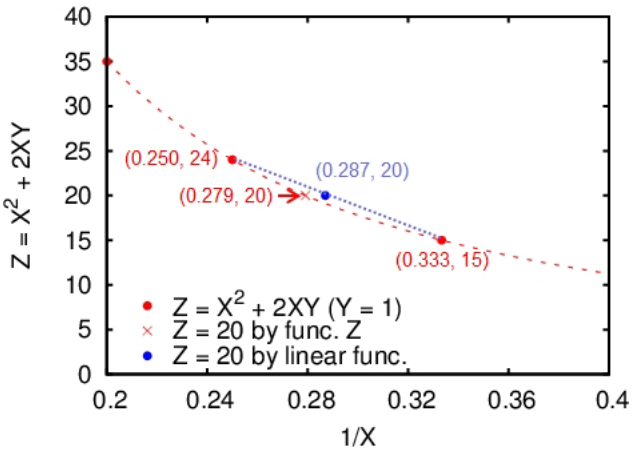

FIG. 4.4 Origin of discrepancy due to the non-linear behavior of Z-value.

As indicated in Fig. 4.5, the capacitances, corresponding to Z-value, exhibiting linear behavior in between 300-600 nF/cm2, and higher temperature regime, which have close data points, are employed. Therefore, we do not expect discrepancy in obtaining contour points using the described algorithm on the experimental data.

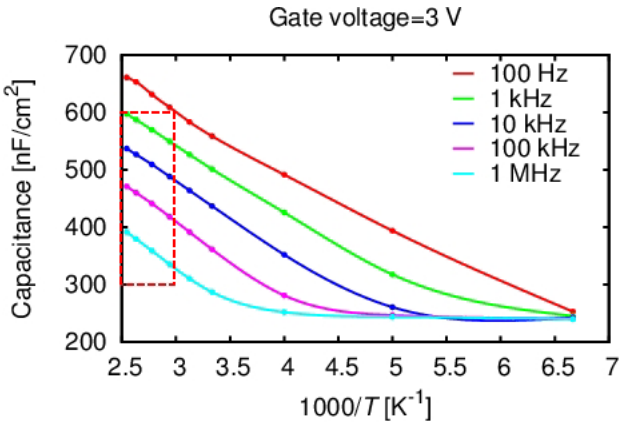

FIG. 4.5 Experimental data showing linear behavior of capacitance and higher temperature regime with close data points.

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- Hong-An Shih, Masahiro Kudo, Masashi Akabori, and Toshi-kazu Suzuki, "Application of Sputtering-Deposited AlN Films to Gate Dielectric for AlGaN/GaN Metal-Insulator-Semiconductor Heterojunction Field-Effect Transistor" Japanese Journal of Applied Physics, **51**, 02BF01 (2012).
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