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Description	

Improvement in passivation quality and open-circuit voltage in silicon heterojunction solar cells by the catalytic doping of phosphorus atoms

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Abstract

We apply phosphorus (P) doping to amorphous silicon (a-Si)/crystalline silicon (c-Si) heterojunction solar cells realized by exposing c-Si to P-related radicals generated by the catalytic cracking of PH₃ molecules (Cat-doping). An ultrathin n⁺-layer formed by P Cat-doping acts to improve the effective minority carrier lifetime (τ_{eff}) and implied open-circuit voltage (implied V_{oc}) owing to its field effect by which minority holes are sent back from an a-Si/c-Si interface. An a-Si/c-Si heterojunction solar cell with a P Cat-doped layer shows better solar cell performance, particularly in V_{oc} , than the cell without P Cat-doping. This result demonstrates the feasibility of applying Cat-doping to a-Si/c-Si heterojunction solar cells, owing to the advantage of the low-temperature (<200 °C) process of Cat-doping.

1. Introduction

The technology of using thin crystalline silicon (c-Si) wafers has become increasingly important owing to the growing photovoltaic market and resulting requirement for cost reduction.¹⁾ Thinner crystalline silicon needs more effective surface passivation layers because of the greater influence of the surface recombination of minority carriers. Amorphous Si (a-Si)/c-Si heterojunction solar cells have been expected as one of the most appropriate cell concepts for thin c-Si wafers.²⁻¹⁶⁾ This is because of their advantages of a symmetric structure, which prevents the bowing of Si wafers, and high-quality passivation realized by using intrinsic a-Si films. There has been a report of the fabrication of an a-Si/c-Si heterojunction solar cell with an outstanding open-circuit voltage (V_{oc}) of 750 mV.²⁾ The formation of a doping layer on a c-Si surface is another way of reducing the surface recombination velocity (SRV) of minority carriers other than by depositing high-quality passivation layers. Doping processes, however, generally require high temperatures such as >800 °C and are thus believed to be incompatible with the a-Si/c-Si heterojunction solar cells containing a-Si films with low thermal tolerance.

We have recently demonstrated that an ultrathin (<5 nm) phosphorus- (P-) doped layer can be formed on a c-Si surface by exposing c-Si to P-related radicals generated by decomposing PH_3 molecules on a heated catalyzing wire.¹⁷⁻²³⁾ This novel doping technique, referred to as “Cat-doping”, can be performed at significantly low substrate temperatures of less than 200 °C, and is thus applicable to the fabrication of a-Si/c-Si heterojunction solar cells. We have already confirmed the effectiveness of P Cat-doping in reducing the SRV of minority carriers on n-type c-Si wafers.^{17, 18, 21-23)} In this study, we attempt to apply P Cat-doping to actual a-Si/c-Si heterojunction solar

cells. A solar cell prepared with P Cat-doping shows better V_{oc} than a cell without P Cat-doping, indicating the applicability of Cat-doping to actual solar cell devices.

2. Experimental procedure

We used (100)-oriented, mirror-polished n-type c-Si wafers with a resistivity of 1–5 Ωcm , a thickness of 290 μm , and a bulk minority carrier lifetime (τ_b) of >10 ms. The c-Si wafers were first cleaved to 20×20 mm^2 -sized pieces. We dipped them into H_2O -diluted 5% hydrofluoric (HF) acid in order to remove native oxide. The samples were immersed in H_2O -diluted 3% hydrogen peroxide (H_2O_2) for 30 s to form ultrathin silicon oxide (SiO_x) layers to prevent the epitaxial growth of Si during a-Si deposition, the details of which will be independently reported in the near future. We then introduced the wafers into a Cat-CVD chamber, and performed P Cat-doping into the wafers using a heated tungsten (W) catalyzing wire under the conditions summarized in Table I. A 10-nm-thick intrinsic a-Si (i-a-Si) capping layer was deposited by Cat-CVD on the P Cat-doped c-Si surface to prepare samples for sheet carrier concentration measurement. Four aluminum (Al) electrodes were evaporated through a hard mask on the a-Si film to form the van der Pauw configuration of 8×8 mm^2 -sized Hall elements. The details of the sample structure and the Hall effect measurement have been summarized elsewhere.²⁰⁾ Note that p-type c-Si wafers with a resistivity of 2900 Ωcm were used only when we performed Hall effect measurement.

In order to prepare samples for the measurement of effective minority carrier lifetime (τ_{eff}) and implied V_{oc} , P Cat-doping was performed on both sides of c-Si wafers, and we then deposited 10-nm-thick i-a-Si and 6-nm-thick n-type a-Si (n^+ -a-Si) stacked films. The minority carrier lifetime and implied V_{oc} of the samples were characterized

using microwave photoconductivity decay (μ -PCD) and quasi-steady-state photoconductance (QSSPC), respectively.^{24,25)} A pulse laser with a wavelength of 904 nm and a photon density of 5×10^{13} /cm² was used for the generation of the excess carriers for the μ -PCD measurement. τ_{eff} was measured in a position-dependent mapping mode, and τ_{eff} shown below are the maximum values in the 20×20 mm² area mapping. QSSPC measurement was carried out in the transient mode. Figure 1 shows the schematic of the sample for τ_{eff} measurement. Postannealing was performed for the structures in air at 200 °C for 30 min, which is because the a-Si/c-Si heterojunction cells also underwent postannealing to improve the conductivity of silver (Ag) electrodes, as mentioned below. The postannealing also improves the interface property and reduce the SRV.

For the characterization of solar cell performance, we performed P Cat-doping on one side and the films of the other side were replaced with 15-nm-thick i-a-Si and 7-nm-thick p-type a-Si (p⁺-a-Si) stacked films. We then deposited 80-nm-thick indium tin oxide (ITO) films on both sides of the samples by sputtering at a substrate temperature of 100 °C, using an ITO target with an tin dioxide (SnO₂) concentration of 5%. We formed comb-shaped electrodes by screen printing and successive annealing at 200 °C on the front and back of the ITO films. The schematic of the solar cell structure is shown in Fig. 2. The deposition conditions of the a-Si films are summarized in Table I. For comparison with these cells, we also prepared cells without P Cat-doping into c-Si wafers. The performance of the solar cells was characterized by current-voltage (J-V) measurement under the 1-sun (AM1.5, 100 mW/cm²) condition, by external quantum efficiency (EQE) measurement, and by Suns-V_{oc}.²⁶⁾ Note that we used c-Si wafers with no alkali texturing and the absolute

values of short-circuit current (J_{sc}) are not sufficiently large owing to unsuppressed optical reflection.

3. Results and discussion

Figures 3 and 4 show τ_{eff} and implied V_{oc} of the structures shown in Fig. 1 with and without P Cat-doping as a function of catalyzer temperature (T_{cat}) during P Cat-doping. One can clearly see that τ_{eff} is effectively improved by the postannealing. The improvement in τ_{eff} of i-a-Si-passivated c-Si wafers by postannealing has also been reported elsewhere,²⁷⁾ and its mechanism can be understood to be the reduction in the number of Si dangling bonds by hydrogen termination. A similar effect may also occur in our samples. The maximum τ_{eff} of 2.4 ms corresponds to an SRV of ~ 6 cm/s, which is estimated using the equation $(\tau_{eff})^{-1} = (\tau_b)^{-1} + 2S_{eff}/w$, where S_{eff} and w represent SRV and wafer thickness, respectively, and assuming $\tau_b = \infty$. Implied V_{oc} also shows an outstanding value of >0.70 V at a T_{cat} of 900 °C after postannealing. Another idea we can confirm from Fig. 1 is that P Cat-doping is effective in improving τ_{eff} and implied V_{oc} , as has been reported previously.^{17, 18, 21-23)} When focusing on the T_{cat} dependence of τ_{eff} and implied V_{oc} , τ_{eff} and implied V_{oc} show maximum values at T_{cat} of around 900 °C.

A possible explanation of the lower τ_{eff} and implied V_{oc} at lower T_{cat} is insufficient P doping. To confirm this, we investigated the T_{cat} dependence of sheet carrier concentration. Figure 5 shows the sheet carrier concentration of P Cat-doped c-Si samples as a function of T_{cat} . P atoms are not effectively doped at T_{cat} of <900 °C probably because of the insufficient decomposition of PH_3 molecules on the heated W catalyzer since the decomposition rate of PH_3 molecules strongly depends on T_{cat} .^{28, 29)}

On the other hand, sheet carrier concentrations on the order of $10^{12} / \text{cm}^3$ have a weak dependence on T_{cat} at $T_{\text{cat}} \geq 900$ °C. Sheet carrier density increases upon postannealing, meaning that P atoms adsorbed on a c-Si surface are additionally activated during postannealing. Annealing at 200 °C seems to be insufficient to activate P atoms in c-Si. The reasonable likely explanation of P activation at such a low temperature is that some P atoms in the Cat-doped layer are originally inactivated by hydrogen atoms and these hydrogen atoms are released from the P atoms during postannealing. This tendency is contrary to the results shown in our previous report,²²⁾ which might be related to the difference in the annealing temperature. It should be noted that the samples with P Cat-doping at T_{cat} of < 900 °C have higher τ_{eff} and implied V_{oc} than the untreated sample even without sufficient P doping, as shown in Figs. 3–5. This can be explained by the effect of atomic hydrogen exposure to c-Si surfaces. Atomic hydrogen can be formed through the catalytic decomposition of PH_3 on W following the reaction $\text{PH}_3 \rightarrow \text{P} + 3\text{H}$.^{28,}
²⁹⁾ The hydrogen atoms adhered on the c-Si surface may form Si-H bonds and act to decrease the number of Si dangling bonds. This effect has been confirmed in our previous work.¹⁷⁾

Because of a weak dependence of sheet carrier density on T_{cat} , there must be other reasons for the lower τ_{eff} and implied V_{oc} at high T_{cat} . The most likely reason is the enhanced etching of the c-Si surface by more effectively generated atomic hydrogen.^{17, 22)} A c-Si surface roughened by atomic hydrogen may result in worse a-Si/c-Si interface quality. We have actually observed more roughened c-Si surfaces after P Cat-doping at higher T_{cat} .¹⁹⁾

According to the above experimental results, we chose T_{cat} of 900 °C for the formation of a P Cat-doping layer in the actual solar cell fabrication process. We also

carried out the measurement of τ_{eff} and implied V_{oc} for p-a-Si/i-a-Si/c-Si/i-a-Si/n-a-Si structures. τ_{eff} was improved from ~ 500 to ~ 1100 μs , and implied V_{oc} was also effectively increased from 0.684 to 0.697 V by introducing P Cat-doping. Figure 6 shows the EQE spectra of a-Si/c-Si heterojunction solar cells with and without P Cat-doping. There seems to be no significant difference between the two EQE spectra. A highly doped layer can generally enhance Auger recombination owing to the large number of majority carriers. A P-doped layer formed by Cat-doping is, however, extremely thin, as mentioned above. The effect of Auger recombination is thus negligible, and we see no reduction in EQE upon introducing a P Cat-doped layer. Figure 7 shows the J-V characteristics of the heterojunction solar cells with and without P Cat-doping. J_{sc} , V_{oc} , fill factor (FF), and conversion efficiency η obtained from the J-V characteristics are summarized in Table II. One can clearly confirm an increase in V_{oc} upon introducing P Cat-doping. This finding is consistent with the results in Figs. 3 and 4 showing an improvement in the passivation quality. V_{oc} values lower than implied V_{oc} may be due to plasma damage of a-Si/c-Si interfaces during ITO sputtering and to the resulting deterioration of passivation quality. FF of <0.7 obtained from the J-V characteristics is much smaller than the pseudo-FF (pFF) of >0.77 . Since pFF is not affected by series resistance, the large difference between FF and pFF results from the high series resistance. Unoptimized ITO sputtering conditions and/or Ag electrode formation process may be part of the reason behind the high series resistance.

It should also be noted that FF is slightly improved upon introducing P Cat-doping. This can be explained by the realization of smoother majority carrier flow owing to the lower energy barrier at the a-Si/c-Si interface after P Cat-doping. Figure 8 shows the simulated band diagrams of the back a-Si/c-Si interfaces in the cases of the

absence and presence of a 2-nm-thick P Cat-doped layer with a P concentration of 10^{19} / cm^3 . The band diagram simulation was carried out using software AFORS-HET version 2.4.1.³⁰⁾ According to the simulation results, the introduction of a 2-nm-thick P Cat-doping layer reduces the barrier height for majority carriers (electrons) by 88 meV. The reduction in barrier height contributes to the enhancement of backward electron flow and the resulting decrease in series resistance and slight improvement in FF.

We finally discuss the significance of P Cat-doping in the fabrication of a-Si/c-Si heterojunction solar cells. Since P Cat-doping can be performed in a Cat-CVD chamber used also for the deposition of n^+ -a-Si films, no additional equipment is necessary. Furthermore, owing to its advantage of being a low-temperature (<200 °C) process, Cat-doping is applicable even after the deposition of a-Si or silicon nitride (SiN_x) films with low thermal tolerance. This advantage is beneficial, particularly when we fabricate a-Si/c-Si heterojunction back-contact (HBC) cells, in which P Cat-doping layers can be applied on both the front and the back. A front P Cat-doped layer in a HBC cell can effectively act as a front-surface field layer.²²⁾ The introduction of P Cat-doping at the interface between n^+ /i-a-Si and c-Si will also contribute to the improvement of V_{oc} and FF of the cell, as demonstrated in this work. The HBC process with the two repetitions of P Cat-doping can be performed whether the process is started from the front or from the back, because of the low process temperature.

4. Conclusions

We have demonstrated the applicability of P Cat-doping to a-Si/c-Si heterojunction solar cells. P Cat-doping, which can be performed at a substrate temperature of <200 °C,

can be utilized for the production of a-Si/c-Si heterojunction solar cells. The introduction of a P Cat-doped layer leads to improvements in τ_{eff} and implied V_{oc} , the effect of which is also reflected in the actual increase in V_{oc} of the a-Si/c-Si heterojunction solar cell. The improvement of FF is found to be another possible effect of the introduction of a P Cat-doped layer on the solar cell performance. Cat-doping can potentially be applied to the a-Si/c-Si heterojunction or HBC solar cells because of its effectiveness in enhancing the solar cell performance and its low-temperature processability.

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Table I. Process conditions for a-Si deposition and P Cat-doping.

	Substrate temperature (°C)	Catalyzer temperature (°C)	Gas flow rate (sccm)				Pressure (Pa)
			He-diluted 2.25% PH ₃	He-diluted 2.25% B ₂ H ₆	H ₂	SiH ₄	
P Cat-doping	200	700-1300	20	-	-	-	1.5
i-a-Si	160	1800	-	-	-	10	1
n ⁺ -a-Si	200	1800	4.4	-	50	20	2
p ⁺ -a-Si	250	1800	-	8	20	10	2

Table II. Characteristics of solar cells without and with P Cat-doping.

	Without P Cat-doping		With P Cat-doping	
	J-V	Suns- V_{oc}	J-V	Suns- V_{oc}
J_{sc} (mA/cm ²)	31.3	-	31.1	-
V_{oc} (V)	0.660	0.669	0.672	0.686
FF	0.683	0.776	0.695	0.777
Efficiency (%)	14.1	-	14.5	-

Table III. Parameters adopted in band diagram analysis by using AFORS-HET.

Layer	n ⁺ -a-Si	i-a-Si	P Cat-doped layer	c-Si
Thickness (cm)	6×10^{-7}	1×10^{-6}	0 or 2×10^{-7}	2.9×10^{-2}
Effective density of state in conduction band (cm ⁻³)	1×10^{20}	1×10^{20}	2.846×10^{19}	2.846×10^{19}
Effective density of state in valence band (cm ⁻³)	1×10^{20}	1×10^{20}	2.685×10^{19}	2.685×10^{19}
Dopant concentration (cm ⁻³)	7.32×10^{19}	-	1.0×10^{19}	1.5×10^{15}
Electron affinity (eV)	3.9	3.9	4.05	4.05
Band gap (eV)	1.72	1.72	1.124	1.124
Relative permittivity	11.9	11.9	11.9	11.9

Figure captions

Figure 1 Schematic of an n^+ -a-Si/i-a-Si/P Cat-doped layer/c-Si sample for τ_{eff} and implied V_{oc} measurement.

Figure 2 Schematic of an a-Si/c-Si heterojunction solar cell with a P Cat-doped layer.

Figure 3 τ_{eff} of n^+ -a-Si/i-a-Si/c-Si samples without and with P Cat-doped layers as a function of T_{cat} .

Figure 4 Implied V_{oc} of n^+ -a-Si/i-a-Si/c-Si samples without and with P Cat-doped layers as a function of T_{cat} .

Figure 5 Sheet carrier concentration of P Cat-doped layers formed on c-Si as a function of T_{cat} .

Figure 6 EQE spectra of a-Si/c-Si heterojunction solar cells without and with a P Cat-doped layer.

Figure 7 J-V characteristics of a-Si/c-Si heterojunction solar cells without and with a P Cat-doped layer.

Figure 8 Band diagram of n^+ -a-Si/i-a-Si/c-Si heterostructures without and with a P Cat-doped layer, obtained by AFORS-HET analysis. The origins of vertical and

horizontal axes are taken to be the vacuum level and the n^+ -a-Si/ITO interface, respectively.

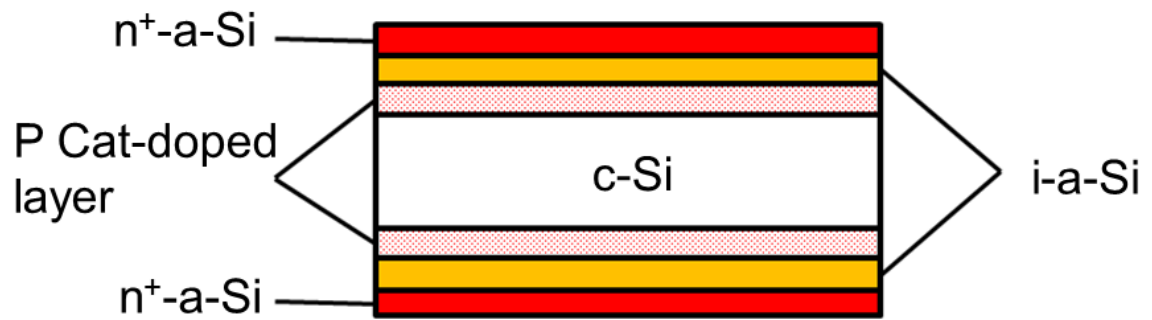


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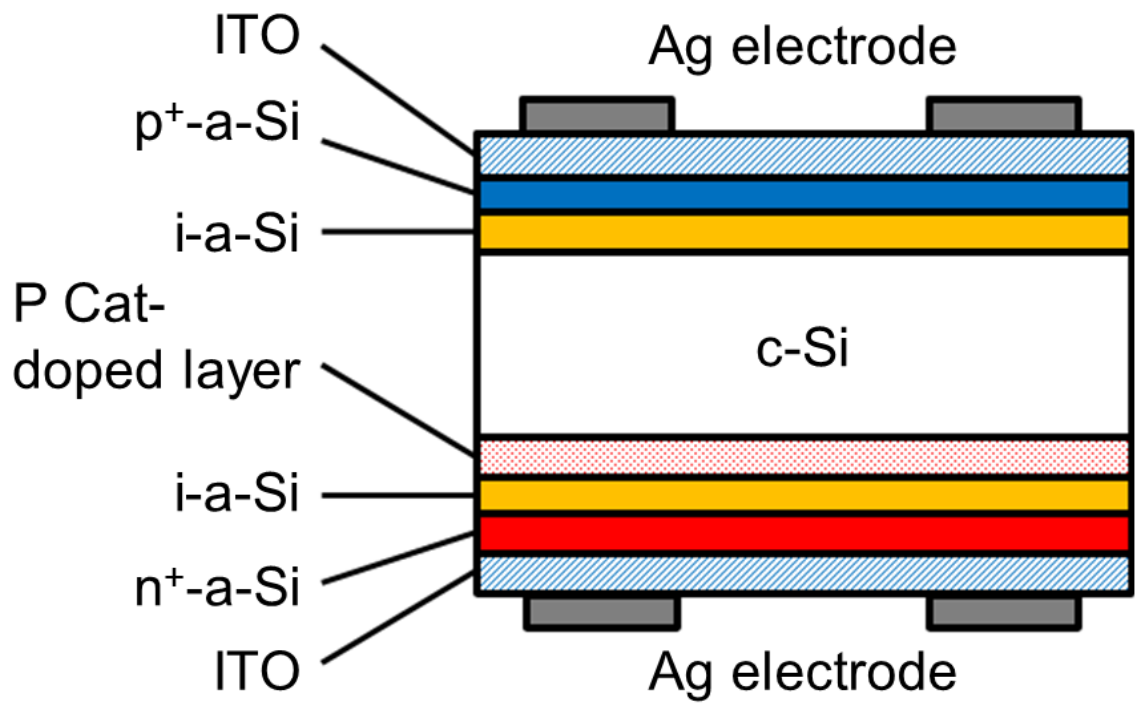


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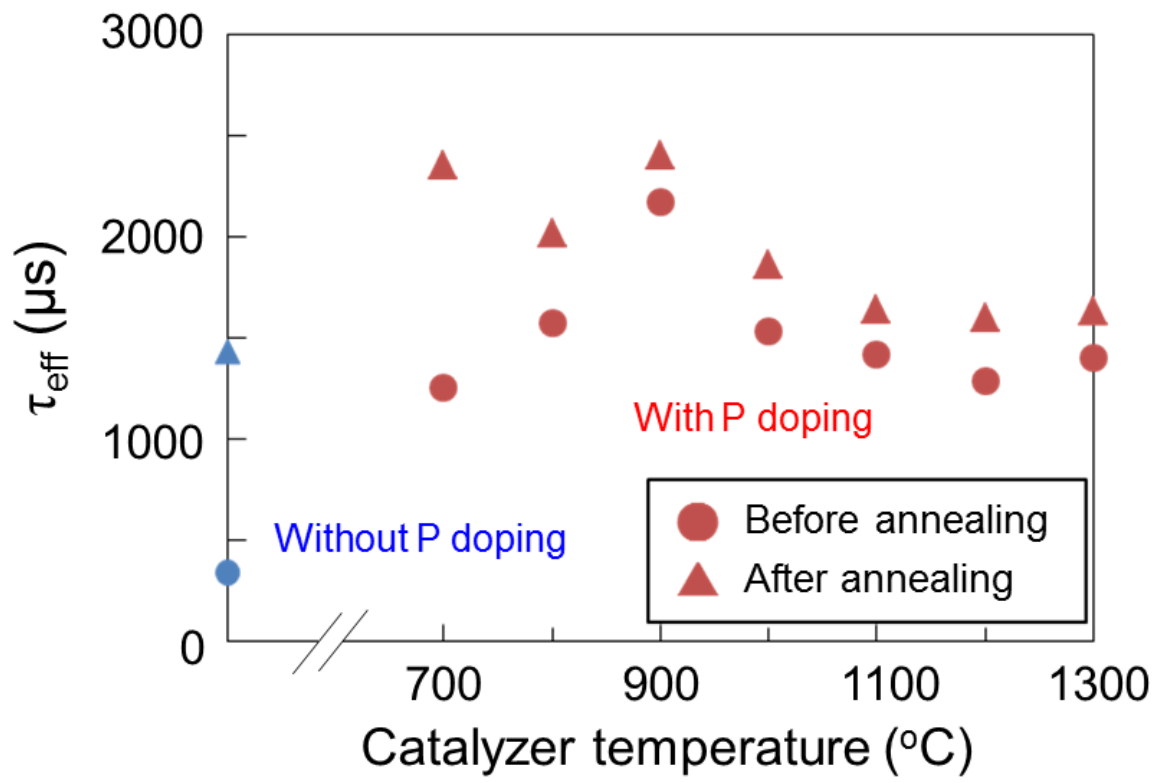


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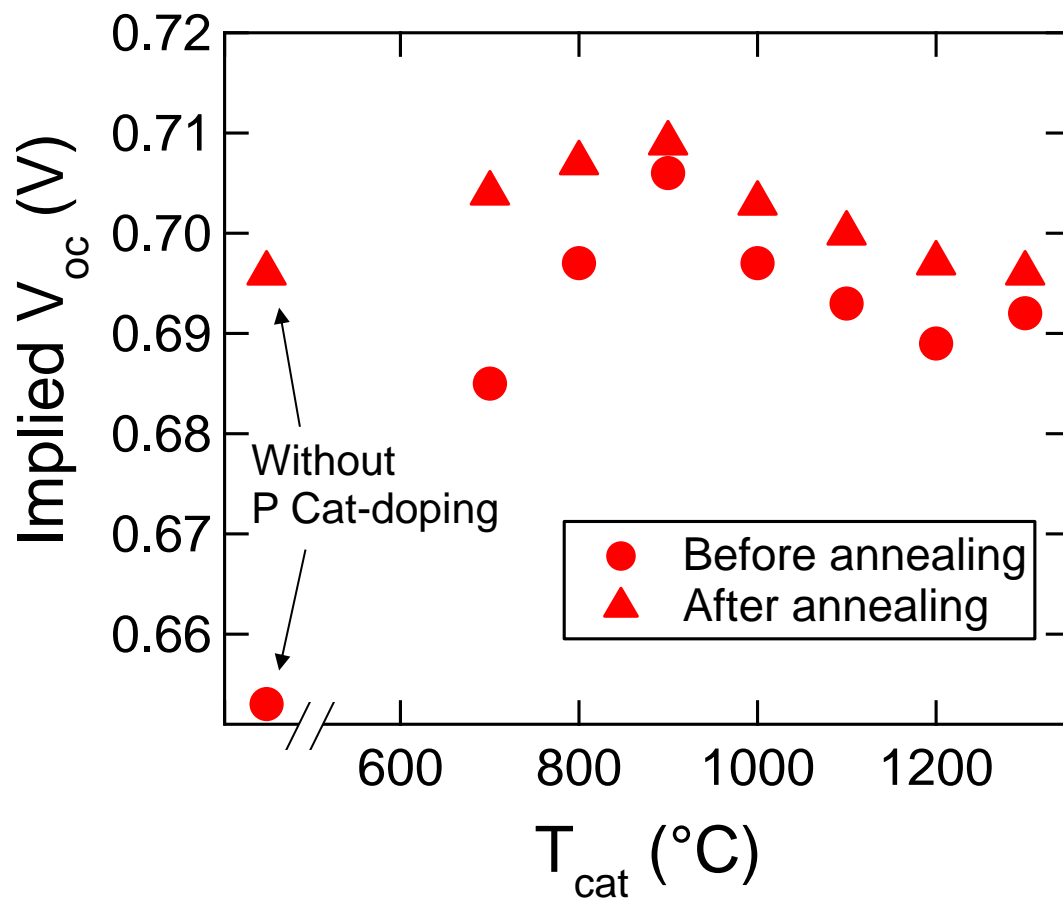


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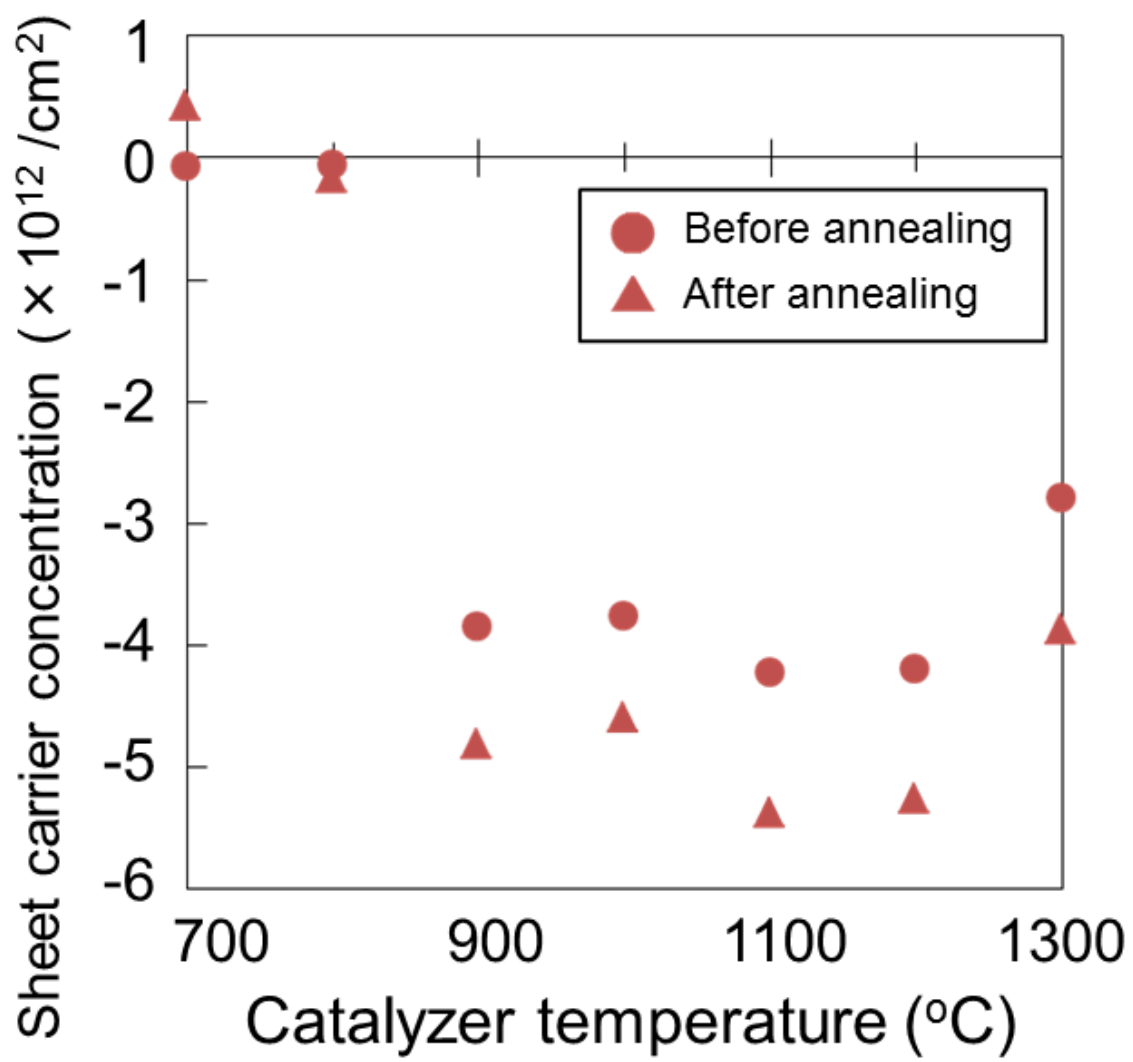


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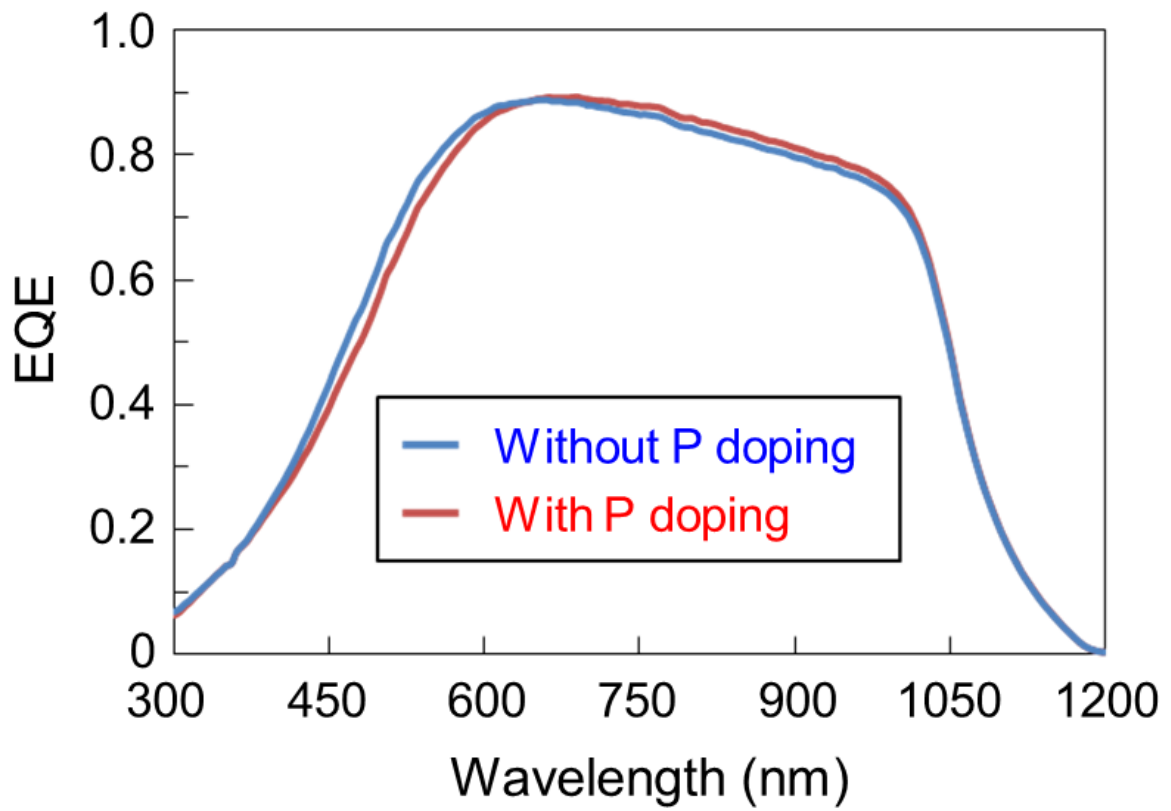


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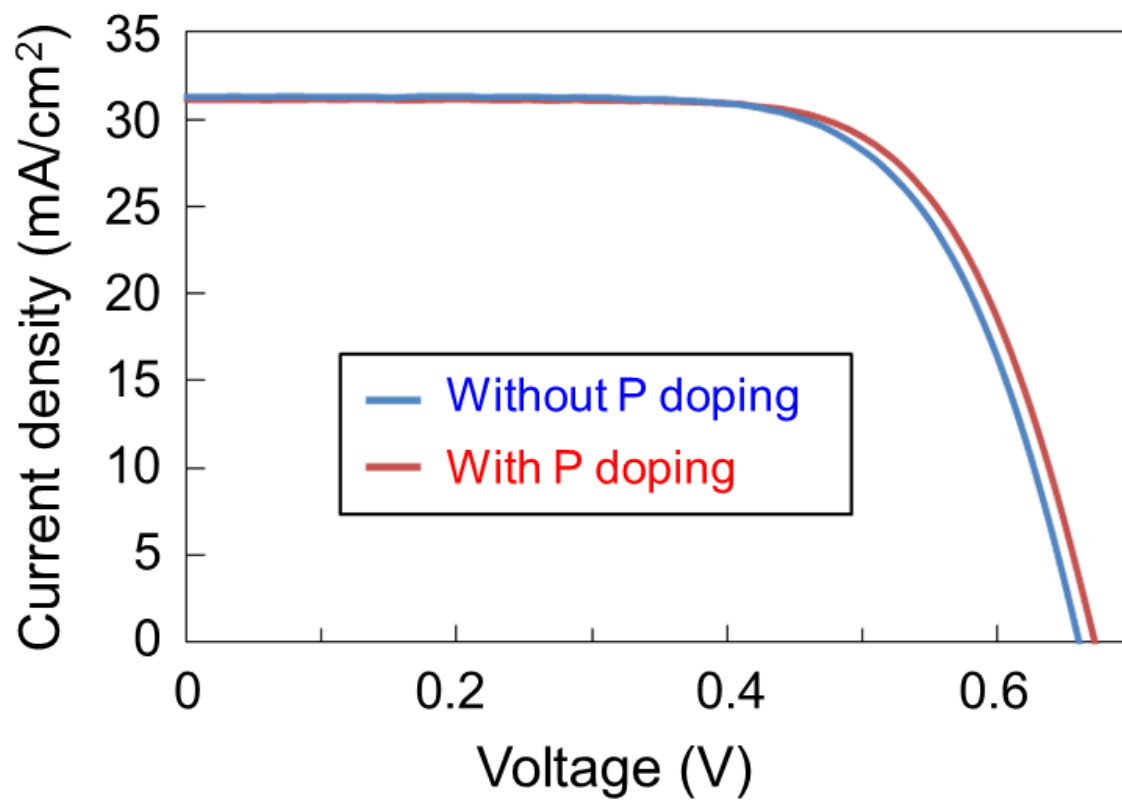


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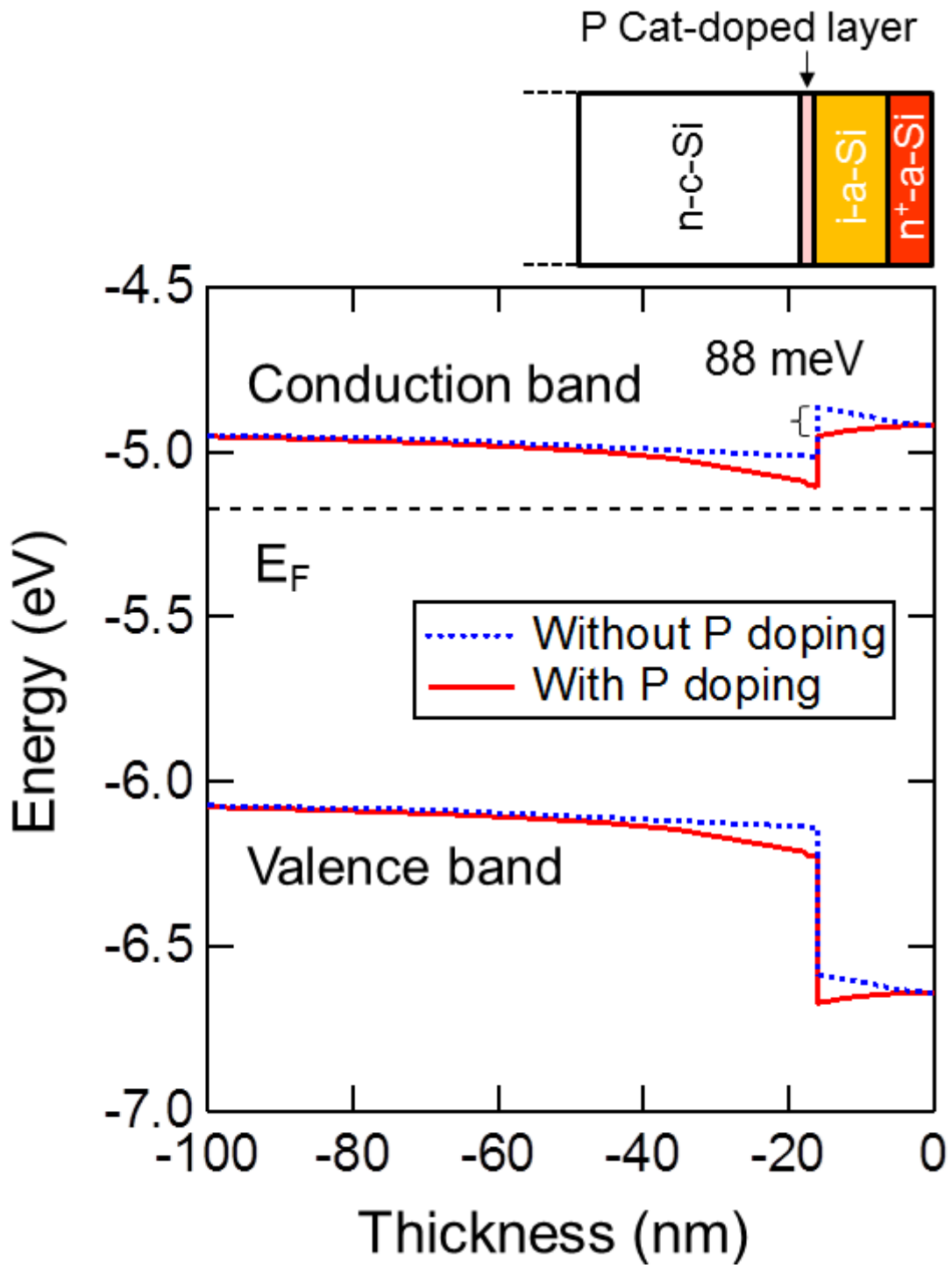


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