A Study on Solution-Processed Self-Aligned ZrInZnO Thin Film Transistor

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Doctoral Dissertation

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ABSTRACT OF DOCTORAL DISSERTATION

To realize all solution-process self-aligned oxide semiconductor thin film transistor (TFT), we have developed a novel diffusion method to dope the oxide semiconductor source and drain regions (S/D regions). Since the self-aligned structure exhibits a low parasitic capacitance and an ability to scale down the size of the device, the TFT with this structure was studied in this dissertation. We studied the ZrInZnO as an oxide semiconductor because of its ability in improving the TFT performance and bias-stress ability.

In our diffusion method, a doping solution, i.e. Sn:PPC solution which is a mixture of a Sn solution and polypropylene carbonate (PPC) solution was prepared. The Sn:PPC solution was coated on the ZrInZnO S/D regions and then the sample was annealed to allow Sn atoms diffuse into the ZrInZnO. Because PPC can be decomposed completely into CO_2 and HO_2 at temperature below 300 ^oC, the utilization of PPC helps to prevent the formation of the SnO_x film, derived from the Sn solution, between S/D regions of the self-aligned structure.

The first work of this study involves the preparation and characterization of the Sn:PPC solution. TG/DTA, FT-IR, DLS and mass spectrometry methods were used to characterized the Sn:PPC solution. The results show that the solute in the Sn:PPC solution was in an configuration with coordination of large PPC molecules with Sn clusters. The Sn cluster was in a configuration of coordinated PrA ligand, water and oxygen around the Sn atom. The size of the Sn clusters was about 1.6 nm, while PPC molecules in solution was about 1.9 nm, 5.5 nm, 37.6 nm and 721 nm.

In the second work, the Sn:PPC solution was employed to fabricate high conductivity ZrInZnO for S/D regions of self-aligned TFT. The Sn:PPC solution was coated and annealed to make Sn diffuse into the ZrInZnO film. It was confirmed by AUS method that Sn diffused into ZrInZnO film to a depth of 22 nm. Sn acts as a donor in ZrInZnO, which results in an increase in the conductivity of the ZrInZnO film. Resistivity of the Sn-diffused ZrInZnO was reduced from 4×10^3 Ω cm to 1.8×10^{-2} Ω cm at annealing temperature of 300 ^oC under N_2 ambience when the Sn:PPC solution was used. The increase in resistivity of the sample annealed at temperature over 500 ^oC was due to the change in structure characteristic of the ZrInZnO film. To make high conductive ZrInZnO the ambience including oxygen should be avoided.

The third work concentrated to fabrication of self-aligned ZrInZnO TFT. The source and drain region of the TFT was doped by using the Sn:PPC solution. The self-aligned ZrInZnO TFT exhibited a mobility of 20 $cm^2 V^{-1} s^{-1}$, a threshold voltage of 1 V, a subthreshold swing of 0.2 V/decade, and an ON/OFF ratio of 7. These results indicate that the solution-based doping could provide an alternative way to substitute the ion implantation or plasma treatment which are conducted under vacuum for fabrication of the self-aligned oxide semiconductor TFT.

Because the purpose of this study is to realize all-solution-processed self-aligned oxide semiconductor TFT, the last work reports a high quality gate insulator fabricated by the solution process. Here I presented the investigation of a polysilazane-derived SiO_2 gate insulator prepared using a wet-annealing method. The leakage current density of the wet-annealing SiO_2 film was 2.2×10^{-9} A/cm^2 at 1 MV/cm, which was more than one order of magnitude smaller than that of dry-annealed SiO_2 films. The solution-processed ZrInZnO TFT with both reserve staggered and self-aligned structures prepared using the wet-annealed SiO_2 film as the gate insulator exhibited a rather small gate leakage current of less than 7×10^{-11} A/cm^2 at 15 V. The off current was also dramatically decreased owing to the good performance of the wet-annealed SiO_2 gate insulator.

Generally, the present thesis exposes that all-solution-processed self-aligned oxide semiconductor TFT can be realized in order to reduce the total fabrication cost and production energy that are important factor in electronic device manufacturing and in our modern life.

Key words: *self-aligned thin film transistor, oxide semiconductor, solution process, polypropylene carbonate, Sn diffusion.*

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Chapter 1

General introduction

1.1 Oxide semiconductor thin film transistor (OS TFT)

In this work, I studied on the ZrInZnO self-aligned thin film transistor (TFT). The ZrInZnO is a type of oxide semiconductor materials which have recently gained considerable attention in emerging electronic applications, such as flat-panel displays (FPDs), transparent and flexible displays including electronic papers (e-papers), organic light-emitting-diode displays (OLEDs) and liquid crystal displays (LCDs) [1-7]. This section will give a brief overview of oxide semiconductor TFT (OS TFT).

1.1.1 History of OS TFT

The first version of an OS TFT was reported in 1964 [8]. The TFT was fabricated on a glass substrate utilizing evaporated SnO_2 as the channel layer with

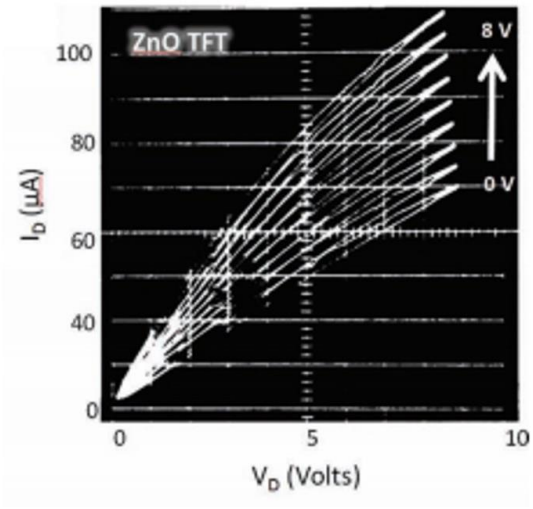


Figure 1-1. I_D – V_D characteristic of a single crystal ZnO TFT.

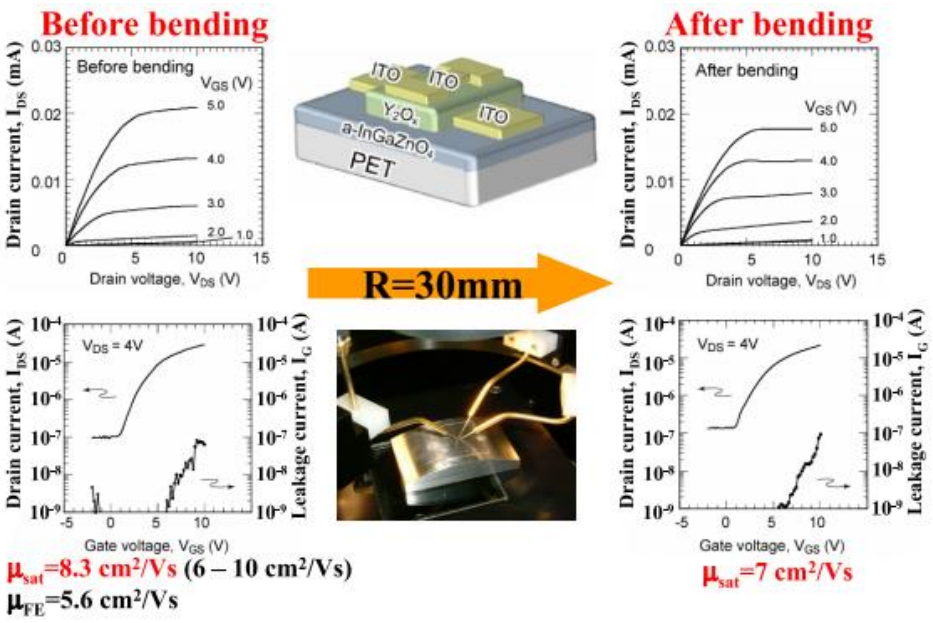


Figure 1-2. Flexible and transparent TFT utilizing oxide semiconductor fabricated on flexible PET substrate. Good TFT performance with saturation mobility above 7 $cm^2 V^{-1} s^{-1}$ is maintained even after a bending test with a curvature radius of 30mm [21].

bottom gate staggered structure, aluminum source/drain and gate electrodes, and an anodized Al_2O_3 gate dielectric. However, the SnO_2 TFTs had a very poor performance: output current did not saturate at large V_D, device could not able to turn off, and an almost negligible amount of transfer curve was observed. Then, in 1968, G.F. Boesen et al [9] reported a ZnO single crystal semiconductor TFT. However, these devices exhibited a very small drain current (I_D) and no I_D saturation when applied gate voltages (V_G) (see Figure 1-1).

After a long incubation period, in 2003 many reports on the poly-ZnO TFTs started to appear [10-12]. The poly-ZnO TFTs exhibited a rather good electrical performance, with a mobility of 2.5 $cm^2 V^{-1} s^{-1}$, showing that oxide semiconductor TFTs could be a viable technology and comparable with a-Si:H and organic TFTs. In 2004, several reports regarding oxide semiconductor TFTs continued to appear, bringing different innovations to this emerging area. Some of the most important achievements were: ZnO TFTs exhibiting improved device performance (mainly regarding mobility) while keeping low or even room temperature ZnO processing [13-15], non-vacuum processes to produce the ZnO layers [16], fully transparent ZnO

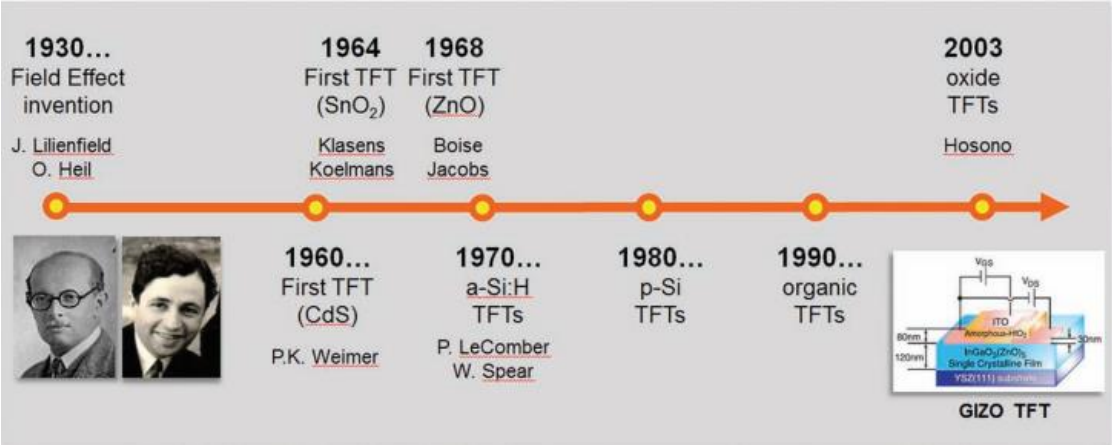


Figure 1-3. Main landmarks achieved with TFTs [24]

TFTs produced at room temperature [17], application of ZnO TFTs as UV photodetectors [18,19], exploration of SnO_2 TFTs [20].

However, the polycrystalline ZnO TFTs still remained many issues to be address, such as the instability and non-uniformity resulted from grain boundaries problem [21]. In addition, the ZnO and other oxide semiconductor materials had rather high residual free carrier concentration ($>10^{17}$ cm^{-3}) which results from zinc interstitials and oxygen vacancies. These problems lead the control of the threshold voltage and the fabrication of normally-off TFTs using poly-ZnO channels become difficult. Therefore, in order to solve these problems, in 2003 Nomura et al. utilized a high quality single crystalline $InGaZnO_4$ (sc IGZO) as a channel layer of the TFT and demonstrated that the residual free carrier concentration of the sc-IGZO film is not so high. As a result normally-off TFTs could be attained [22]. This layer also allowed to obtain an impressive effective mobility of 80 $cm^2 V^{-1} s^{-1}$, and an ON/OFF ratio of 10^6. Although this excellent performance was realized at a very high temperature of 1400 ° C, this paper made history. Because it proves that high-performance oxide semiconductor TFTs are a reality. In the following year (late 2004) Nomura et al. [23] represented their first result of a transparent TFTs with amorphous InGaZnO (α-InGaZnO) channels fabricated at room temperature on flexible polyethylene terephthalate (PET) substrate by pulsed laser deposition. The TFT exhibited a saturation mobility of around 8.3 $cm^2 V^{-1} s^{-1}$, threshold voltage of 1–2 V and on/off ratio of 10^3, as can be seen in Figure 1-2. Nomura's results opened

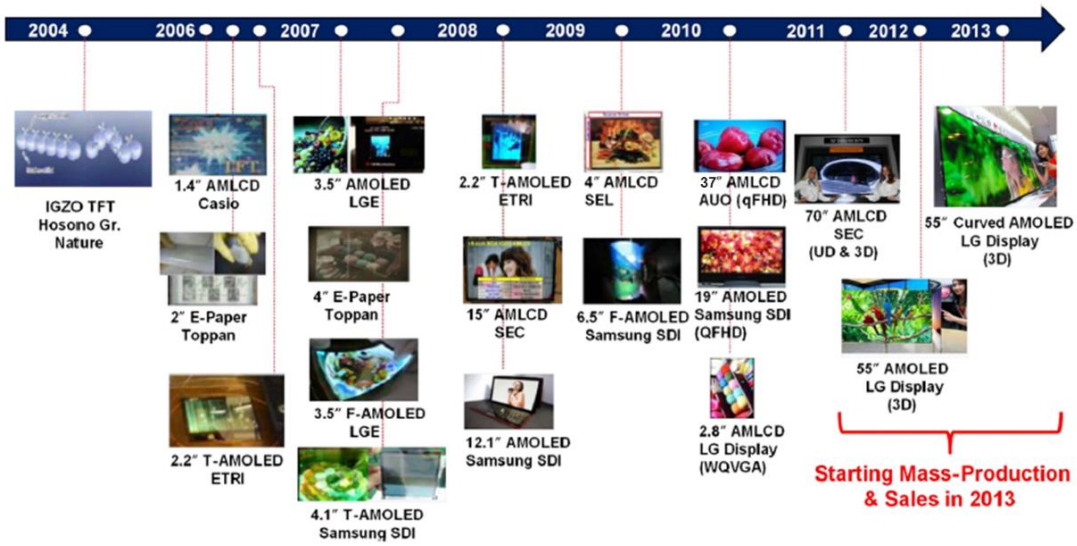


Figure 1-4. Historical overview of development in oxide semiconductor TFT-based devices [27].

the door for a rapidly growing number of publication regarding the application of amorphous multicomponent oxides as channel layer in flexible and transparent TFTs. The main landmarks achieved with either generic TFTs or oxide based TFTs are shown in Fig. 1-3.

1.1.2 Advantages of amorphous oxide semiconductor (AOS)

Since the report in 2004 of Nomura group on transparent and flexible AOS TFT, several display companies have joined to develop this type of TFTs as TFT backplanes for various FPDs including e-papers, OLEDs and LCDs. The largest panel sizes of prototype displays reached 19” for OLEDs [25] and 37” for LCDs as of early 2010 [26]. In 2013, a 55-in. AMOLED TV (LG Electronics), with options for flat or curved screens, reached commercial markets. The large active matrix (AM) OLED-productions based on oxide semiconductor devices become the major investments of Samsung, LG, Sharp and AUO. The development trends of prototype display panels based on oxide-semiconductors is reported in Figure 1-4. This section presents the key advantages of AOS materials to explain the reason why they become the promising channel materials for TFT backplanes in FPDs.

Table 1-1 shows some basic features of AOS TFTs for comparison with amorphous Si (a-Si:H) and low-temperature poly-Si (LTPS) TFTs utilized as TFT backplane in FPD. The AOS TFT combine advantages of a-Si:H and LTPS TFTs. They have relatively high mobilities (2 ~ 40 $cm^2 V^{-1} s^{-1}$), which can be used to drive OLEDs, large LCDs (e.g. 55 inches) and high-frame-rate 3D displays. The excellent uniform in device characteristics due to the amorphous structure, and low-temperature fabrication (below 400 ^oC or even at room temperature) made AOS TFTs to be compatible with large glass substrate and current FPD technology. The long term reliability of AOS TFTs is still under investigation, however, it is proved that the AOS TFTs are more stable than a:Si-H and organic TFTs.

Table 1-1. Comparison of a-Si:H, AOS and LTPS TFTs [21, 28, 29]

	a-Si:H	**AOS**	**LTPS**
Fabrication Temperature (^{o} C)	150 - 350	RT- 400 (600)	> 400
Mobility ($cm^2 V^{-1} s^{-1}$)	0.1 ~ 1	2 ~ 40	100 ~ 400
Uniformity	Excellent	Excellent	Bad
Stability	Bad	Good	Excellent
Pixel TFT	NMOS	NMOS	CMOS
Pixel circuit	Complex (ex. 4T 2C)	Simple (ex. 2T 1C)	Complex (ex. 5T 2C)
Main application	AMLCD	AMLCD/AMOLED	AMOLED
Cost	Low	Low	High

T: transistor, C: capacitance, NMOS: N-type Metal Oxide Semiconductor, CMOS: Complementary MOS

1.1.3 ZrInZnO TFTs

Electrical performance of oxide semiconductor TFTs (field-effect mobilities (μ_{FE}), sub-threshold gate swing (SS), and on/off ratios) have been dramatically improved since Nomura group reported on the amorphous InGaZnO TFTs. However, the TFTs still have some problems such as device instability under electrical bias and thermal stresses, which causes an obstacle in applying them in AMOLED displays [30, 31]. It was supposed that the problem of device instability is owing to the defect states, such as oxygen vacancies, in the active layers [32, 33]. Therefore to improve

the stability of the oxide TFTs, it is necessary to reduce the oxygen vacancies. For the InGaZnO oxide semiconductor material, one discovered that the Ga^{3+} ions make to suppress the formation of oxygen vacancies because they can tightly bind to oxygen ions [27]. This results from the fact that Ga has a low standard electrode potential (SEP) or high metal oxidization energy. After this discovery, there have been many studies reported on the incorporation of low SEP materials, such as Y [34], Hf [35], Zr [36], Mg [37], La [38], and Sc [39], which is believed to efficiently suppress the formation of oxygen vacancies, into the In–Zn–O system.

In 2009, Park et al. [36] introduced a novel ZrInZnO semiconductor materials (Zr was substituted for Ga) for use as robust channel layers of TFT to resolve the problem of device instability. The ZrInZnO film fabricated by RF sputter co-deposition using InZnO and ZrO_2 targets had nanoscale ZrInZnO crystallites dispersed in an amorphous phase matrix. The ZrInZnO TFTs exhibited the field effect mobility of 3.9 cm^2V^{-1} s^{-1}, swing slope of 0.98 V/decade, and ON/OFF ratio of 10^7. With regards to device stability, the shift of the threshold voltage under biasing stress at I_D = 3 μA for 60 hours was only 0.99 V, which is smaller than that obtained from a-IGZO TFTs and ZnO TFTs.

Following that, Jeong et al. [40], Chung et al. [41] and Tue et al. [42] reported on using the solution-processed ZrInZnO for channel layers of TFTs. They investigated the effects of adding Zr into InZnO through electrical characteristics of their films and TFTs. It was confirm that Zr atoms acted as electron charge suppressors in the ZIZO system, which effectively prevented the formation of oxygen vacancies and hence reduced interface charge trapping. This, in turn, improved the performance and bias-stress stability of the TFT.

1.2 Self-aligned oxide semiconductor thin film transistor

1.2.1 Advantages of self-aligned structure

Thus far, OS TFTs have been generally studied and developed as conventional structures which are widely used for fabrication of a-Si:H TFTs. These structures are illustrated in Figure 1-5 [21]. The TFT structures are specified by the stacking order of gate electrode, channel layer and source/drain electrodes (contacts) and classified into combination of top/bottom gate and top/bottom contact, as can be seen in Figure 5 (a) and (b). The inverted staggered structures (see Figure 5 (c) and (d)) have been employed for back-plane transistors in most prototype displays including AMLCDs

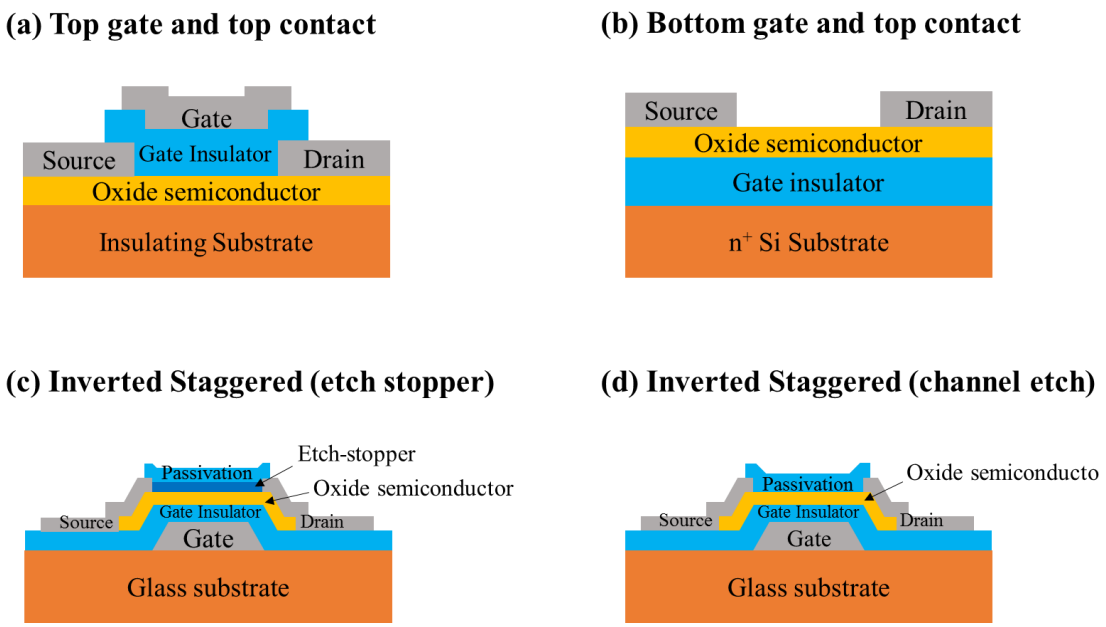


Figure 1-5. Typical conventional device structures used for OS TFTs

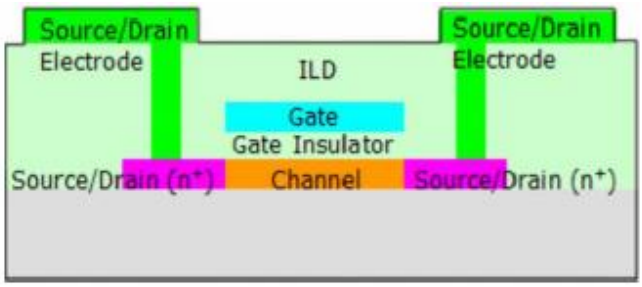


Figure 1-6. A schematic cross-sectional view of self-aligned top gate GIZO TFTs [47]

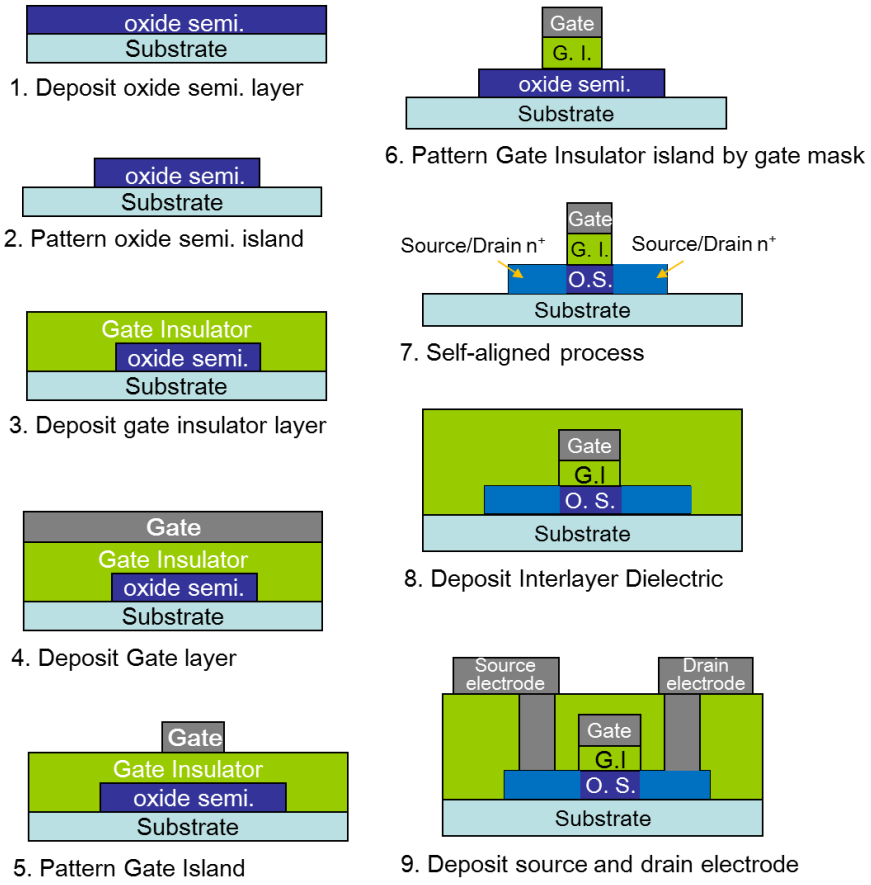


Figure 1-7. Fabrication step for self-aligned top gate AOS TFT

and AMOLEDs. However, these structures have two main problems that degrades performance of the TFTs. First, there is high parasitic capacitances due to large overlap areas between the source/drain electrodes and the gate, which can cause image flicker and sticking in displays, large noise in flat-panel displays, and long propagation delay when used in digital circuits [43]. The second problem is the difficulty in manufacture the short channel TFTs, which is important for improve driving current, due to $I_D \sim 1/L$, and thus device performance and circuit speed [44, 45]; and for fabricating larger and higher resolution AMLCDs and AMOLEDs.

The conventional structure OS TFTs cannot avoid the high parasitic capacitance and the adversity in scaling down the channel length which is a consequence of the overlapping area between the channel and the source/drain electrodes. Because to fabricate these conventional TFTs the source/drain electrodes and gate electrode are defined in different masking steps. Therefore, the reasonable large overlap between

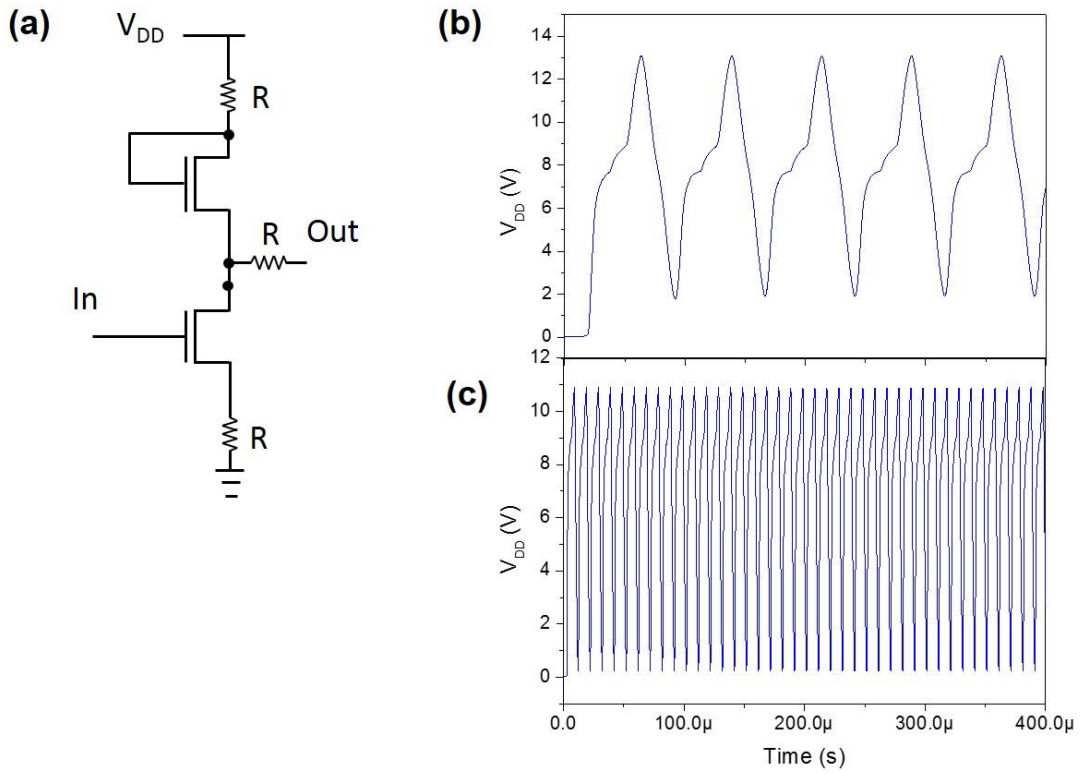


Figure 1-8. Inverter circuit configuration (a) and simulated output of ring oscillator with seven inverter stages based on the TFTs with (b) inverted staggered and (c) self-aligned structure

the channel and the source/drain electrodes must be designed to permit the alignment error between photolithography steps. This overlapping region can be as large as 66 % of the whole channel length in the case of a-Si-H TFTs with conventional structure [46].

In order to eliminate the required overlapping area and to obtain the shorter channel TFTs, and thus improve device performance, a self-aligned structure has been proposed. The widely used self-aligned structure for OS TFTs is shown in Figure 1-6. Figure 1-7 shows detail sequence of the fabrication steps for the TFT with self-aligned top gate structure. The most important step to acquire this type of TFT is the self-aligned process step (see Figure 1-7 (7)), which can produce high conductivity source and drain regions (Source/Drain n^+) from the OS layers. This step is also called as doping process or metallization process. Detail technology of self-aligned process for OS TFTs is described in section 1.2.2.

To confirm the effect of parasitic capacitance of the TFTs on digital circuit, I simulated ring oscillators consisting of seven inverter stages used the n-type AOS TFTs with self-aligned and inverted staggered structure (channel etch). The inverter circuit configuration of the simulated ring oscillator is shown in Figure 1-8 (a). The channel length of the TFTs is 10 μm. The simulations suggest that the oscillation frequency for a ring oscillator employing the self-aligned TFTs with mobility of 5 $cm^2\ V^{-1}\ s^{-1}$ and bias at V_{DD} = 15 V should be ~103 kHz which is eight times larger than one with inverted staggered structure, shown in Figure 1-8 (b) and (c).

1.2.2 Current status of self-aligned OS TFT researches

As mentioned above, the self-aligned process is most important step to achieve the self-aligned structure TFT. Thus far, there are different self-aligned process technologies have been developed for OS materials. They are including implantation of boron, phosphorous, or arsenic [48] - [50], the hydrogen, aluminum or fluorine diffusion [51] - [53], and the hydrogen plasma treatment [54], or the argon plasma treatment [47], etc.

The self-aligned top gate α-InGaZnO TFTs was firstly introduced by J. Park et al. in 2008 [47]. The Ar plasma was utilized to treat on the source/drain regions of the α-InGaZnO active layer to reduce the series resistance. Effect of Ar plasma is made to break the relatively weak In-O bonds. Then In atoms collect near the surface of the film, which causes the InGaZnO become more conductive. The self-aligned TFT had a mobility of 5 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of 0.2 V and subthreshold swing of 0.2 V/decade.

The diffusion method was applied to introduce the hydrogen, aluminum or fluorine atoms into α-InGaZnO source/drain regions. These atoms act as a donor in the InGaZnO, which helps increase carrier concentration, and thus increase conductivity. To employ these diffusion methods, they adopted SiN_x:H (grown by PECVD or plasma treatment), Al (deposited by DC magnetron sputtering), or SiN_x:F (inductively-coupled plasma chemical vapor deposition) as the InGaZnO source/drain passivation layer. By annealing process the hydrogen, aluminum or

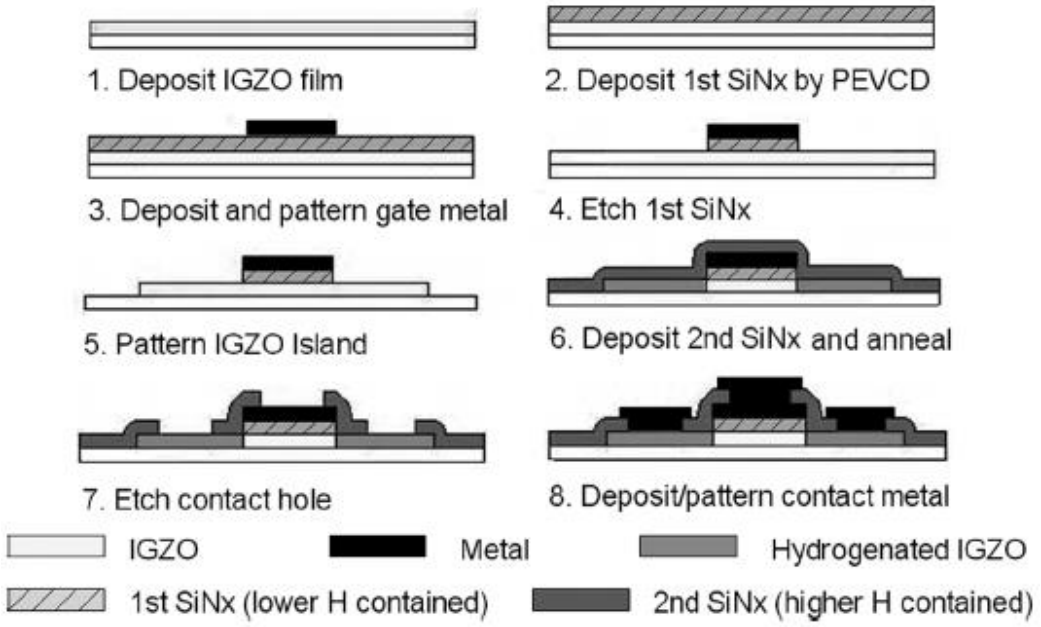


Figure 1-9. Process flow of the self-aligned top gate GIZO fabricated by hydrogen diffusion method [52]

fluorine atoms from these layers can diffuse into the InGaZnO. Figure 1-9 [51] shows fabrication steps of a self-aligned top gate InGaZnO TFT using hydrogen diffusion from SiN_x:H via PECVD.

The implantation methods have been investigated as a replacement of plasma treatment and hydrogen diffusion. Because they can enhance thermal stability of the TFTs. It was reported that by using boron implantation method we can apply a better quality passivation layer deposited at a temperature as high as 300 ^{o}C. Performance of the self-aligned OS TFTs prepared by different self-aligned processes is summarized in Table 1-2. However, most of the aforementioned methods are typically conducted under vacuum, which results in a complicated process and very high fabrication costs.

1.3. Solution process

Today, vacuum process is a process technology that has been widely used in laboratory research and in industry for mass production of electronic devices. As I mentioned above, however, the vacuum process still has various disadvantages. For example, from the viewpoint of efficient utilization of materials there is about 5

Table 1-2. The summarized transistor characteristics with different self-aligned processes

Published year	Self-aligned process	Gate structure	OS material	S/D regions' resistivity (Ω cm)	W/L (μm/μm)	Mobility ($cm^2 V^{-1} s^{-1}$)	On/Off ratio	SS (V/decade)	Threshold voltage (V)
2008 [47]	Ar plasma	Top	InGaZnO	4×10^{-3}	5/10	5	10^7	0.2	0.2
2009 [55]	Hydrogen diffusion	Bottom	InGaZnO	6.2×10^{-3}	60/10	9.5	10^9	0.13	0.13
2009 [51]	Hydrogen diffusion	Top	InGaZnO	2×10^{-1}	100/200	1.6	10^6	0.8	1
2009 [56]	NH_3 plasma	Top	InGaZnO	5.5×10^{-3}	10/4	6	10^7	0.23	0.21
2011 [52]	Al diffusion	Top	InGaZnO	4×10^{-3}	10/4	9.8	10^7	0.22	- 1.5
2011 [57]	Hydrogen diffusion	Top	InGaZnO	No report	4/(4~10)	23.3 ~ 24.7	~ 10^7	0.2 ± 0.01	3.6 ± 0.1
2012 [48]	Boron implantation	Top	ZnO	2×10^{-3}	30/16	2	10^6	0.2	0.1
2012 [58]	CHF3/O2 plasma treatment	Top	ZnO	No report	10/2	27	9×10^6	0.12	- 0.5
2012 [49]	Phosphorous implantation	Top	InGaZnO	No report	30/16	5	9×10^7	0.5	5.6
2013 [50]	Arsenic implantation	Top	InGaZnO	No report	30/16	12	9×10^7	0.5	3.2
2013 [59]	Ar Plasma	Top	InZnO	4×10^{-3}	10/10	157	10^9	0.19	0
2014 [53]	Fluorine diffusion	Bottom	InGaZnO	4.2×10^{-3} Ω cm	66/12	10.6	10^8	No report	No report
2014 [60]	Rapid thermal annealing	Bottom	InGaZnO	No report	200/50	8.3	3.1×10^6	0.44	1.4

to 10 % of source material that can be deposited on a substrate. In photolithography process most of deposited material is removed. Therefore when the entire fabrication process is completed, less than 1% of the original source material is left. Moreover, in vacuum process the generally required equipment are very large and complicated, which causes a high cost, a large space requirement and an increase in energy consumed for operation and maintaining vacuum environment.

In order to solve these problems, a solution process which uses functional liquid as source material to form thin films, patterns, and thus electronic devices was proposed. The solution process is a process that can fabricate the electronic devices with very high efficiency in material utilization. For example, when ink-jet technology is used, only less than 2 % of the source material is wasted [61]. In contrast with vacuum process equipment, typical solution process equipment is rather small, simple, and inexpensive. In addition, by means of the ink-jet or nano-imprint technology we can directly pattern thin films and devices, so the number of step in fabrication process will be decreased. As a result, the solution process helps reduction of the total fabrication cost and production energy that are important factors in electronic device manufacturing and of course, in our modern life.

1.4 Research objective and dissertation outline

The objective of this dissertation is applying the solution process to fabricate the ZrInZnO TFT with self-aligned structure to obtain a high performance device and to reduce fabrication cost and production energy. I have developed a special doping method for self-aligned process, which based on solution process. In particular, a doping solution, i.e. Sn:PPC solution which is a mixture of an Sn solution and a propylene carbonate (PPC) solution was prepared. The Sn:PPC solution was coated on the ZrInZnO S/D regions and then the sample was annealed to allow Sn atoms diffuse into the ZrInZnO. Because PPC can be decomposed completely into CO_2 and H_2O at temperature below 300 ^oC, the utilization of PPC helps to prevent the formation of the SnO_x film, derived from the Sn solution, between the S/D regions of

the self-aligned structure. Sn acts as a donor in ZrInZnO, resulting in an increase in the conductivity of the ZrInZnO S/D regions.

In this study, my aim is to develop and systematically investigate characteristics of the doping solution. Then, apply it to dope the ZrInZnO film and fabricate a self-aligned ZrInZnO TFT. Due to important role of gate insulator in performance of devices I also evaluate the wet-annealing SiO_2 derived from polysilazane solution.

This dissertation consists six chapters as follows.

After the introduction in chapter 1, chapter 2 reports on the characteristics of the doping solution, i.e. the Sn:PPC solution. At first, the characteristics of the Sn, PPC and Sn:PPC solution including thermal behavior and particle size distribution of the solute in these solution are discussed. Then, state of solute in the Sn:PPC solution is investigated by mass spectroscopy and FT-IR. From these results, model structure of the solute in the doping solution is proposed by the first principle calculation method. Furthermore, in this chapter a role of the PPC in the doping material is discussed.

Chapter 3 describes the doping process for the ZrInZnO by using the Sn:PPC solution. The effects of tin concentration in the Sn:PPC solution, annealing temperature, time and ambience on resistivity of the doped ZrInZnO is investigated. The dependence of resistivity of the doped ZrInZnO on annealing temperature is revealed. In order to confirm that Sn diffused into the ZrInZnO film, Auger electron spectroscopy was performed.

Chapter 4 deals with the fabrication and analysis of self-aligned ZrInZnO TFTs with source/drain regions doped by the Sn:PPC solution.

Chapter 5 focuses on an investigation of the wet-annealing SiO_2 derived from polysilazane solution as a gate insulator for the TFTs with rather small leakage current in comparison with the dry-annealing SiO_2. The FT-IR analysis is utilized to characterize the wet-annealed SiO_2 film. Electrical properties (I-V and C-V) of the film is reported. Finally, this chapter presents the fabrication and characterization of the ZrInZnO TFT using the wet-annealed SiO_2 gate insulator.

Reference

[1] Kwon J. Y. et al., Electronic Material Letter, vol. 7, pp. 1, 2011.

[2] Park J. S. et al., Applied Physics Letter, vol. 95, pp. 013503, 2009.

[3] Rield T. et al, Journal of Display Technology, vol. 5, pp. 501, 2009.

[4] Jeong J. K., Semiconductor Science and Technology, vol. 26, pp. 034008, 2011.

[5] Park J. S. et al., Thin Solid Films, vol. 520, pp. 1679, 2012.

[6] Wager J. F. et al., Transparent Electronics, Springer, New York, 2008.

[7] Kamiya T. et al., Journal of Electroceramics, vol. 17, pp. 267, 2006.

[8] Klasens H. A. et al., Solid State Electronics, vol. 7, pp. 701, 1964.

[9] Boesen G.F. et al, Proc. IEEE, vol. 56, pp. 2094, 1968.

[10] Hoffman R. L. et al., Applied Physics Letter, vol. 82, pp. 733, 2003.

[11] Carcia P. F. et al., Applied Physics Letter, vol. 82, pp. 1117, 2003.

[12] Masuda S. et al., Journal of Applied Physics, vol. 93, pp. 1624, 2003.

[13] Fortunato E. M. C. et al, Applied Physics Letter, vol. 85, pp. 2541, 2004.

[14] Fortunato E. et al., presented at NATO Advanced Research Workshop, St Petersburg, RUSSIA , Jun 23-25 , 2004 .

[15] Nishii J. et al., Japanese Journal of Applied Physics, vol. 42, pp. L347, 2003.

[16] Norris B. J. et al., Journal of Physics D: Applied Physics, vol. 36, pp. L105, 2003.

[17] Fortunato E. M. C. et al., Advanced Materials, vol. 17, pp. 590, 2005.

[18] Bae H. S. et al., Applied Physics Letter, vol. 83, pp. 5313, 2003.

[19] Bae H. S. et al., Thin Solid Films, vol. 75, pp. 469, 2004.

[20] Presley R. E. et al., Journal of Physics D: Applied Physics, vol. 37, pp. 2810, 2004.

[21] Kamiya T. et al., Science and Technology of Advanced Materials, vol.11, pp. 044305, 2010.

[22] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano and H. Hosono, Science 2003, 300, 1269.

[23] K. Nomura , H. Ohta , A. Takagi , T. Kamiya , M. Hirano , H. Hosono , Nature 2004, 432 , 488.

[24] E. M. C. Fortunato, P. M. C. Barquinha, and R. F. P. Martins, Adv. Mater. 2012, 24, 2945.

[25] H. D. Kim, J-S Park, Y. G. Mo and S. S. Kim 2009 *9th Int. Meeting on Information Display* (12–16 October 2009, Seoul, Korea) 3-1.

[26] M-C Hung, W. T Lin, J. J. Chang, P. L. Chen, C. Y. Wu, C. J. Lin, H. L. Chiu, C. Y. Huang and Y. C. Kao 2010 *Int. Workshop on Transparent Amorphous Oxide Semiconductors 2010* (*25–26 January 2010, Tokyo, Japan*) http://techon.nikkeibp.co.jp/english/NEWS_EN/20100128/179719/

[27] J-S. Park, H. D. Kim and I-D. Kim, J. Electroceram. 2014, 32, 117.

[28] A. Nathan, S. Lee, S. Jeon, and J. Robertson, J. Disp. Tech. 2014, 10, 917.

[29] S. H. Cho et al, in *SID Int. Symp. Dig. Tech. Papers* 2014, 45, 473.

[30] A. Suresh and J. F. Muth, *Appl. Phys. Lett.*, 2008, 92, 033502-1.

[31] R. B. M. Cross and M. M. De Souza, *Appl. Phys. Lett.*, 2006, 89, 263513-1.

[32] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, *Appl. Phys. Lett.*, 2008, 93, 123508-1.

[33] E. Chong, K. C. Jo, and S. Y. Lee, *Appl. Phys. Lett.* 2010, 96, 152102-1.

[34] J.W. Hennek, M.-G. Kim,M. G. Kanatzidis, A. Facchetti, and T. J.Marks, *J. Amer. Chem. Soc.*, 2012, 134, 9593.

[35] W. H. Jeong, G. H. Kim, H. S. Shin, B. D. Ahn, H. J. Kim, M.-K. Ryu, K.-B. Park, J.-B. Seon, and S. Y. Lee, *Appl. Phys. Lett.*, 2010, 96, 093503-1.

[36] J.S. Park, K. S. Kim, Y.-G. Park, Y.-G. Mo, H. D. Kim, and J. K. Jeong, *Adv. Mater.* 2009, 21, 329.

[37] G. H. Kim, W. H. Jeong, B. D. Ahn, H. S. Shin, H. J. Kim, H. J. Kim,

M.-K. Ryu, K.-B. Park, J.-B. Seon, and S.-Y. Lee, *Appl. Phys. Lett.* 2010, 96, 163506-1

[38] D. N. Kim, D. L. Kim, G. H. Kim, S. J. Kim, Y. S. Rim, W. H. Jeong, and H. J. Kim, *Appl. Phys. Lett.*, 2010, 97, 192105-1.

[39] Y. Choi, G. H. Kim, W. H. Jeong, J. H. Bae, H. J. Kim, J.-M. Hong, and J.-W. Yu, *Appl. Phys. Lett.*, 2010, 97, 162102-1.

[40] T. H. Jeong, S. J. Kim, D. H. Yoon, W. H. Jeong, D. L. Kim, H. S. Lim, and H. J. Kim, *Jpn. J. Appl. Phys.* 2011, 50, 070202.

[41] Y. W. Chung, F. C. Chen, Y. P. Chen, Y. -Z Chen, and Y.-L. Chueh, *Phys. Status Solidi* 2012, 6, 400.

[42] P. T. Tue, T. Miyasako, J. Li, H. T. C. Tu, S. Inoue, E. Tokumitsu, and T. Shimoda, *IEEE Trans. Electron Devices*, 2013, 60, 320.

[43] P. Mei, J.P. Lu, C. Chua, J. Ho, Y. Wang, J.B. Boyce, MRS Symp. Proc. 1999, 557.

[44] S. M. Sze, Semiconductor devices Physics and Technology, John Wiley and Sons, 2001, pp. 199.

[45] J.P. Lu, P. Mei, J. Rahn, J. Ho, Y. Wang, J.B. Boyce, R.A. Street, Journal of Non-Crystalline Solids 2000, 266, 1294.

[46] J.P. Lu, P. Mei, R. Lujan, and J. B. Boyce, "Performance study of self-aligned amorphous silicon thin-film transistor circuit", Proc. 4th Thin Film Transistor Technol. 1998, 392.

[47] J. Park, I. Song, S. Kim, S. Kim, C. Kim, J. Lee, H. Lee, E. Lee, H. Yin, K. –K. Kim, K. –W. Kwon, and Y. Park, *Appl. Phys. Lett.*, 2008, 93, 053501.

[48] Z. Ye, L Lu, and M. Wong, *IEEE Trans. Electron Devices*, vol. 59, pp. 393, 2012.

[49] R. Chen, W Zhou, M Zhang, M Wong, and H-S Kwok, "Self-Aligned Indium–Gallium–Zinc Oxide Thin-Film Transistor with Phosphorus-Doped Source/Drain Regions," *IEEE Electron Device Lett.*, vol. 33, pp. 1150, 2012.

[50] R. Chen, W Zhou, M Zhang, M Wong, and H-S Kwok, "Self-Aligned Indium–Gallium–Zinc Oxide Thin-Film Transistor With Source/Drain Regions Doped by Implanted Arsenic," *IEEE Electron Device Lett.*, vol. **34**, pp. 60, 2013.

[51] C. –H. Wu, H. –H Hsieh, C. –W. Chien, and C. –C. Wu, *J. Display Technol.*, 2009, 5, 515.

[52] N. Morosawa, Y. Ohshima, M. Morooka, T. Arai and T. Sasaoka, *Jpn. J. Appl. Phys.* 2011, 50, 096502.

[53] J. Jiang, M. Furuta, and D. Wang, *IEEE Electron Device Lett.* 2014, 35, 933.

[54] D. H. Kang, I. Kang, S. H. Ryu, and J. Jang, "Self-Aligned Coplanar a-IGZO TFTs and Application to High-Speed Circuits," *IEEE Electron Device Lett.*, vol. 32, pp. 1385, 2011.

[55] A. Sato, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, *Appl. Phys. Lett.*, 2009, 94, 133502.

[56] S. Kim, J. Park, C. Kim, I. Song, S. Kim, S. Park, H. Yin, H.-I. Lee, E. Lee, and Y. Park, *IEEE Electron Device Lett.* 2009, 30, 374.

[57] D. H. Kang, I. Kang, S. H. Ryu, and J. Jang, *IEEE Electron Device Lett.* 2011, 32, 1385.

[58] R. Chen, W. Zhou, M. Zhang, and H. S. Kwok, *Thin Solid Film* 2012, 520, 6681.

[59] J. C. Park, H.-N. Lee, and S. Im, *ACS Appl. Mater. Interfaces* 2013, 5, 6990.

[60] H.-C. Wu and C.-H. Chien, *IEEE Electron Device Lett.* 2014, 35, 645.

[61] J. Bharathan and Y. Yang, *Appl. Phys. Lett.*, 1998, 72, 2660.

Chapter 2

Characterization of the Sn:PPC solution

2.1. Introduction

As mentioned in section 1.2 of chapter 1, the self-aligned process is most important step to achieve the self-aligned structure TFT. This is a process which can produce high conductivity source and drain regions from the oxide semiconductor (OS) layers (in the case of self-aligned OS TFT). So far, there are different self-aligned process technologies have been developed for OS materials such as plasma treatment, implantation and diffusion method [1- 8]. However, most of the aforementioned methods are typically conducted under vacuum, which results in a complicated process and very high fabrication costs. On the contrary, by employing the solution process costs would be greatly decreased, because it can simplify equipment and efficiently use materials and production energy. Up to now, there has not been any study on the application of a solution process to self-aligned process for the OS TFT. It is thus apparent that in order to apply the solution process to self-aligned process a functional solution should be employed. The functional solution utilized in this study is a solution of Sn and polypropylene carbonate (PPC), denoted as Sn:PPC solution. The PPC, an aliphatic polycarbonate (Figure 2-1) synthesized via the copolymerization of CO2 and propylene was used here because it has a unique

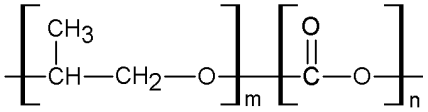


Figure 2-1. Molecular structure of PPC

property. It can be completely decomposed into H_2O and CO_2 at temperature below 300 °C (see thermal gravimetric profiles of the PPC shown in Figure 2-2). Therefore the combination of the Sn solution with the PPC solution helps to prevent the formation of the SnO_x film, derived from the Sn solution, between the S/D regions of the self-aligned structure. In this chapter characteristics of the Sn:PPC solution which was systemically investigated is reported.

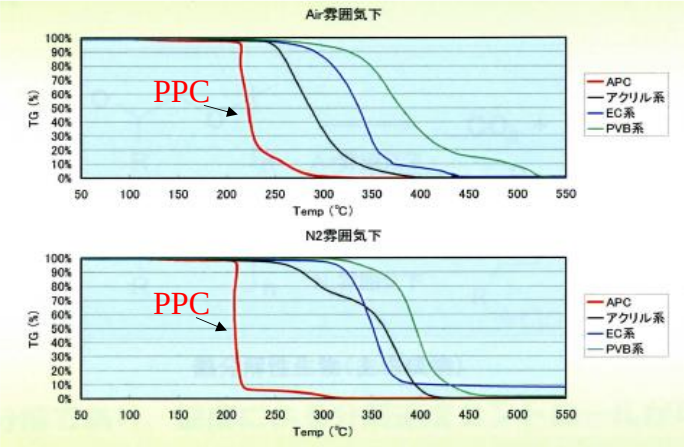


Figure 2-2. Thermal gravimetric profiles of PPC (from Sumitomo Seika Chemicals Co., Ltd., Osaka, Japan)

2.2 Experimental procedure

2.2.1 Preparation of the Sn:PPC solution

To synthesize the doping solution_ Sn:PPC solution, two solutions were prepared: Sn solution and PPC solution. The PPC solution had a concentration of 6 wt% purified PPC (Sumitomo Seika Chemicals) at molecular weight of 23.4×10^4 g/mol, which was prepared by dissolving PPC in diethylene glycol monoethyl ether acetate (DEGMEA) (Tokyo Chemicals Industry). The solution was stirred for 12 hours at 50 °C to completely dissolve PPC in DEGMEA. For the synthesis of the Sn solution, tin acetyl acetonate ($Sn(Acac)_2$) [$Sn(OCCH_3CHOCCH_3)_2$] (Sigma-Aldrich) was dissolved in propionic acid (Kanto Chemical) and stirred for 1 h at 120 °C. Concentration of the Sn solution was 0.2 mol/kg. The Sn:PPC solution was obtained by dispersing the Sn solution in PPC solution and stirring for 1 hour at room temperature.

The tin content in the Sn:PPC solution was controlled by varying the mixing ratio of the Sn solution to the PPC solution. The Sn:PPC solutions were prepared with different weight ratio of [Sn solution] : [PPC solution]. For example, the Sn:PPC solution 10 means a solution with weight ratio of [Sn solution] : [PPC solution] = 10:100. The Sn:PPC solution investigated in this chapter was the Sn:PPC solution 10.

2.2.2 Characterization

Thermal behavior of the Sn solution, PPC solution and mixture Sn:PPC solutions was analyzed by the thermal-gravimetry-differential thermal analysis (TG-DTA) using TG/DTA 6200 SII Nano-Techonology Inc. system. The solutions were measured from room temperature to 600 ^{o}C at a temperature rising rate of 5 ^{o}C/min, and under air ambience.

Dynamic light scattering (DLS) was used to determined particle size distribution of the solute in the Sn, PPC and Sn:PPC solution. In this study the DLS measurement was performed by using Zetasizer Nano (Malvern Instrument).

Structure of solute in the Sn and Sn:PPC solution was determined by cryspray ionization Fourier-transform ion cyclotron resonance mass spectrometry (CSI-FT-ICR-MS) produced by Bruker Daltonics Inc. Solarix-JA. The positive mode was carried out. The obtained data is a ratio m/z, which is the mass number divided by charge number of the detected complex, and equals to the molecular weight since the charge number was 1.

The molecular composition of the solutions, gel and solid state were characterized by using a Fourier transform infrared (FT-IR) spectrophotometer (Bruker Alpha). The transmission FT-IR measurement was carried in the range from 400 to 4000 cm^{-1}.

The molecular composition of the solute in the solution obtained from mass spectrometry was calculated by the first-principles calculation, which is supported by

Prof. Tadaoki Mitani. Based on the achieved structure, the FT-IR vibration spectra was determined.

The surface morphology was investigated by scanning electron microscope (SEM Hitachi S 4500).

2.3 Results and discussion

2.3.2 Role of PPC in self-aligned structure

Before reporting the characteristics of the Sn:PPC solution, I explain the reason why the PPC solution was used in the doping solution (Sn:PPC solution). The PPC solution was prepared by dissolving purified PPC in DEGMEA. The purified PPC consists a basic unit $[CH(CH_3)CH_2O]_m[CO_2]_n$. It is a biodegradable aliphatic polycarbonate that can be completely decomposed to H_2O and CO_2 at the temperature around 300 °C [9]. Moreover, it was supposed that the PPC solute in the PPC solution

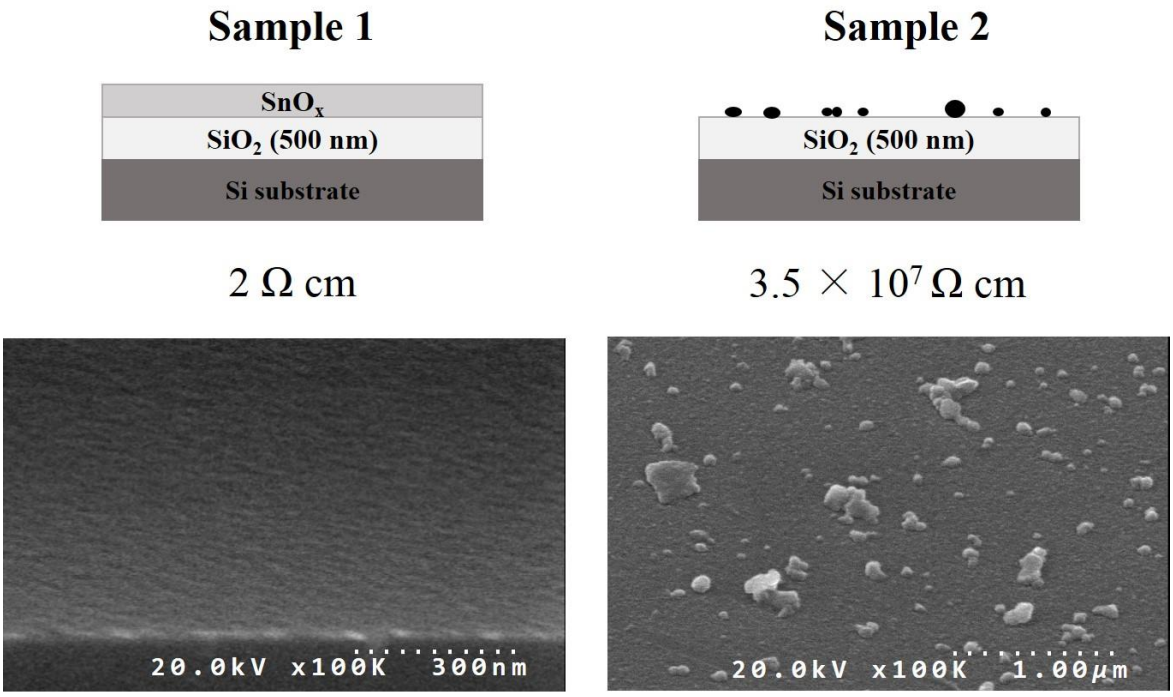


Figure 2-3. Schematic cross sections, resistivity and SEM surface images of the samples prepared by coating SiO_2/Si substrates with the solution containing only Sn (sample 1) and with the Sn:PPC solutions (sample 2) and annealing at 400 °C for 20 min.

exists in large-size particle. Therefore, when the Sn:PPC solution with high concentration of PPC was spin-coated to form a thin film and then heat-treated at temperature greater than 300 ^{o}C, the Sn solution-derived-SnO_x film would not be form. This is due to the complete decomposition of the large-size PPC particle, which leads to the excessive weight loss and shrinkage. As a result cracking could be occurred. Film would not be formed. Therefore, I believed that when the Sn:PPC solution was coated and heat-treated on the self-aligned TFT a SnO_x thin film would not be form between the source and drain regions (S/D regions).

To confirm the effect of PPC on preventing the formation of SnO_x between S/D regions of a self-aligned TFT we spin-coated the Sn solution and the Sn:PPC solution 10 onto 500-nm SiO_2/Si substrates to prepare samples 1 and 2, respectively. Subsequently, the samples were dried at 180 °C for 30 min and annealed at 400 °C for 20 min under nitrogen ambience. Resistivity of the 500 nm thick SiO_2/Si substrate was about 1×10^8 Ω cm. Resistivities of the sample 1 and the sample 2 are shown in Figure 2-3. Because of the formation of the SnO_x film on the SiO_2 substrate, the resistivity of sample 1 was reduced from 1×10^8 Ω cm to 2 Ω cm. In contrast, the resistivity of sample 2, which was treated using the Sn:PPC solution, was similar to that of the SiO_2 film. This means that the conductive SnO_x film did not form on the SiO_2/Si substrate. The validity of above statement was confirmed by using the SEM measurement. As can be seen from the SEM surface image of the sample 2 treated by the Sn:PPC solution no SnO_x film was formed; only SnO_x particles was remained. The obtained results, on the other hand, indicate that the use of PPC prevents the formation of SnO_x between source and drain (S/D) regions of a self-aligned TFT.

2.3.1 Thermal analysis

Figure 2-4 (a) shows thermal analysis results of the 6 wt% PPC solution using TG-DTA in ambient air at the temperature ranging from room temperature to 400 ºC. As can be seen from the TG curve the two weight loss regions were observed: one between 100 °C and 180 °C and the other at approximately 230 °C to 270 °C. The weight loss at the temperature greater than 270 ºC was 100 %. This indicates that, above 270 ºC PPC completely decomposed and no PPC remained. The DTA result shows two endothermic peaks at approximately 160 ºC and 235 ºC. The first endothermic peak corresponds to the significant weight loss (94.2 %) shown in the TG curve, which was attributed to dehydration and evaporation of the DEGMEA solvent. The second endothermic peak was assigned to the decomposition of PPC, which explains why no PPC remained at temperatures greater than 270 °C.

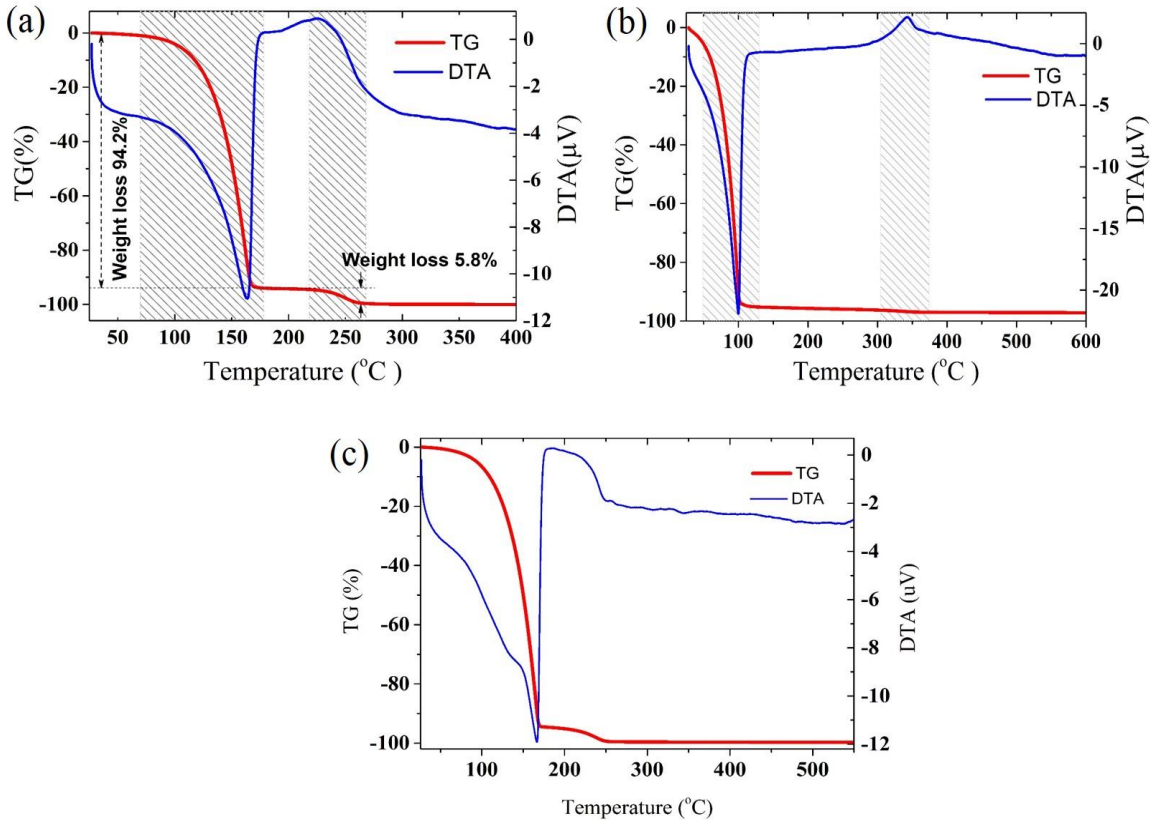


Figure 2-4. Thermal analysis of (a) PPC solution (6 wt%), (b) Sn solution (0.2 mol/kg) and (c) Sn:PPC solution 10

Figure 2-4 (b) shows the TG and DTA curves of the Sn solution with concentration of 0.2 mol/kg in ambient air. It was observed from the TG curve a dramatic weight loss of about 92 % occurred for the temperature from 50 ^{o}C to 100 ^{o}C. The endothermic peak corresponding to this region of weight loss indicates the evaporation of the propionic acid solvent in the solution. At around 345 ^{o}C the weight loss is about 97.5 %, which is corresponding to the exothermic peak in the DTA curve. The exothermic peak results from the formation of SnO_x. At the temperature greater than 345 ^{o}C no mass reduction can be observed.

Thermal analysis of the Sn:PPC solution 10 in ambient air is reported in Figure 2-4 (c). As can be seen, thermal behavior of the Sn:PPC solution and the PPC solution is rather similar. This is due to the fact that concentration of the PPC solution in the mixture Sn:PPC solution is much higher than that of the Sn solution, about 90 wt %. Because of a very small content of the Sn solution in the Sn:PPC solution, we could not observe the exothermic peak in the DTA curve of the Sn:PPC solution. However,

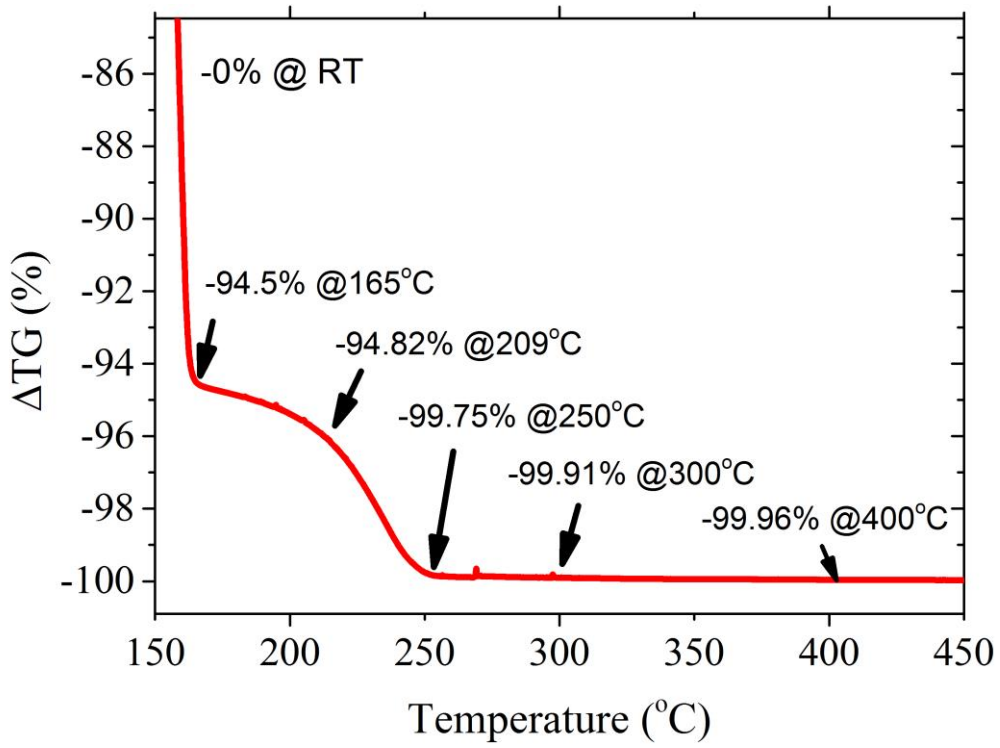


Figure 2-5. Enlargement of TG curve of Sn:PPC solution 10

it should be noted that the endothermic hump observed at 70 to 130 ^{o}C was attributed to the evaporation of the propionic acid solvent. The weight loss of the Sn:PPC solution, shown in Figure 2-5, at the temperature 250 ^{o}C was about 99.75 % and slightly reduced to 99.96 % at 400 ^{o}C. Thus, it is concluded that the very small amount of residual remained during heat treatment of the Sn:PPC solution is a product corresponding to decomposition of Sn-organics compound, which plays an important role for diffusion process, also known as doping process.

2.3.3 DLS measurement

The particle size distribution of the solute in the Sn, PPC and Sn:PPC solution was determined by DLS measurement, shown in Figure 2-6. DLS results demonstrated that each of the solution was comprised particles of multiple sizes. For the PPC solution, four particle sizes was observed from distribution. They were the

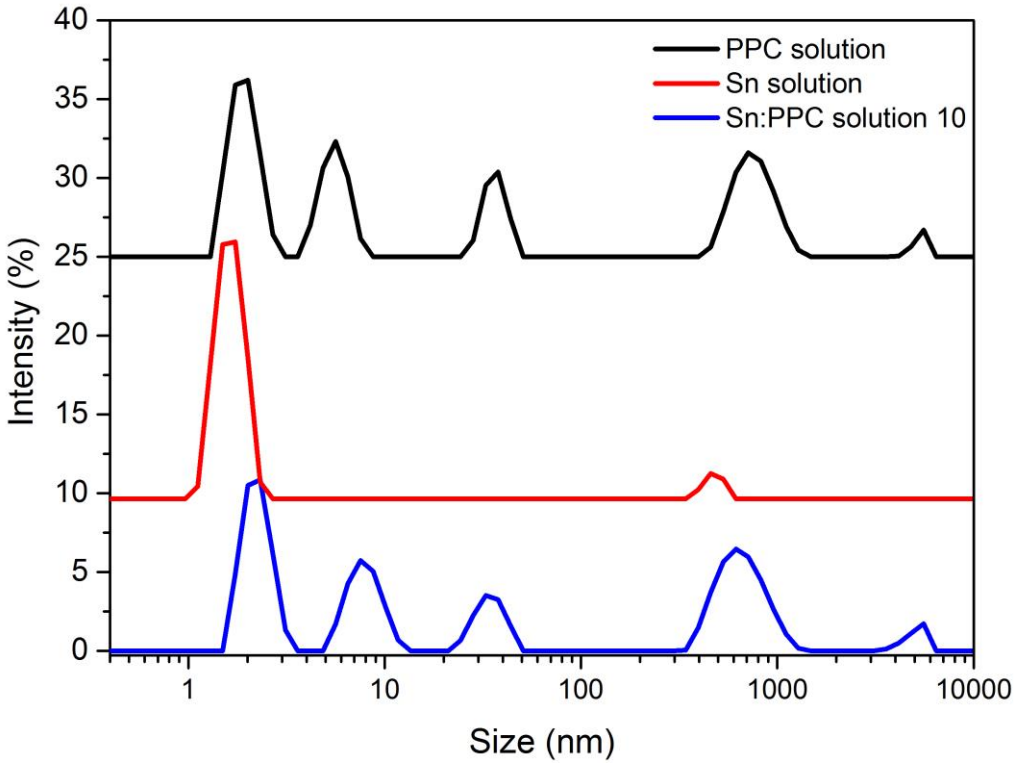


Figure 2-6. Intensity size distribution measured by dynamic light scattering at room temperature for the PPC solution, Sn solution, and Sn:PPC solution 10

sizes of about 1.9 nm, 5.5 nm, 37.6 nm and 721 nm. The size of roughly 5660 nm was suggested as dust contamination. It was supposed that the size of 1.9 nm represented to single polymer chains. The multiple size distribution of the PPC solution suggests that the particles aggregate together to form larger particles. There were two particle sizes existing in the Sn solution, one is about 1.6 nm corresponding to Sn-clusters and larger one is about 487 nm. The latter is assumed to be negligible minority. Particle size populations of the Sn:PPC solution are similar to one of the PPC solution.

2.3.4 Analysis structure of the solute in the Sn and Sn:PPC solution

2.3.4.1 The solute of the Sn solution

a. Mass spectrometric analysis

It was considered that structure of the solute in the Sn:PPC solution strongly affects to doping process. Because the Sn solution was dissolved in the PPC solution, it is very important to clarify the effect of PPC on the structure of solute in the solution. Therefore this section presents an investigation of the structure of solute in the Sn solution.

Figure 2-7 (a) and (b) show the mass spectrometric results in positive-mode measurements of the solute in the Sn solution. As can be seen, many peaks in the range from 400 to 500 m/z was detected. The ratio m/z is the mass number divided by the charge number of detected complex, and equal to molecular weight since the charge number was 1. The peak corresponding to Sn acetylacetonate (m/z = 316) was not observed. This means that the solute of the Sn solution did not exist in monomeric structure of Sn-acetylacetonate (Sn-acac). It was suggested that an exchange between acac ligands and propionic acid (PrA) ligand occurred. The structure of the solute in the Sn solution was supposed as a form the multimers of Sn. The individual peak intervals in Figure 2-7 (b) show differences in the molecular weights, with the peak interval of 26 demonstrating ligand exchange between

acetylacetonate ($OCCH_3CHOCCH_3^-$, MW = 99) and PrA ($CH_3CH_2COO^-$, MW = 73, referred as EtCOO) ligands and the peak interval of 16 corresponding to the increase and decrease of an oxygen atom in Sn multimers. The highest peak is from a molecule with molecular weight of 403. It is clear that the acac ligand was replaced by EtCOO ligand in the PrA solvent. Therefore the Sn multimers comprised EtCOO ligands.

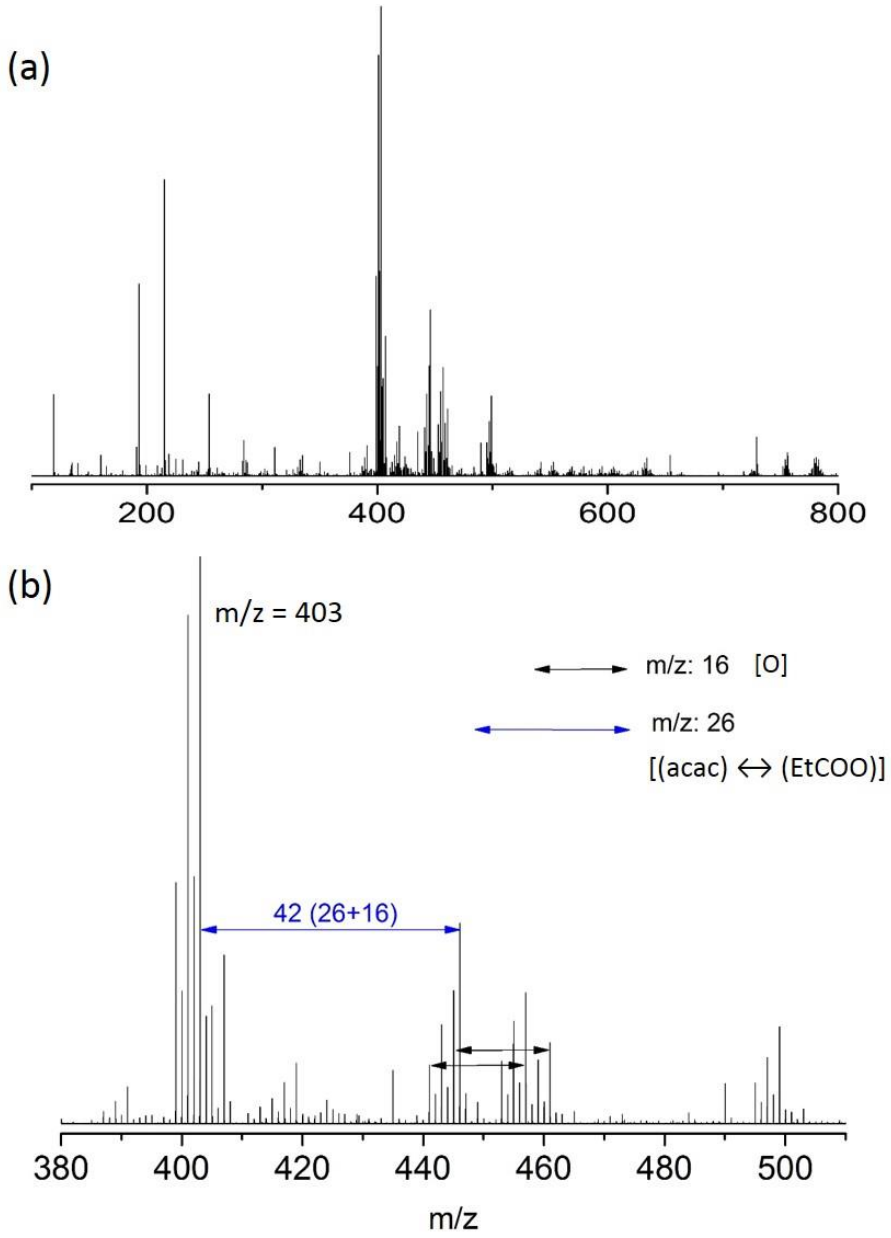


Figure 2-7. CSI-FT-ICR-MS analysis of the Sn solution. (a) The spectrum of the whole measured m/z range. (b) Expanded spectrum of panel (a) in the range of m/z = 380 – 510. The peak intervals and the corresponding ligand change are indicated.

The oxygen and hydrogen were supposed to be presented in the Sn multimers. An estimation of structure of the Sn multimers in the Sn solution is shown in Table 2-1. The Sn multimers was estimated to be in structure of $SnO_aH_b(EtCOO)_c(acac)_d$, where a, b, c, and d are integers. It was suggested that the organic molecular such as EtCOO and acac coordinated to SnO_a multimer.

Table 2-1 Estimation of structure of the Sn multimers in the Sn solution.

Exp. MS	Metal	Ligand	Oxygen	Cal. MS
401	Sn_1	$(EtCOO)_3$	O_4	401
403	Sn_1	$(EtCOO)_3$	O_4	401(+2H)
446	Sn_1	$(acac)_1(EtCOO)_2$	O_5	443 (+3H)
461	Sn_1	$(acac)_1(EtCOO)_2$	O_6	459 (+2H)

EtCOO = C_2H_5COO,

b. FT-IR analysis

Molecular structure of the Sn solution during drying process at room temperature and 100 ^oC was investigated by FT-IR measurement. FT-IR spectrum of the Sn solution was shown in Figure 2-8 (a), which is similar to that of the solvent propionic acid (PrA). Figure 2-8 (b) shows FT-IR spectra of Sn solution dried at RT and 100 ^oC. These samples were prepared by dropping the solution with a volume of 30 μl on undoped Si substrates and then drying. For the sample dried at RT, the solvent PrA was completely evaporated after 10 min. Therefore obtained product was due to the aggregation of the solute in the Sn solution. As can be seen from the FT-IR spectrum of the RT dried sample, we can observe the absorbance peak

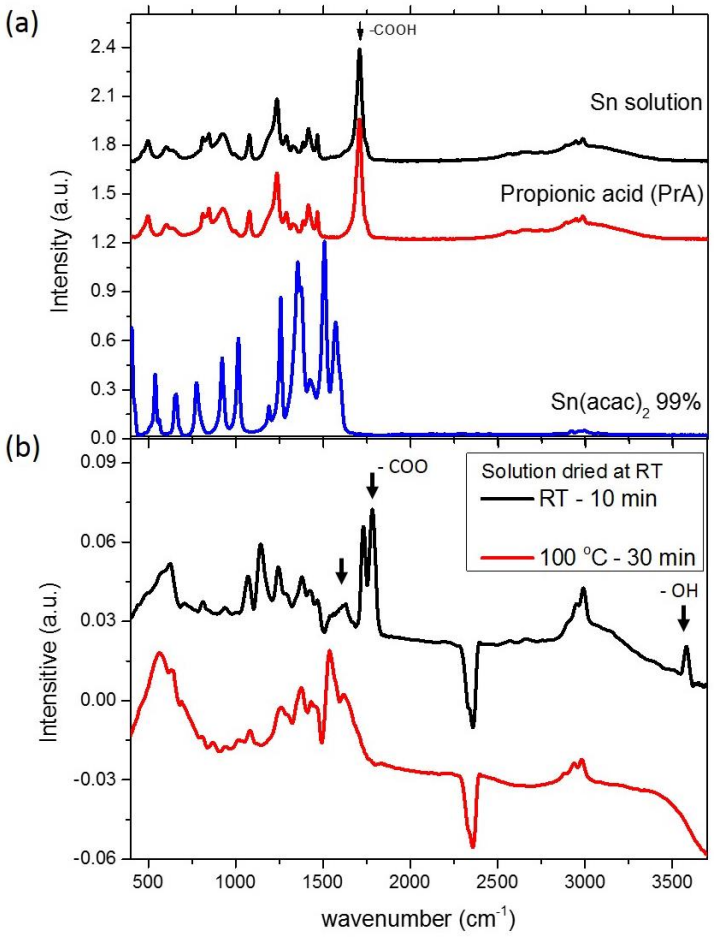


Figure 2-8. FT-IR spectra for (a) the starting compound of Sn ($Sn(acac)_2$), the solvent Propionic acid (PrA), and Sn solution; (b) Sn solution dried at RT for 10 min and at 100 ^oC for 30 min

corresponding to –COOH and –OH vibration (around 1730 cm^{-1} and 3500 cm^{-1}, respectively). This indicates the existence of the PrA, which was estimated from the mass spectrometric results and water molecules in the solute of the Sn solution. When the solution was dried at 100 ^oC, the –COOH and -OH peaks were significantly decreased. It was considered that PrA components and water molecules were removed from the Sn multimers.

c. Modelling structure of the Sn multimers_Sn clusters

Figure 2-9 shows the schematic and calculated atomic models of the Sn clusters in the Sn solution. Based on the results achieved by mass spectrometric and FT-IR measurement, we supposed that the Sn clusters in the Sn solution was the coupling

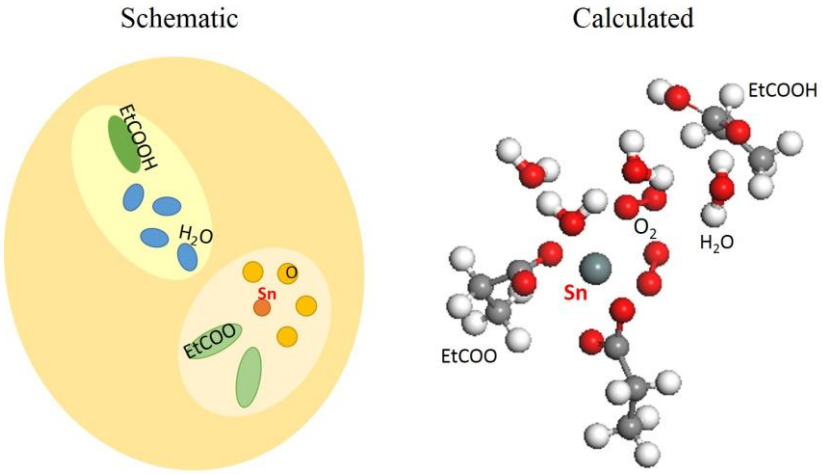


Figure 2-9. The schematic and calculated atomic model of the Sn cluster in the Sn solution. Atomic model was calculated by the first-principles molecular-dynamics simulation.

of two type materials: one is the organic cluster including propionic acid (EtCOOH) and water molecules, the other is comprising Sn, oxygen, water and EtCOO molecules. It was assumed that the cluster consists a $SnO_4(EtCOO)_2(H_2O)_4EtCOOH$ configuration. For the former cluster, the EtCOOH are bound to water molecules by hydrogen bonds. In addition, due to long-range interaction with the Sn atom, thermal energy at temperature of 100 ^oC could be enough to break the hydrogen bonding between EtCOOH and the water molecules near EtCOOH. The removing of EtCOOH and water molecule from the clusters was confirmed by FT-IR result shown in Figure 2-8 (b).

Figure 2-10 shows comparison in the FT-IR the Sn solution dried at RT for 10 min and FT-IR spectrum obtained by first-principle calculation for the clusters with structure of $SnO_4(EtCOO)_2(H_2O)_4EtCOOH$. Although there is a shifting to lower wavenumbers, the calculated FT-IR spectral shape is rather consistence with experimental FT-IR result.

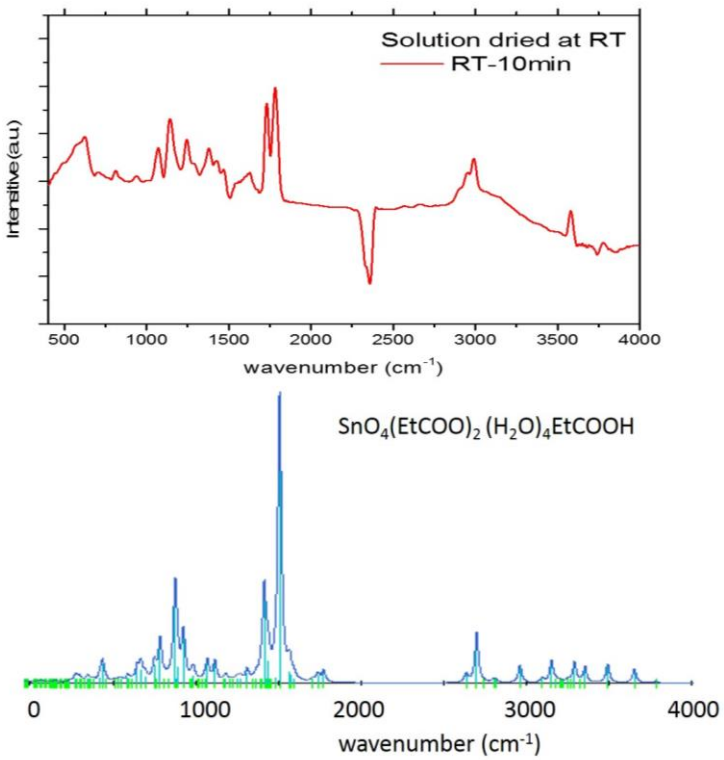


Figure 2-10. Comparison of FT-IR spectrum of Sn solution dried at RT and FT-IR spectrum obtained by first-principle calculation for cluster with structure of $SnO_4(EtCOO)_2(H_2O)_4EtCOOH$

2.3.4.2 The solute of the Sn:PPC solution

Figure 2-11 (a) and (b) show the mass spectrometric results in positive-mode measurements of the solute in the Sn:PPC solution. Since molecular weight of PPC is over limitation of the CSI-FT-ICR-MS system (m/z = 5000), molecules of PPC could not detected. The very high intensity peaks at m/z = 177, 199 and 375 in Figure 2-11 (a) correspond to the solvent DEGMA of the PPC solution. Figure 2-11 (b) shows the expanded spectrum of panel (a) in the range of m/z = 200– 350. It was confirmed that the peaks at m/z = 273 and 309 from the molecules including Sn. Table 2-2 shows an estimation of structure of the Sn multimers in the Sn:PPC solution. It seems that the Sn multimers in the PPC solution existed in the same configuration of the Sn multimers in the Sn solution. However, it is still not clear whether there is an effect of PPC molecules in the change in structure of Sn clusters or not. I supposed that in the Sn:PPC solution the Sn clusters was coordinated with the large PPC molecules.

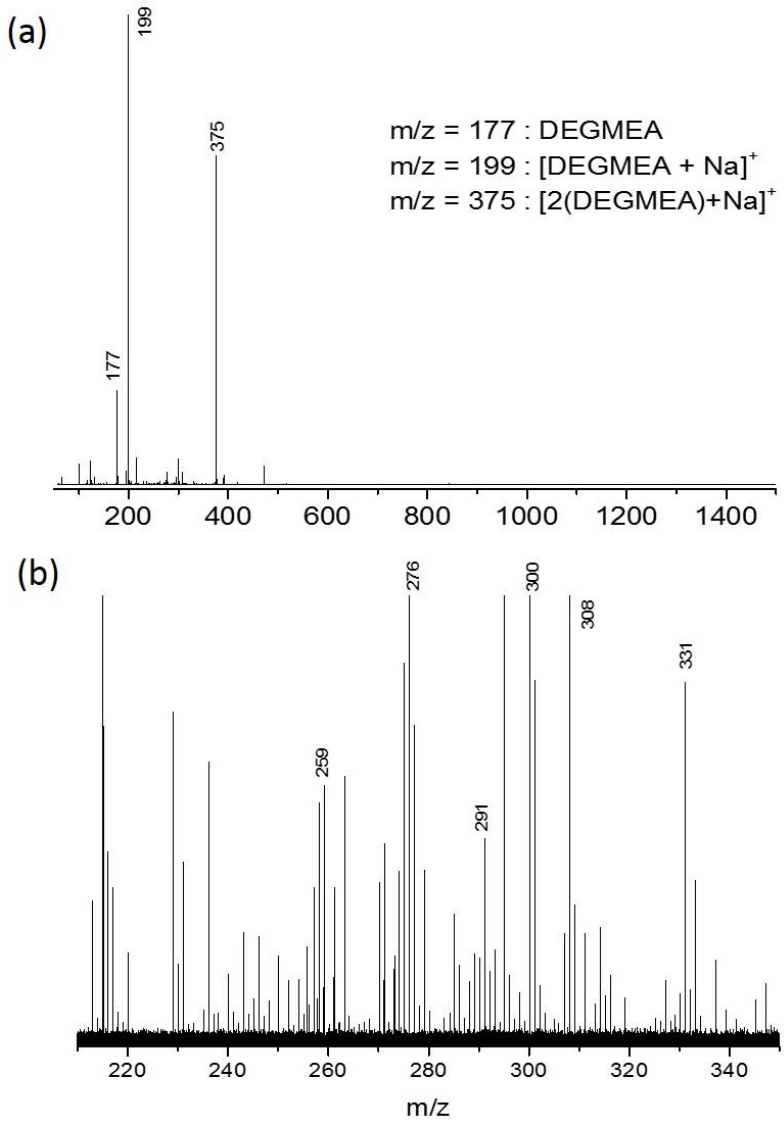


Figure 2-11. CSI-FT-ICR-MS analysis of the Sn:PPC solution. (a) The spectrum of the whole measured m/z range. (b) Expanded spectrum of panel (a) in the range of m/z = 200– 350.

Table 2-2 Estimation of structure of the Sn multimers in the Sn:PPC solution.

Exp. MS	Metal	Ligand	Oxygen	Cal. MS
273	Sn_1	$(EtCOO)_1$	O_5	271 (+2H)
308	Sn_1	$(acac)_1(EtCOO)_1$	O_1	306 (+2H)

EtCOO = C_2H_5COO,

2.4 Conclusion

The Sn:PPC solution was selected as doping material for source and drain region of the ZrInZnO self-aligned TFT. The Sn:PPC solution is a mixture of the Sn solution and PPC solution. The structure of solute in the Sn and Sn:PPC solution was investigated by using mass spectrometric, FT-IR analysis, the first principles molecular dynamics simulation. It was found that the solute in the Sn solution was in a configuration of coordinated PrA ligand, water and oxygen around the Sn atom, so called Sn multimers or Sn cluster. For the Sn:PPC solution, we supposed that the solute was in an configuration with coordination of large PPC molecules with Sn clusters that is in the same configuration of one in the Sn solution. These obtained results can help to clarify the mechanism of Sn diffusion during doping process.

Reference

[1] J. Park, I. Song, S. Kim, S. Kim, C. Kim, J. Lee, H. Lee, E. Lee, H. Yin, K. –K. Kim, K. –W. Kwon, and Y. Park, *Appl. Phys. Lett.*, 2008, 93, 053501.

[2] Z. Ye, L Lu, and M. Wong, "Zinc-Oxide Thin-Film Transistor With Self-Aligned Source/Drain Regions Doped With Implanted Boron for Enhanced Thermal Stability," *IEEE Trans. Electron Devices*, vol. 59, pp. 393, 2012.

[3] R. Chen, W Zhou, M Zhang, M Wong, and H-S Kwok, "Self-Aligned Indium–Gallium–Zinc Oxide Thin-Film Transistor with Phosphorus-Doped Source/Drain Regions," *IEEE Electron Device Lett.*, vol. 33, pp. 1150, 2012.

[4] R. Chen, W Zhou, M Zhang, M Wong, and H-S Kwok, "Self-Aligned Indium–Gallium–Zinc Oxide Thin-Film Transistor With Source/Drain Regions Doped by Implanted Arsenic," *IEEE Electron Device Lett.*, vol. **34**, pp. 60, 2013.

[5] C. –H. Wu, H. –H Hsieh, C. –W. Chien, and C. –C. Wu, *J. Display Technol.*, 2009, 5, 515.

[6] N. Morosawa, Y. Ohshima, M. Morooka, T. Arai and T. Sasaoka, *Jpn. J. Appl. Phys.* 2011, 50, 096502.

[7] J. Jiang, M. Furuta, and D. Wang, *IEEE Electron Device Lett.* 2014, 35, 933.

[8] D. H. Kang, I. Kang, S. H. Ryu, and J. Jang, "Self-Aligned Coplanar a-IGZO TFTs and Application to High-Speed Circuits," *IEEE Electron Device Lett.*, vol. 32, pp. 1385, 2011.

[9] X.H. Li, Y.Z. Meng, Q. Zhu and S.C. Tjong, "Thermal decomposition characteristics of poly(propylene carbonate) using TG/IR and Py-GC/MS techniques", *Polymer Degradation and Stability*, vol. 81, pp 157, 2003.

Chapter 3

Fabrication of Sn-doped ZrInZnO by the Sn:PPC solution

3.1. Introduction

In previous chapter, the characteristics of the Sn:PPC solution was reported. It was indicated that the Sn:PPC solution can be applied for self-aligned process. The utilization of PPC prevents the formation of SnO_x film between source and drain regions of the self-aligned TFT. This chapter describes in detail the fabrication of high conductive ZrInZnO by using the Sn:PPC solution.

3.2 Experimental procedure

3.2.1 Sample preparation

3.2.1.1 ZrInZnO film

In this study, the ZrInZnO was fabricated by using solution process. The ZrInZnO precursor solution with the concentration of 0.2 mol/kg was synthesized by blending 0.2 mol/kg of zinc chloride [$ZnCl_2$] (Kanto Chemical) dissolved in 2-methoxyethanol with 0.2 mol/kg of indium(III) acetylacetonate [$In(OCCH_3CHOCCH_3)_3$] (Sigma-Aldrich) and zirconium(IV) butoxide [$Zr(OC_4H_9)_4$] (Sigma-Aldrich) dissolved in propionic acid. The atomic ratio of Zr:In:Zn was 0.1:2:1. To form a 40-nm-thick ZrInZnO film the ZrInZnO solution was spin-coated onto a SiO2/Si substrate twice at 3000 rpm for 30 s and annealed by the rapid thermal annealing (RTA) at 500 °C for 10 min in ambient oxygen [1], [2].

3.2.1.2 Doping solution _ Sn:PPC solution

The doping solution_ Sn:PPC solution was synthesized by mixing a PPC solution with a Sn solution. The PPC solution containing 6 wt% PPC was prepared by dissolving purified PPC (Sumitomo Seika Chemicals) in diethylene glycol monoethyl ether acetate (DEGMEA) (Tokyo Chemicals Industry). For the synthesis of the Sn solution, tin acetyl acetonate ($Sn(Acac)_2$) [$Sn(OCCH_3CHOCCH_3)_2$] (Sigma-Aldrich) was dissolved in propionic acid (Kanto Chemical). Concentration of the Sn solution was 0.2 mol/kg. The tin content in the doping solution was controlled by varying the mixing ratio of the Sn solution to the PPC solution. The Sn:PPC solutions were prepared with different weight ratio of [Sn solution] : [PPC solution]. For example, the Sn:PPC solution 10 means a solution with weight ratio of [Sn solution] : [PPC solution] = 10:100 or the Sn:PPC solution 2 means a solution with weight ratio of [Sn solution] : [PPC solution] = 2:100.

3.2.1.3 Doping process

To dope the ZrInZnO film the Sn:PPC solution was spin-coated onto the ZrInZnO film at 1500 rpm for 25 s , and the samples were subsequently dried at 180 °C for 30 min and annealed by RTA at various temperatures from 300 to 600 ^oC under different ambiences, including N_2, O_2, air and vacuum.

3.2.2 Film characterization

Resistivity values of the Sn-doped ZrInZnO films were measured by four-probe method (Loresta AX Mitsubishi Chemical Co. Ltd.). Depth profile of Sn-doped ZrInZnO film was characterized by the auger electron spectroscopy (AES). Thermal desorption spectroscopy (TDS) was used to monitor desorption of components from the ZrInZnO films.

3.3 Results and discussion

3.3.1 Effect of content of Sn in the Sn:PPC solution in resistivity of Sn-doped ZrInZnO

Figure 3-1 reports the resistivity of the 40 nm ZrInZnO films after being treated by the Sn:PPC solutions from 1 to 20 . The Sn:PPC solution spin-coated on the ZrInZnO film and annealed at 400 ºC for 10 min under ambient N_2. As can be seen in this figure, before being treated by the Sn:PPC solution the ZrInZnO film, fabricated by solution process, had a very high resistivity around 4×10^3 Ω cm. However, the resistivity of the ZrInZnO film was reduced dramatically to 4.1×10^{-2} Ω cm after the film was treated by the Sn:PPC solution 2. When the concentration of Sn solution in the Sn:PPC solution increased to 5, the resistivity of the ZrInZnO film

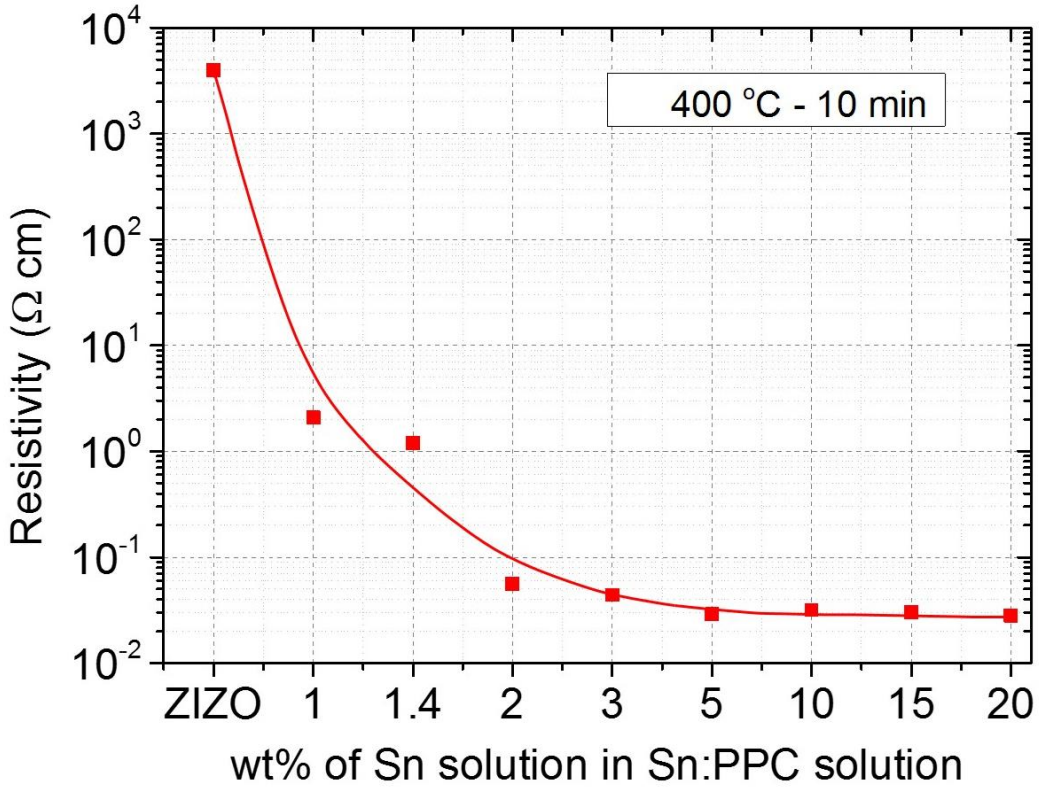


Figure 3-1. Dependence of resistivity on the concentration of Sn solution in the Sn:PPC solution for the 40 nm ZrInZnO film.

slowly decreased to 2.7 × 10^{-2} Ω cm. After that it did not change further and stayed constant.

3.3.2 Effect of annealing temperature and annealing time on resistivity of Sn-doped ZrInZnO

Figure 3-2 shows the effect of annealing temperature on the resistivity of the ZrInZnO film treated by the Sn:PPC solution 10. As shown in this figure, when the sample was annealed at 300 °C the resistivity of the ZrInZnO film reached to about 1.8 × 10^{-2} Ω cm. At annealing temperatures of over 300 °C, the resistivity of the film slowly increased. For the sample annealed at 600 °C the resistivity was dramatically increased to 1.2 x 10^{2} Ω cm. It was supposed that the significant increase in resistivity of this sample resulted from a change in characteristics of the ZrInZnO film. To confirm this supposition we executed thermal gravimetry (TG) measurement for a

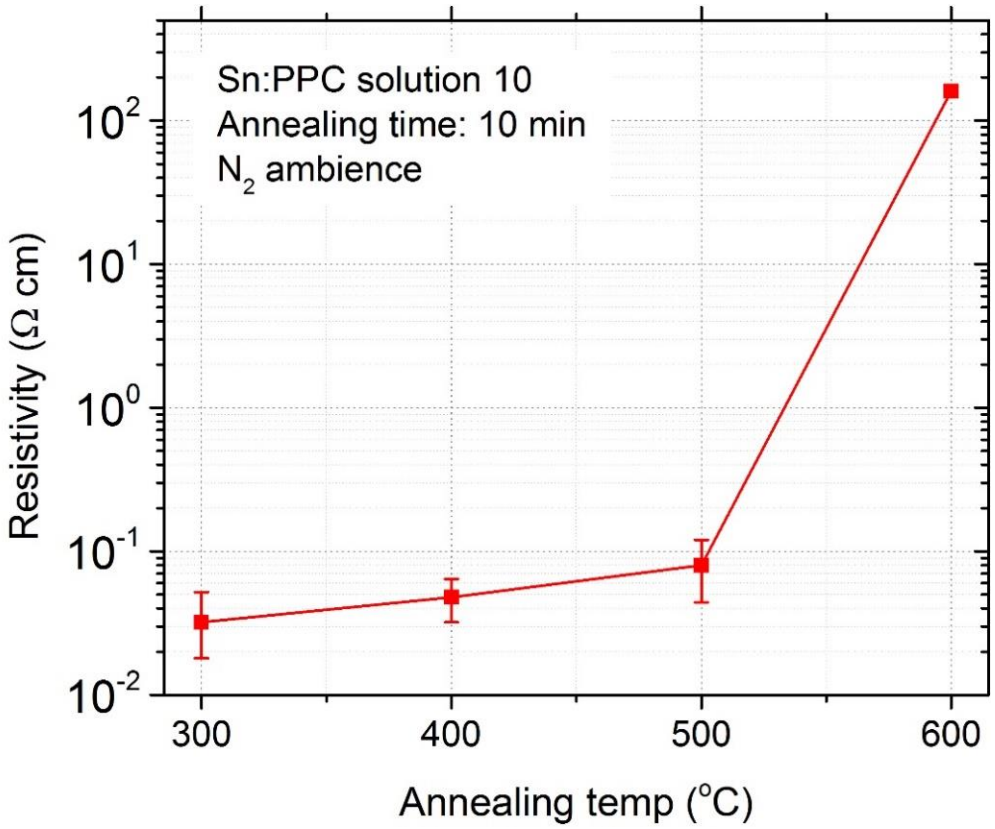


Figure 3-2. Dependence of resistivity on annealing temperature for the 40 nm ZrInZnO film coated by the Sn:PPC solution 10

ZrInZnO gel. For preparation of the ZrInZnO gel, the ZrInZnO solution was dropped on a glass substrate and then dried at 250 ºC for 5 min. Since most solvent propionic

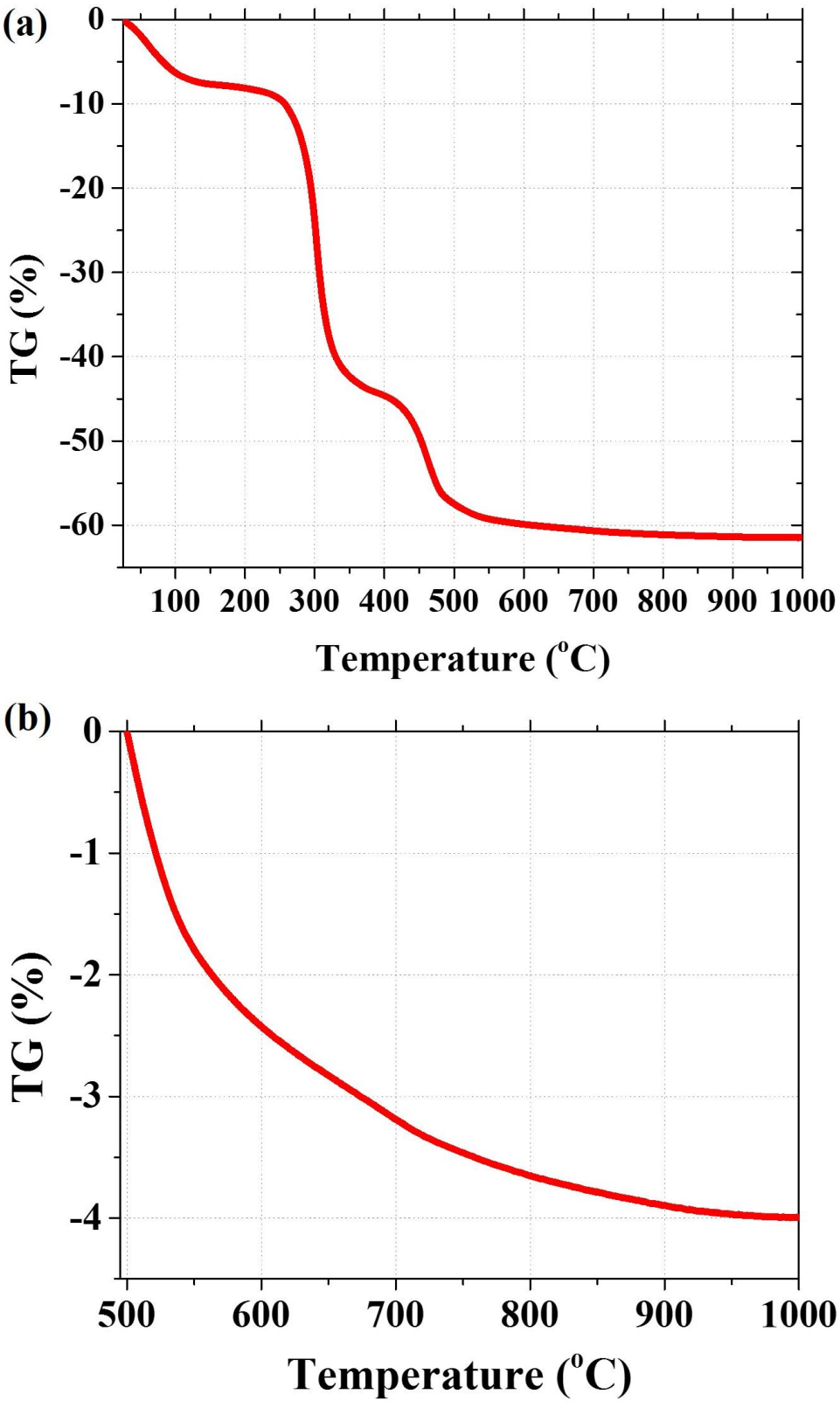


Figure 3-3. Thermal gravimetry analysis of ZrInZnO gel

acid was evaporated, we obtained the ZrInZnO gel and evaluated accurately thermal decomposition process of the ZrInZnO film only. The weight loss of the ZrInZnO gel at the temperature from 25 °C to 1000 °C under ambient nitrogen is shown in Figure 3-3 (a). From the TG curve, a slow weight loss was observed for temperature above 500 °C. The weight loss percentage of the ZrInZnO at temperature from 500 °C to 1000 °C is indicated in the Figure 3-3 (b). As can be seen from this curve at around 600 °C the weight loss is about 2.5 %. We assumed that this weight loss results from C components released. Figure 3-4 displays TDS results for CO_2, Sn, SnO and SnO_2 desorbed from the ZrInZnO film coated by Sn:PPC solution and dried at 180 °C for 30 min. A desorption peak of CO_2 was observed at the temperature around 510 °C. This result agrees with our supposition for CO_2 released from the ZrInZnO film. The remove of CO_2 from the ZrInZnO film results in a change in structural characteristics

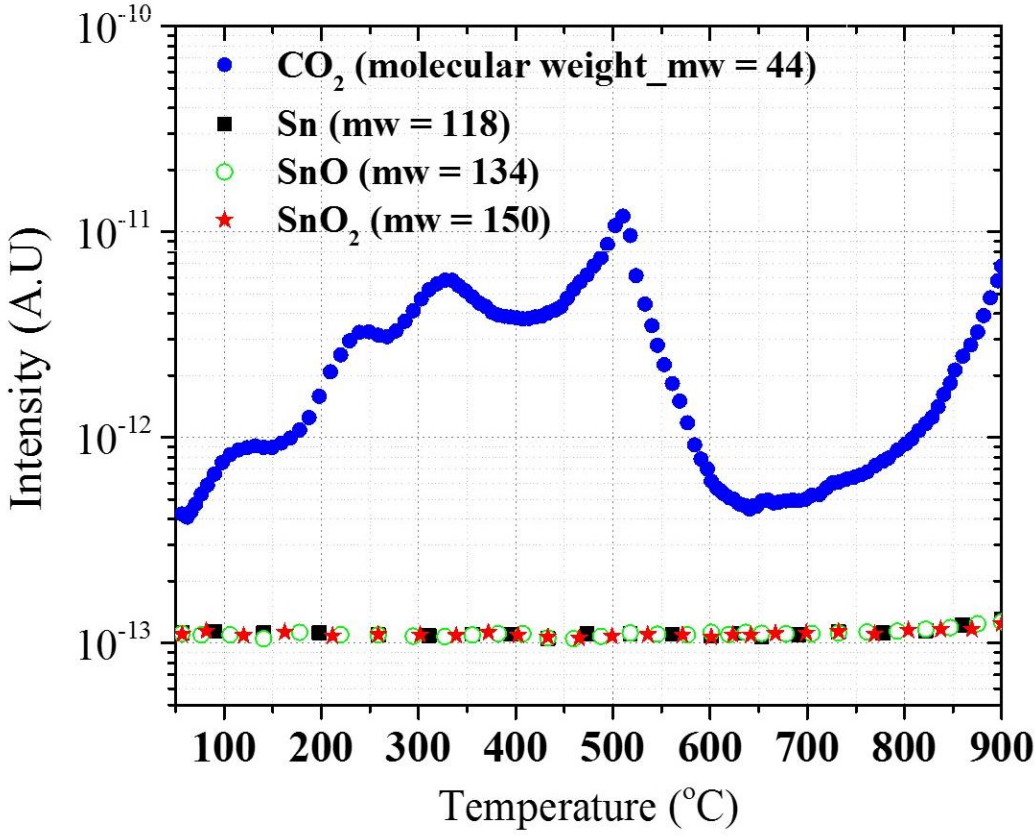


Figure 3-4. TDS spectra of CO_2 (molecular weight_mw = 44), Sn (mw = 118), SnO (mw = 134) and SnO_2 (mw = 150) of the ZrInZnO film coated by Sn:PPC solution and dried at 180 °C for 30 min.

of the ZnInZnO film, which leads to a dramatic increase in resistivity. We did not observe any desorption peak of Sn, SnO and SnO_2 from the ZnInZnO film when temperature increased up to 900 ^oC. This means that tin out-diffusion effect, which is considered as a reason for reducing conductivity of the sample did not occur. From these results, we can conclude that the significant increase in resistivity of the 600 ^oC treated sample was due to the change in structure characteristic of the ZrInZnO film.

The dependence of the resistivity on annealing time of the ZrInZnO film treated by the Sn:PPC solution was shown in Figure 3-5. These samples were annealed at 300 ^oC under ambient N_2. The resistivity of the ZrInZnO film increased gradually from 1.8×10^{-2} Ω.cm to 1.4×10^{-1} Ωcm as the annealing time was increased from 10 to 120 min.

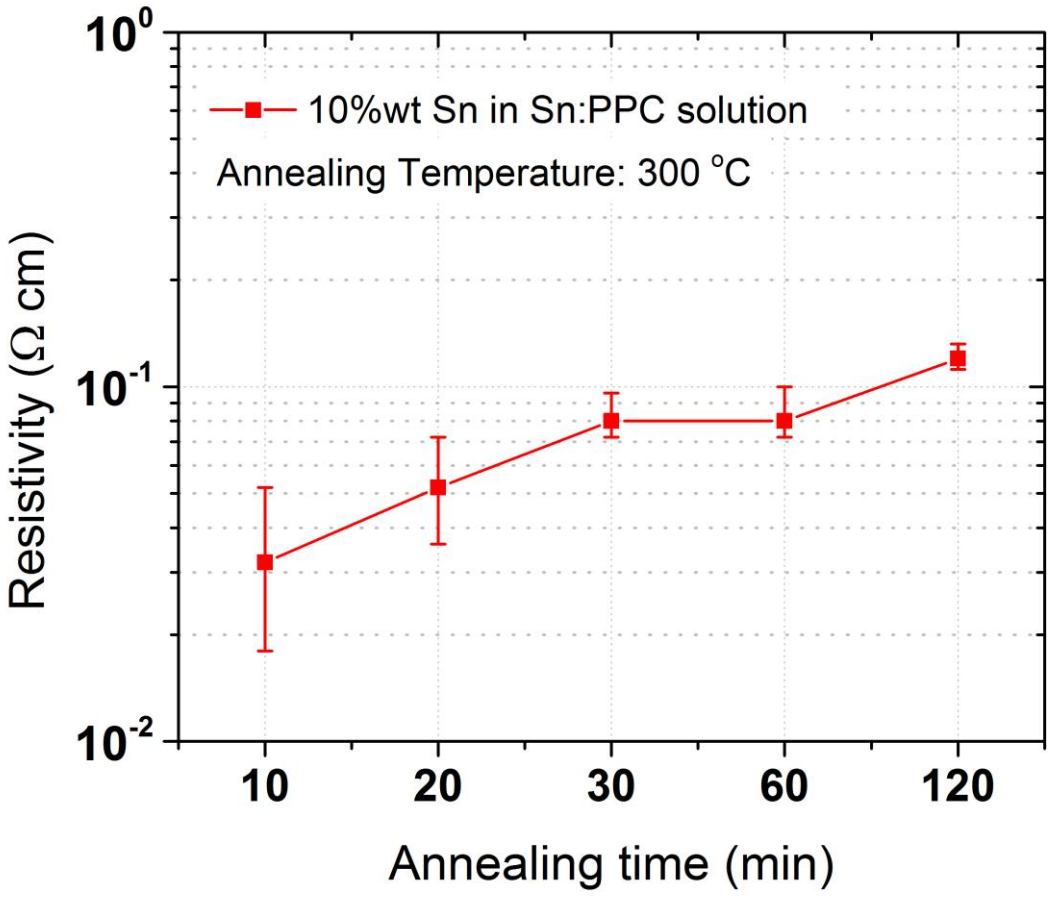


Figure 3-3. Dependence of resistivity on annealing time for the 40 nm ZrInZnO film coated by the Sn:PPC solution 10

3.3.3 Effect of annealing ambience on resistivity of Sn-doped ZrInZnO

The influence of the annealing ambience on the resistivity of the ZrInZnO film treated by the Sn:PPC solution was studied. Figure 3-5 shows the dependence of a resistivity on the annealing ambience, including vacuum, N_2, air and O_2. These samples were annealed at 300 ^oC for 10 min. It is apparent that the change in annealing ambience induced a corresponding change in resistivity. For the sample annealed under vacuum the resistivity of the ZrInZnO film was reduced sharply to ~1.6 × 10^{-2} Ω cm. This value was about 10^3 times lower than that obtained after annealing in air and oxygen ambience. Although vacuum ambience had a good effect on reducing resistivity of the film, nitrogen ambience was selected to use in this work based on our objective of eliminating the vacuum process.

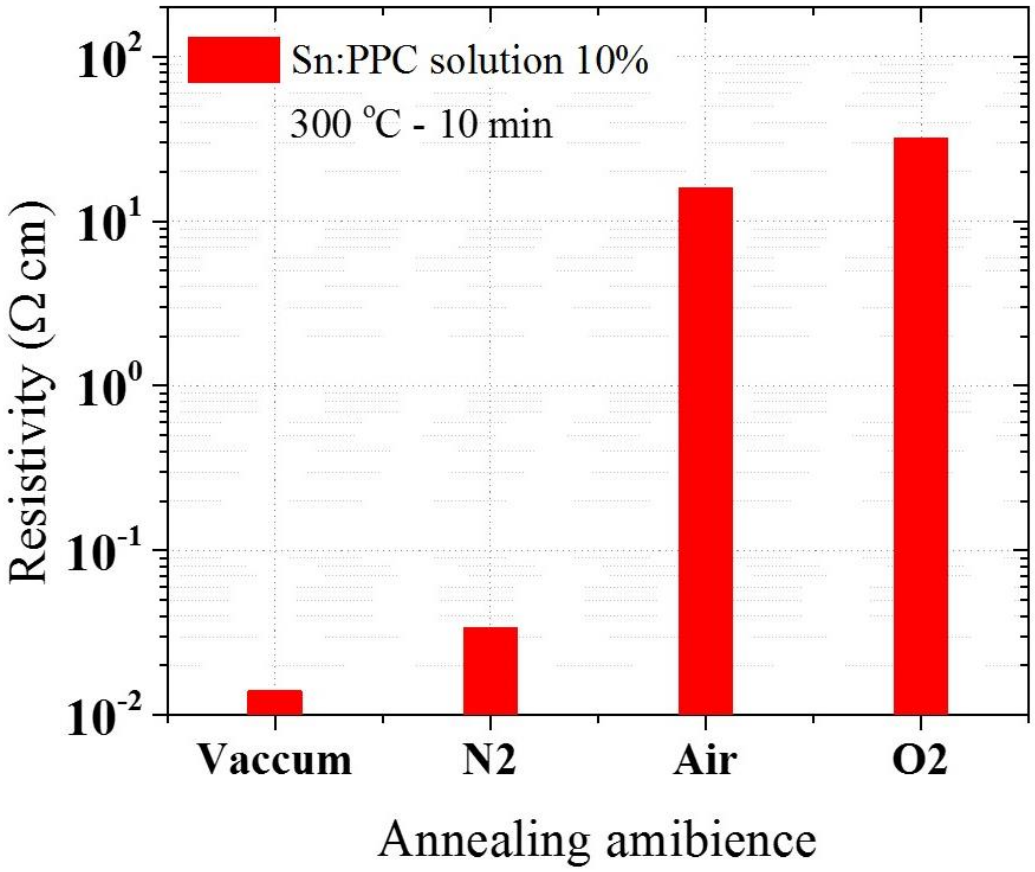


Figure 3-5. Influences of annealing ambience on resistivity of the 40 nm ZrInZnO film coated by the Sn:PPC solution 10

These results demonstrate that the ZrInZnO semiconductor becomes metallic after being treated by the Sn:PPC solution, which have a good effect at the annealing temperature of 300 °C for 10 min under ambience without oxygen. Although resistivity of the obtained ZrInZnO film in this study was about 4 times higher than that of the IGZO film treated by the vacuum method, such as Ar plasma [3], NH_3 plasma [4], hydrogen diffusion [5] and aluminum diffusion [6], it can be applied to fabricate the self-aligned TFT.

3.3.4 Depth profile of Sn-doped ZrInZnO

It was supposed that Sn was diffused into the ZrInZnO film during an annealing process. Sn acts as a donor in a ZrInZnO film, resulting in an increase in the conductivity of the S/D regions. In order to confirm that Sn diffused into the ZrInZnO film, Auger electron spectroscopy was performed. Figure 3-6 shows the depth profile of Sn and oxygen in a 40-nm-thick ZrInZnO film after the film had been spin-coated

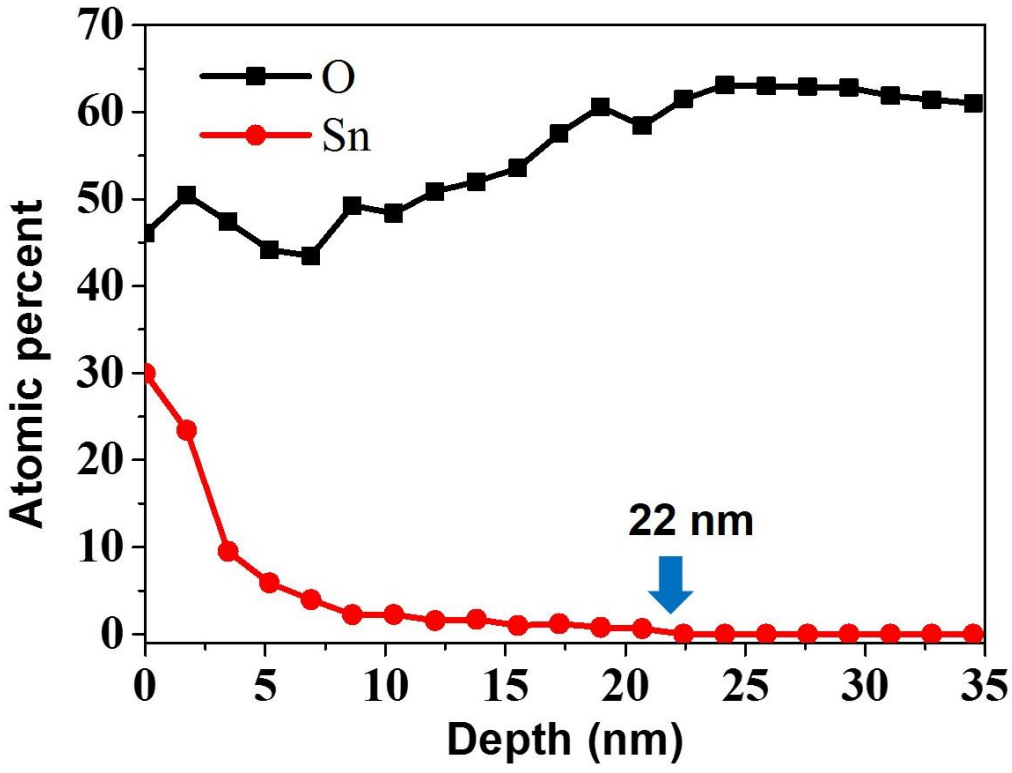


Figure 3-6. Atomic depth profile of Sn and O in a 40-nm-thick ZrInZnO film spin-coated with Sn:PPC solution 10 and annealed at 400 °C for 20 min

with the Sn:PPC solution 10 and annealed at 400 °C for 20 min under N_2 ambience. The results show that Sn diffused into the ZrInZnO film to a depth of 22 nm. Thus, we propose that Sn acts as a donor in ZrInZnO, resulting in an increase in the conductivity of the ZrInZnO film.

3.4 Conclusion

The Sn:PPC solution was used to fabricated high conductivity ZrInZnO for source and drain regions of self-aligned TFT. The Sn:PPC solution was coated and annealed to make Sn diffuse into the ZrInZnO film. It was confirmed that Sn diffused into ZrInZnO film to a depth of 22 nm. Sn acts as a donor in ZrInZnO, which results in an increase in the conductivity of the ZrInZnO film. It was confirmed that resistivity of the Sn-diffused ZrInZnO was reduced to 1.8×10^{-2} Ω cm at annealing temperature of 300 ^{o}C when the Sn:PPC solution was used. The increase in resistivity of the sample annealed at temperature over 500 ^{o}C was due to the change in structure characteristic of the ZrInZnO film. To make high conductive ZrInZnO the ambience with oxygen should be avoided.

Reference

[1] P. T. Tue, T. Miyasako, J. Li, H. T. C. Tu, S. Inoue, E. Tokumitsu, and T. Shimoda, “High-performance solution-processed ZrInZnO thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 60, pp. 320, 2013.

[2] H. T. C. Tu, S. Inoue, P. T. Tue, T. Miyasako, and T. Shimoda, “Investigation of Polysilazane-Based SiO_2 Gate Insulator for Oxide Semiconductor Thin-Film Transistors,” *IEEE Trans. Electron Devices*, vol. 60, pp. 1149, 2013.

[3] J. Park, I. Song, S. Kim, S. Kim, C. Kim, J. Lee, H. Lee, E. Lee, H. Yin, K. –K. Kim, K. –W. Kwon, and Y. Park, *Appl. Phys. Lett.*, 2008, 93, 053501.

[4] S. Kim, J. Park, C. Kim, I. Song, S. Kim, S. Park, H. Yin, H.-I. Lee, E. Lee, and Y. Park, *IEEE Electron Device Lett.* 2009, 30, 374.

[5] A. Sato, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, *Appl. Phys. Lett.*, 2009, 94, 133502.

[6] N. Morosawa, Y. Ohshima, M. Morooka, T. Arai and T. Sasaoka, *Jpn. J. Appl. Phys.* 2011, 50, 096502.

Chapter 4

Fabrication and characterization of self-aligned ZrInZnO TFT with source and drain regions doped by Sn:PPC solution

4.1 Introduction

In previous chapter, I reported on the using of the Sn:PPC solution to perform the diffusion of Sn into the ZrInZnO film , which resulted in a substantial reduction in the resistivity of the ZrInZnO film. Particularly, the resistivity of the Sn-diffused ZrInZnO film decreased to 1.8×10^{-2} Ω cm. This result indicate a potential application of the Sn:PPC solution in fabrication of source/drain regions (S/D regions) of the self-aligned ZrInZnO TFT. This chapter describes the fabrication and characterization of self-aligned ZrInZnO TFTs with source and drain (S/D) regions doped by the Sn:PPC solution.

4.2 Experimental procedure

The self-aligned top-gate ZrInZnO TFT with S/D regions doped by the Sn:PPC solution fabricated in this study is shown schematically in Figure 4-1.

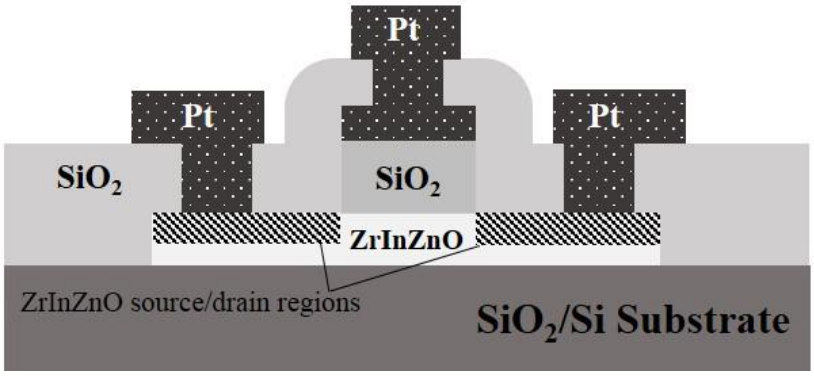


Figure 4-1. Schematic cross-section of a self-aligned top-gate ZrInZnO TFT with S/D regions doped by the Sn:PPC solution

All steps for fabrication of the self-aligned top gate ZrInZnO TFT are described as follows.

Step 1: *Cutting SiO_2/Si Substrate and cleaning*

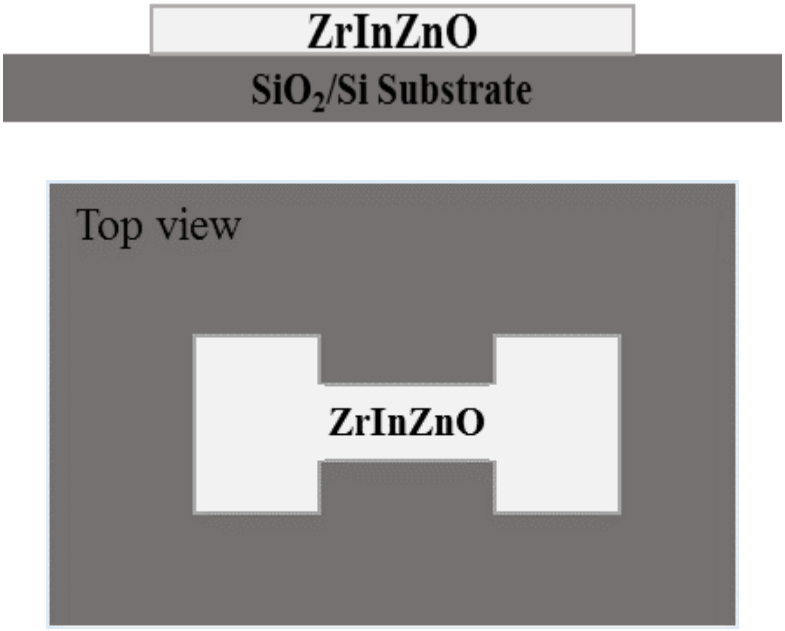
A SiO_2 (500 nm)/Si substrate with 2 cm × 2 cm in size was cut by a diamond pen from the commercial 4-inch SiO_2/Si wafer. After that, the substrate was cleaned by ultrasonic agitation in acetone for 5 min and rinsed with running deionized water followed by air blowing. Then, it was dried at 100 ^oC for 1 min by hotplate. In order to remove organic contaminants on the substrate surface, O_2 plasma ashing (15 W, O_2 flowing rate 30 sccm, 3 min) was performed.

Step 2: *Deposition of ZrInZnO film*

A 40-nm ZrInZnO film was deposited by spin-coating the ZrInZnO solution onto the SiO_2/ Si substrate twice at 3000 rpm for 30 s and subsequently annealing at 500 °C for 10 min under oxygen ambience.

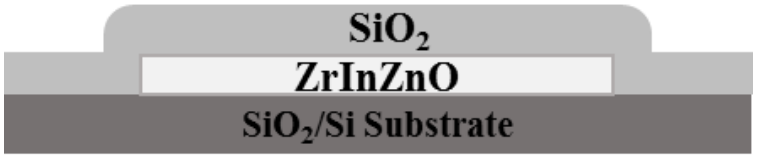
Step 3*: Patterning ZrInZnO*

To form the ZrInZnO channel pattern, OMR-85 resist patterns were formed on the ZrInZnO film. Then an inductively coupled plasma etching at 80-W ICP power, 16-W RF power, and 50 sccm in Ar for 15 min was performed to etch away the ZrInZnO outside the OMR-85 patterns. The OMR-85 resist was removed by O_2 plasma ashing (50 W, O_2 flowing rate 30 sccm, 5 min).



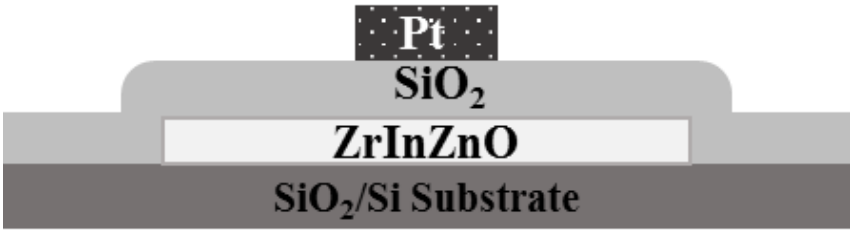
Step 4: *Deposition of SiO2 gate insulator*

A 115~120-nm-thick SiO_2 layer as gate insulator was deposited on top of the ZrInZnO layer by spin-coating polysilazane solution and then wet-annealing at 450 °C for 2 h.



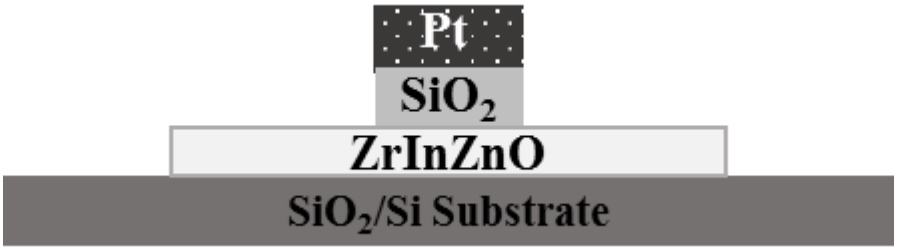
Step 5: *Deposition of Pt gate electrode*

A 130-nm thick Pt film was deposited via radio-frequency (RF) sputtering in Ar gas at 3×10^{-3} Pa at 100 ^{o}C and patterned for a gate electrode by a lift-off technique.



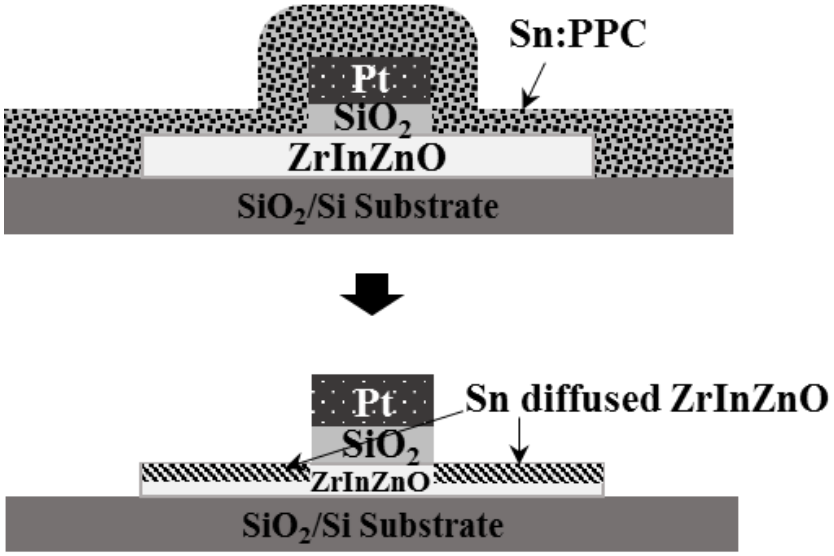
Step 6: *Etching SiO2 gate insulator*

In order to expose ZrInZnO source and drain regions for the TFT, a plasma CF_4 etching was performed to remove away the SiO_2 outside Pt gate electrode. At this stage, the Pt gate electrode acts as a mask.



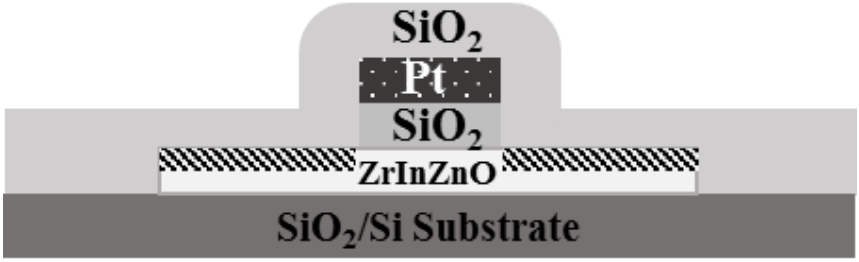
Step 7: *Doping the ZrInZnO*

To dope the ZrInZnO source and drain regions, the Sn:PPC solution 10 was spin-coated and annealed at 400 °C for 20 min. During this process, PPC was decomposed to H_2O and CO_2, and tin was diffused into the ZrInZnO, thereby resulting in the formation of a doped source and drain.



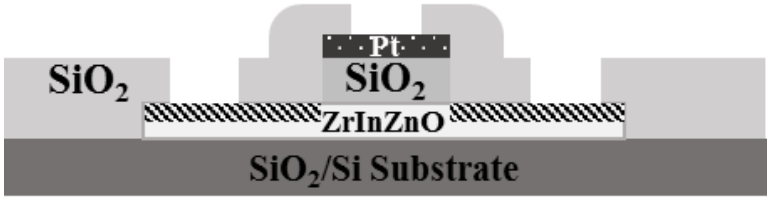
Step 8: *Deposition of SiO2 passivation layer*

The 115~120-nm polysilazane-derived SiO_2 was deposited again for source/drain passivation. The film was annealed at 450 °C for 2 h.



Step 9: *Etching SiO2 passivation layer for opening contact hole*

Contact holes to the ZrInZnO source and drain regions were opened by a plasma CF_4 etching.



Step 10: *Depositing and patterning source/drain and gate contact*

A 130-nm thick Pt used as source/drain and gate contact was first sputtered in Ar gas at 3×10^{-3} Pa at 100 ^{o}C and then patterned by lift-off technique.

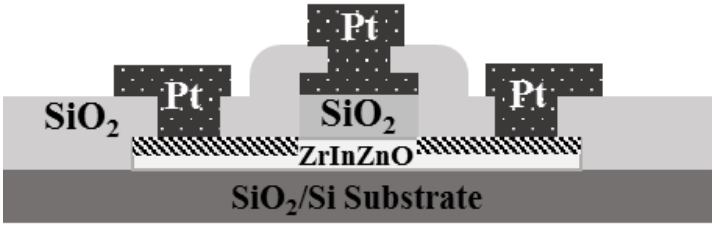


Figure 4-2 shows an optical microscopy image of the fabricated self-aligned TFT with a channel length and width of 20 µm and 60 µm, respectively.

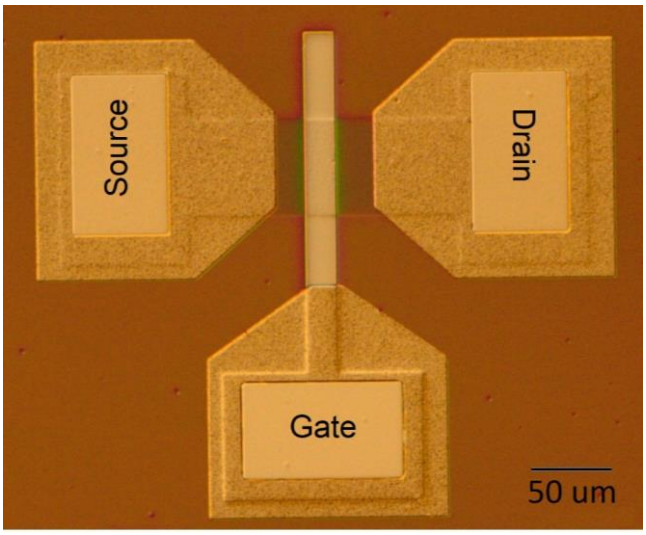


Figure 4-2. Optical microscopy image of a self-aligned TFT with a channel length and width of 20 µm and 60 µm, respectively.

The transfer and output characteristics of the TFTs were measured using a semiconductor parameter analyzer (Agilent 4155C).

4.3 Results and discussion

4.3.1 Effect of plasma CF4 etching on ZrInZnO

In this study, SiO_2 was used as the gate insulator of the self-aligned ZrInZnO TFT. To remove away the SiO_2 outside Pt gate electrode (in fabrication step 6), I used the plasma CF_4 etching. In this process over etching could not avoid, which may be affect resistivity of the ZrInZnO. It was reported that during plasma treatment of IGZO, due to ion bombardment the relative weak In-O bonds are preferentially broken and then In atoms collect near the surface of the film. This leads to a reduction in resistivity of IGZO [1]. Therefore, effect of plasma CF_4 etching on resistivity of the ZrInZnO should be confirmed. Figure 4-3 shows resistivity of the 40 nm thick-ZrInZnO after being exposure in CF_4 plasma for a period of time from 30 s to 3 min. As can be seen, resistivity of the plasma CF_4 treated ZrInZnO is still as same as that

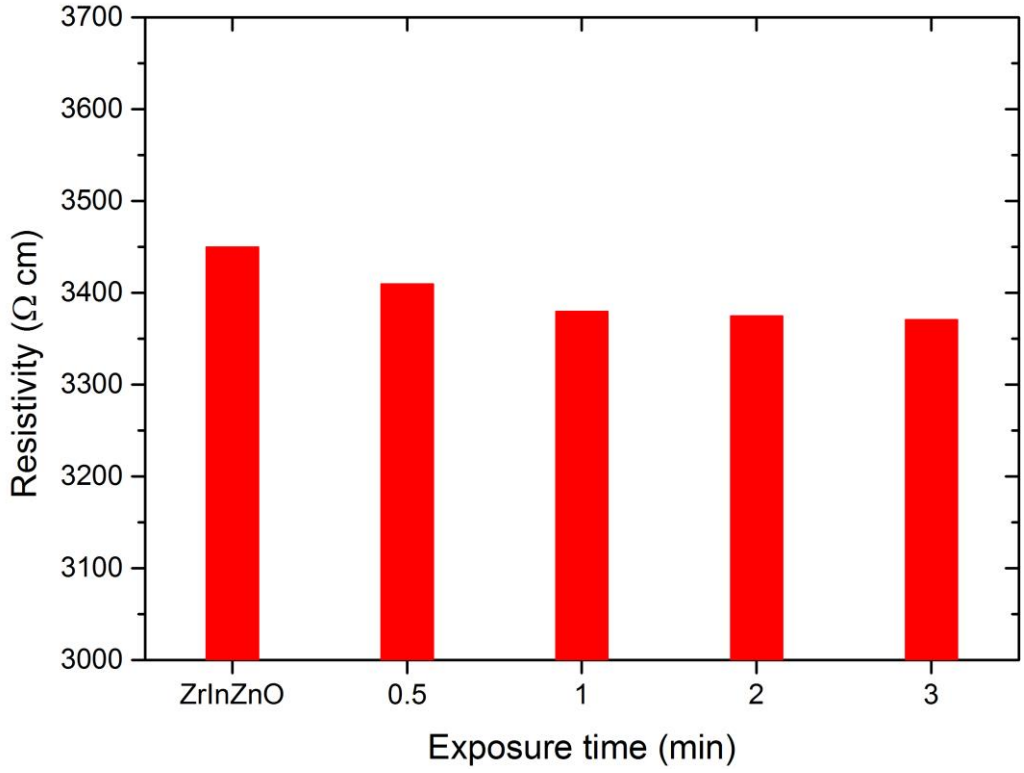


Figure 5-3. Dependence of resistivity the 40 nm thick ZrInZnO film on CF_4 plasma exposure time

of the non-treated ZrInZnO film. Therefore, it can be concluded that the CF_4 plasma did not contribute to reducing resistivity of the ZrInZnO.

4.3.2 Resistivity of ZrInZnO source and drain regions after plasma CF4 etching to remove SiO2 gate insulator layer

Since etching rate of SiO_2 by CF_4 etching is about 7.5 nm per min, so in this study to etch 115~120 nm thick-SiO_2 gate insulator it takes about 15 min. Figure 4-4 shows resistivity of the ZrInZnO source and drain regions obtained by four-probe measurement after plasma etching to remove SiO_2 gate insulator with etching time from 15 to 17 min. As can be seen, resistivity of the ZrInZnO source and drain regions was significantly decreased after etching. For the sample be etched for 17 min the resistivity was 1.2×10^{-1} Ω cm. It was suggested that the reduction in resistivity of ZrInZnO after being etched to remove SiO_2 gate insulator could be due to the diffusion of hydrogen atoms in the polysilazane derived SiO_2 into the ZrInZnO during annealing process at 450 ^oC. The polysilazane derived SiO_2 was studied elsewhere [2]. It was reported that the hydrogen in oxide semiconductor materials

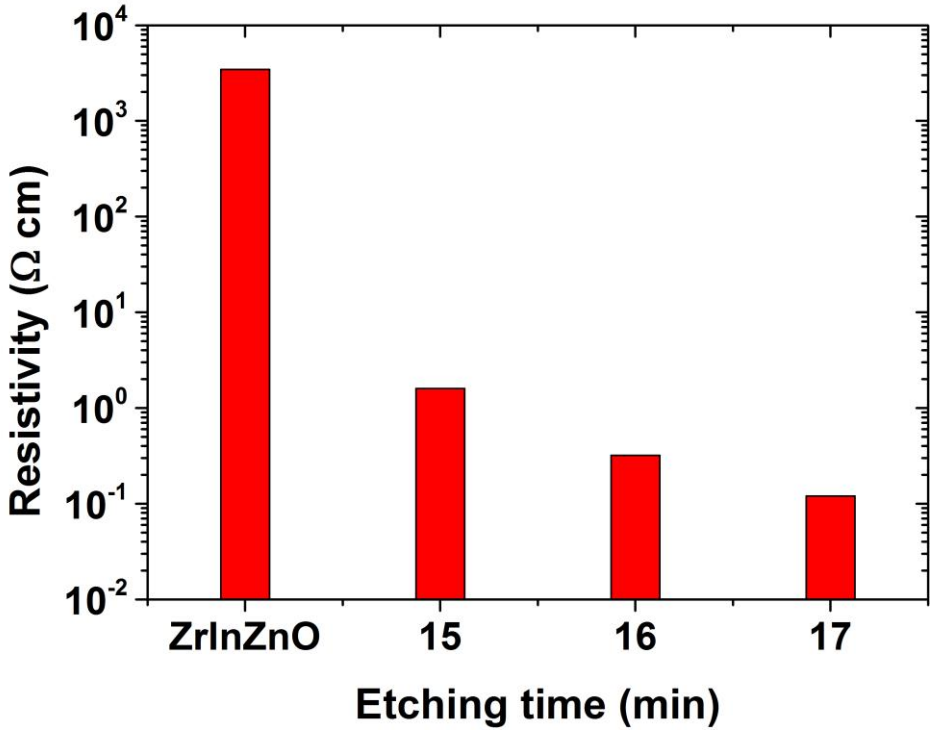


Figure 4-4. Resistivity of ZrInZnO source and drain regions after plasma CF_4 etching to remove SiO_2 gate insulator

acts as shallow donor, which leads to an increase in carrier concentration and thus an increase in conductivity of the oxide semiconductor [3]-[4].

By heat treatment at 250 ºC for 5 min on hotplate the electrical characteristic of the ZrInZnO was recovered, i.e. resistivity of the etched-ZrInZnO was increased to 3.5×10^3 as high as that of ZrInZnO as fabricated. The self-aligned TFT fabricated in this study was heat treated to recover the resistivity of the ZrInZnO after being deposited polysilazane derived SiO_2 gate insulator and CF_4 etching.

4.3.3 TFT characteristics

Figure 4-5 shows the transfer characteristics of the self-aligned top-gate ZrInZnO TFTs that S/D regions was coated by the Sn:PPC solution 10 and annealed at 400 ºC for 20 min under N_2 (at fabrication step 7). The channel width and length were 60 µm and 5 µm, respectively. It was confirmed that good transfer characteristics were achieved, which results from high conductivity of the S/D

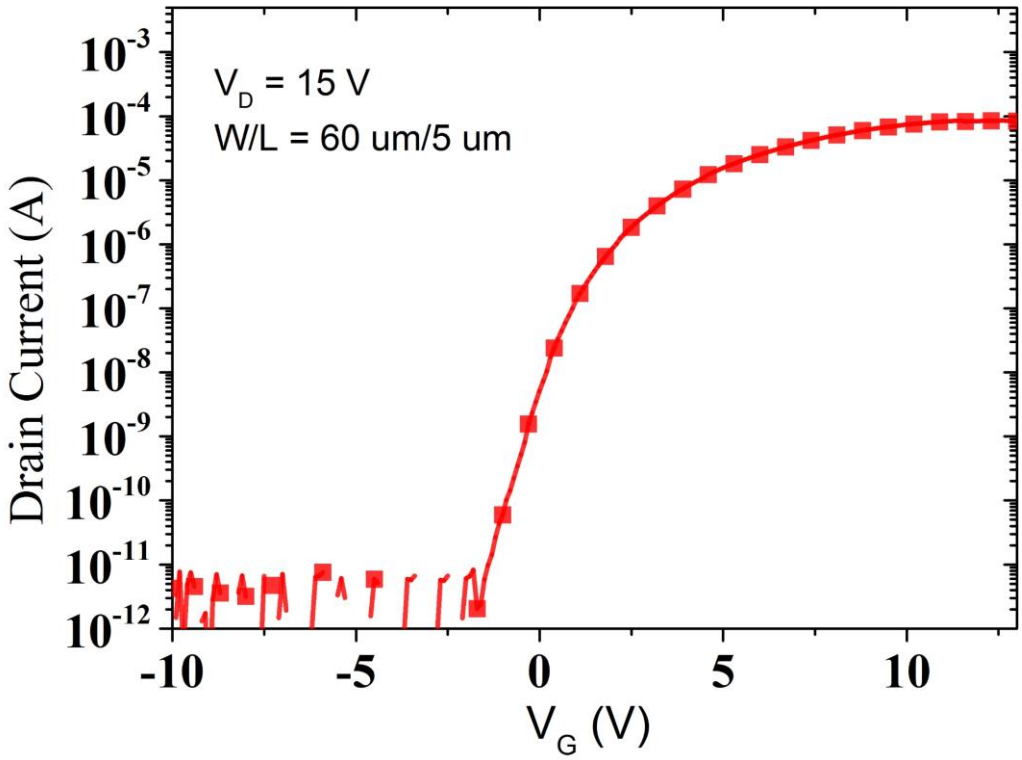


Figure 4-5. Transfer characteristics of self-aligned top-gate ZrInZnO TFT as doped by the Sn:PPC solution (at fabrication step 7)

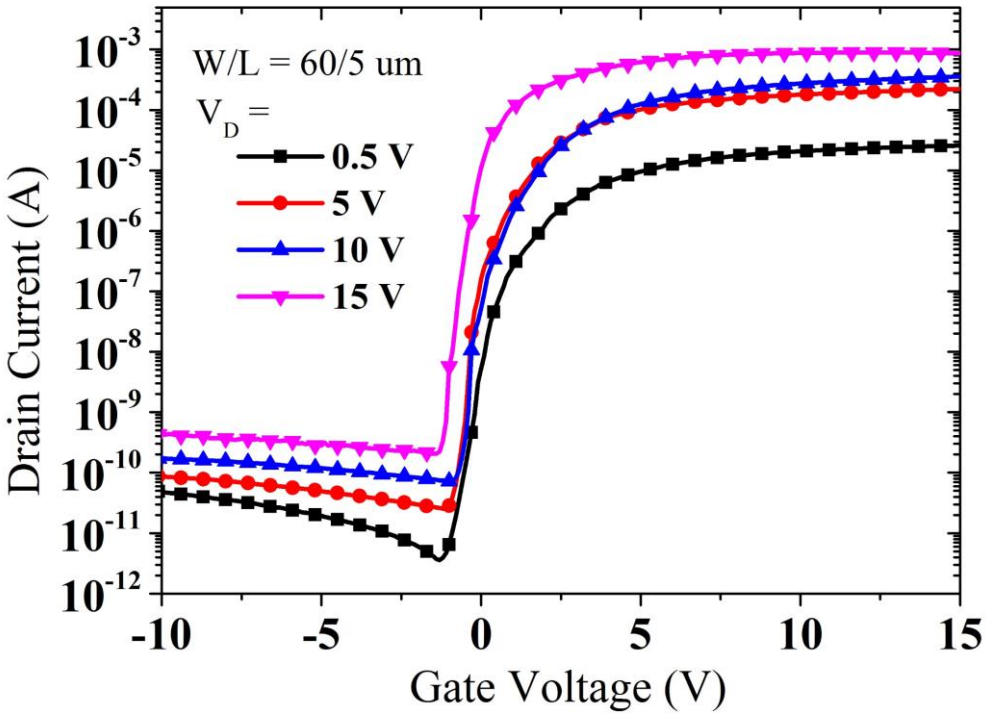


Figure 4-6. Transfer characteristics of self-aligned top-gate ZrInZnO TFT with different applied drain voltages.

regions of the TFT. The doping method using the Sn:PPC solution was successfully applied to fabricate self-aligned TFT.

Figure 4-6 shows the transfer characteristics of the self-aligned top-gate ZrInZnO TFTs with final structure, shown in Figure 4-2. As can be seen in this figure, good transfer characteristics were obtained. The TFT exhibited a high mobility of 20 $cm^2 V^{-1} s^{-1}$, a high ON/OFF ratio of 7 and a small subthreshold swing of 0.2 V/decade. The saturation mobility was estimated form the slope of $(I_D)^{0.5}$ versus the gate voltage (V_{GS}). A threshold voltage of 1 V of the TFT was induced from the intersection of the linear portion of the $(I_D)^{0.5}$ curve at the x-axis (V_{GS}). The subthreshold swing was calculated as the minimum value of the inverse slope of the $\log_{10}(I_D)$ versus V_{GS}:

$$S.S = \frac{dV_{GS}}{d(\log_{10} I_D)}.$$

The characteristics of the self-aligned ZrInZnO TFT with S/D regions doped by the Sn:PPC solution are comparable with those of the self-aligned TFT with S/D regions fabricated by implantation [5-6], Ar plasma treatment [7], or hydrogen

diffusion [8]. These results indicate that the solution process involving PPC solution can be used to fabricate self-aligned oxide TFTs.

4.4 Conclusion

The solution-processed self-aligned ZrInZnO TFT was fabricated. The source and drain region of the TFT was doped by using the Sn:PPC solution. The self-aligned ZrInZnO TFT exhibited a mobility of 20 $cm^2 V^{-1} s^{-1}$, a threshold voltage of 1 V, a subthreshold swing of 0.2 V/decade, and an ON/OFF ratio of 7. These results are very promising for the development of high-operation-speed circuits using a solution-based process.

Reference

[1] J. Park, I. Song, S. Kim, S. Kim, C. Kim, J. Lee, H. Lee, E. Lee, H. Yin, K. –K. Kim, K. –W. Kwon, and Y. Park, *Appl. Phys. Lett.*, 2008, 93, 053501.

[2] H. T. C. Tu, S. Inoue, P. T. Tue, T. Miyasako, and T. Shimoda, "Investigation of Polysilazane-Based SiO_2 Gate Insulator for Oxide Semiconductor Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 60, pp. 1149, 2013.

[3] C. –H. Wu, H. –H Hsieh, C. –W. Chien, and C. –C. Wu, *J. Display Technol.*, 2009, 5, 515.

[4] S. Kim, J. Park, C. Kim, I. Song, S. Kim, S. Park, H. Yin, H.-I. Lee, E. Lee, and Y. Park, *IEEE Electron Device Lett.* 2009, 30, 374.

[5] R. Chen, W Zhou, M Zhang, M Wong, and H-S Kwok, "Self-Aligned Indium–Gallium–Zinc Oxide Thin-Film Transistor with Phosphorus-Doped Source/Drain Regions," *IEEE Electron Device Lett.*, vol. 33, pp. 1150, 2012.

[6] R. Chen, W Zhou, M Zhang, M Wong, and H-S Kwok, "Self-Aligned Indium–Gallium–Zinc Oxide Thin-Film Transistor With Source/Drain Regions Doped by Implanted Arsenic," *IEEE Electron Device Lett.*, vol. **34**, pp. 60, 2013.

[8] J. Park, I. Song, S. Kim, S. Kim, C. Kim, J. Lee, H. Lee, E. Lee, H. Yin, K. –K. Kim, K. –W. Kwon, and Y. Park, *Appl. Phys. Lett.*, 2008, 93, 053501.

[9] D. H. Kang, I. Kang, S. H. Ryu, and J. Jang, *IEEE Electron Device Lett.* 2011, 32, 1385.

Chapter 5

Wet-annealed Plysilazane-derived SiO_2 gate insulator for further improvement

The main purpose of this dissertation is to realize all solution processed self-aligned oxide semiconductor TFT. In previous chapters I reported the self-aligned ZrInZnO TFT with solution-processed ZrInZnO channel and the novel doping method based on solution-processed. In this chapter I will present the solution-processed gate insulator.

5.1 Introduction

The main purpose of this dissertation is to realize all solution processed self-aligned oxide semiconductor TFT. In previous chapters I reported the self-aligned ZrInZnO TFT with solution-processed ZrInZnO channel and the novel doping method based on solution-processed. In this chapter I will present the solution-processed gate insulator.

In oxide semiconductor TFT, along with the significant role that the active oxide semiconductor layer plays in determining the characteristics of TFTs, gate insulators also greatly influences their stability and overall performance [1, 2]. A low leakage current and high breakdown voltage are required for good insulators, and both contribute to the stability of TFTs. Among insulating materials, SiO_2 is the most promising candidate for a good insulator due to the ability of satisfying the above-mentioned requirements [3-5].

Previously, we prepared a SiO_2 gate insulator with a leakage current of 10^{-8} A/cm^2 at 1 MV/cm by using polysilazane, which is the same level as those of CVD-SiO_2 films, and then this film was applied to solution-processed ZrInZnO TFTs [6]. However, the leakage current of the film was still much higher than that of a thermally prepared SiO_2 film. It was assumed that the high leakage current was owing to an incomplete conversion of the polysilazane to SiO_2. Therefore, enhancement of this conversion is necessary for obtaining higher quality films.

In this chapter, therefore I report a wet-annealing method for the fabrication of high-quality SiO_2 films from polysilazane-derived solutions. That is to say, water vapor was supplied during the annealing process to enhance the conversion. The properties of a wet-annealed film is evaluated, and the effect of the film on the characteristics of a ZrInZnO TFT with self-aligned and non-self-aligned structure is investigated.

5.2 Experimental procedure

5.2.1 Thin-film deposition

Polysilazane solution (5% in di-butyl-ether, ANL120-5, AZ Electronics Materials) was used to form the SiO_2 films. Polysilazane consists a basic unit $[H_2Si–NH]_n$. To produce SiO_2 the following reaction occurs.

$$-\left(H_2Si-NH\right)-+2H_2O \rightarrow SiO_2+NH_3+2H_2$$

More detailed information regarding the preparation of SiO_2 films from polysilazane can be found in the literature [6]. The solution was spin coated at 2500 rpm for 30 s onto p^+−silicon substrates that were cleaned by dipping in acetone for 5 min, followed by O_2 ashing at 15 W for 3 min to form films. These films were then annealed at 450 °C for 2 h either under an air atmosphere (dry annealing) or a water vapor atmosphere (wet annealing). The setup of the system for wet annealing is shown in Figure 5-1. To obtain a wet environment, oxygen was passed through a bottle containing water. The moistened oxygen gas was introduced into a bell that covered a hotplate. The water was maintained at room temperature, and the flow rate

of O_2 was 100 ml/min. The thickness of the films ranged from 114 to 120 nm.

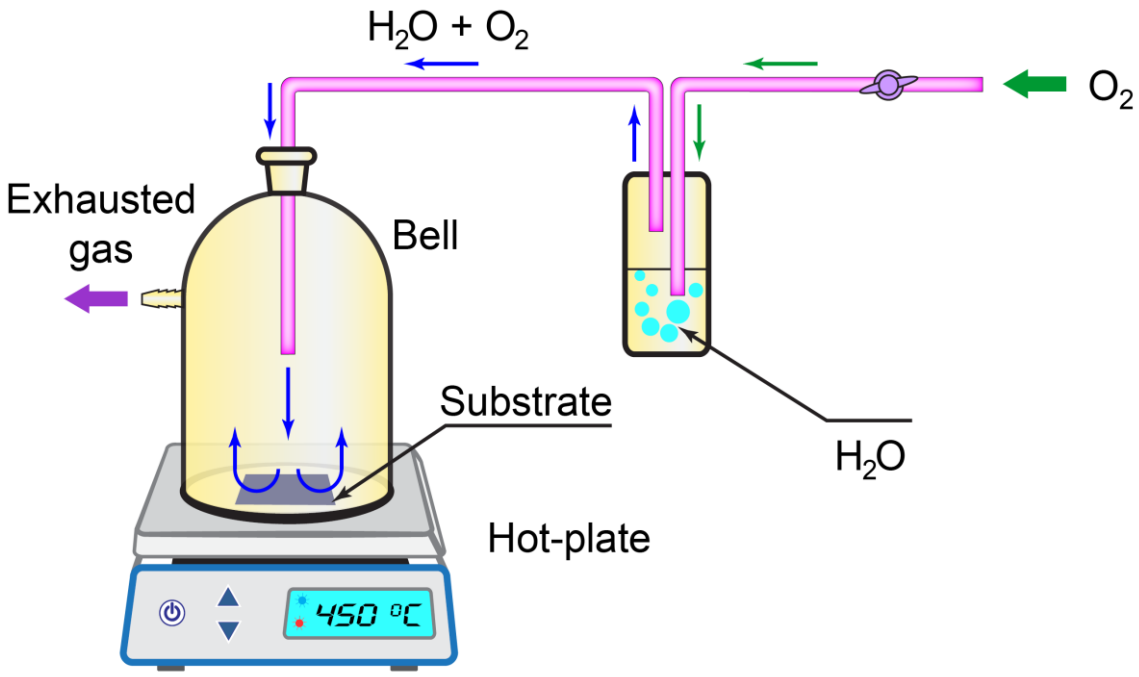


Figure 5-1. Schematic of the wet-annealing system

5.2.2 Device fabrication

5.2.2.1 Capacitors

To investigate the electronic properties of these SiO_2 films, two types of capacitor structures were fabricated: a capacitor composed of Pt/polysilazane-derived SiO_2/p^+−silicon and a metal/insulator/semiconductor/metal (MISM) capacitor composed of Al/polysilazane-derived SiO_2/n-Si/Al. The 200-nm Pt electrode was deposited via RF sputtering in Ar gas at 2.7×10^{-3} Pa at room temperature. The 100 nm-thick Al layer was deposited by evaporation method. For fabrication of the MISM capacitor, the polysilazane solution was spin coated at 2500 rpm for 30 s on one side of 290-μm-thick n-type (100) Si wafers with a resistivity of 2.5 Ω cm to form films. These film were wet-annealed at 450 °C for 2 h. These capacitors were then post-annealed at 400 °C in N_2 for 10 min using RTA.

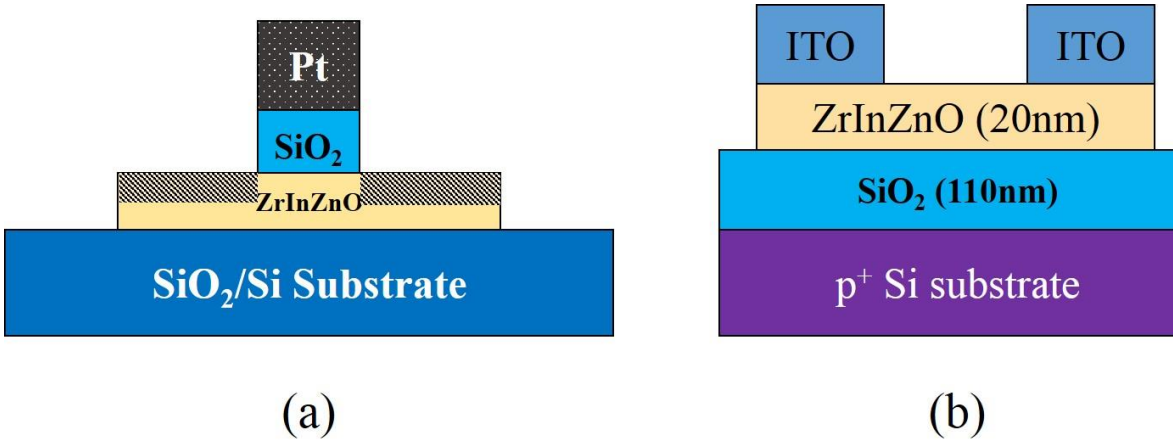


Figure 5-2. Schematic cross-section view of TFT with (a) self-aligned and (b) non-self-aligned (reverse-staggered) structure

5.2.2.2 Thin-Film Transistors

Two types of TFT structures were fabricated using wet-annealed polysilazane-derived SiO_2 films as the gate insulators: a self-aligned structure and a non-self-aligned structure, i.e. reverse-staggered, shown in Figure 5-2. Fabrication process of the self-aligned TFTs are describes in Chapter 5. The reverse-staggered TFTs were fabricated by spin-coating polysilazane on p^+-Si substrate used as their gate electrode and then annealed at 450 ^oC for 2 h, forming a SiO_2 gate insulator with thickness of about 115 nm. Next, the 20 nm active channel ZrInZnO was deposited. Fabrication conditions of this film are described in Chapter 4. After that, ITO source and drain electrodes were deposited via RF sputtering in Ar gas at 8×10^{-4} Pa at 100 °C. Finally, the TFTs were post-annealed with RTA at 400 ^oC for 10 min in ambient air.

5.2.3 Characterization

The molecular composition of the films was characterized by using a Fourier transform infrared (FT-IR) spectrophotometer (Bruker Alpha). The leakage current was measured by using a semiconductor parameter analyzer (Agilent 4155C). Positive voltages were applied to the top electrode of the capacitor, whereas the bottom electrode was grounded. The capacitance–voltage (C–V) characteristics were

measured at a frequency of 1 kHz using an Agilent 4284A LCR meter. The transfer (I_D–V_G) characteristics of the TFTs were measured using a semiconductor parameter analyzer (Agilent 4155C).

5.3 Results and discussion

5.3.1 FT-IR analysis

Figure 5-3 shows normalized FT-IR absorbance spectra at 4000−440 cm^{-1} of the wet- and dry-annealed SiO_2 films. The 1057, 810, and 455 cm^{-1} peaks are attributed to the Si–O–Si asymmetric stretching, bending (or symmetric stretching), and rocking vibrations, respectively [6-9]. As also can be seen in this figure, the intensity of the shoulder peak in the lower-frequency region near 960–860 cm^{-1} of

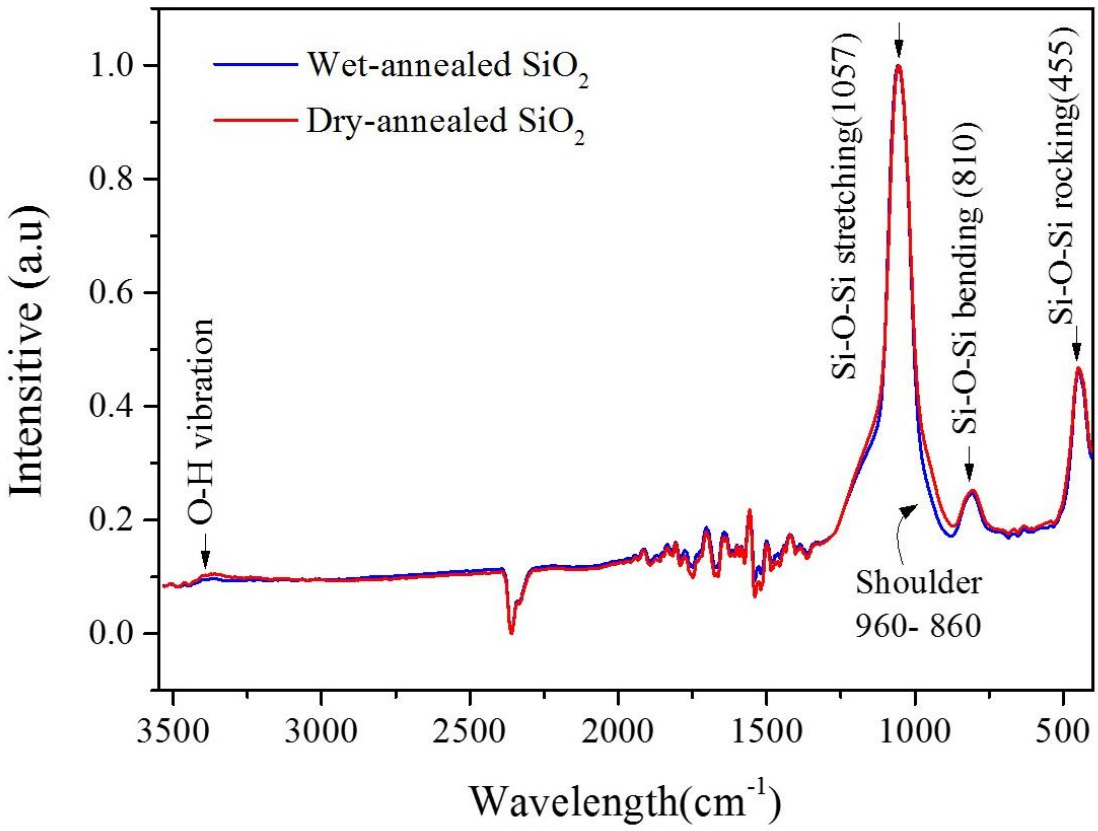
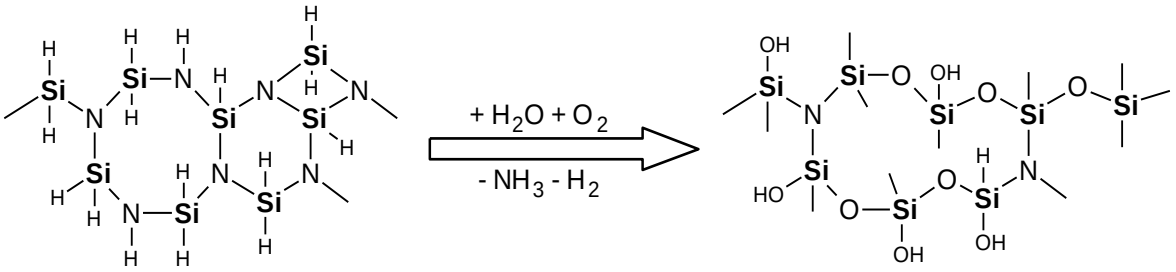


Figure 5-3. FT-IR normalized absorbance spectra of wet- and dry-annealed SiO_2 films prepared from polysilazane. These films were deposited on non-doped Si substrates.



Polysilazane Annealed film composition

the wet-annealed SiO_2 film was smaller than that of the dry-annealed SiO_2 film. In order to understand the origin of this decrease, the spectra in the range of 1300–700 cm^{-1} was deconvoluted by Gaussian fitting. Five absorbance bands centered at approximately 1190, 1140, 1057, 955, and 810 cm^{-1} were obtained, which are shown in Figures 5-4 (a) and (b). The two deconvoluted peaks at 1190 and 1140 cm^{-1} are presumably due to vibrations of the Si–O–Si network [8]. The peak at 955 cm^{-1} is assigned to a Si–OH vibration mode [8, 10]. The remaining Si–OH bonds in the films are assumed to be due to incomplete hydrolysis/condensation reactions to form a Si–O–Si network, which is seen in the following proposed reaction scheme:

As can be observed in Figures 5-4 (a) and (b), the intensity of the Si–OH peak decreased when the film was wet-annealed. This result was also confirmed by the decrease in the intensity of the peak for the O–H vibration mode (at approximately 3400 cm^{-1}) that can be seen in Fig. 2 [8]. The reduction in the intensity of the Si–OH peak when the film was wet-annealed indicate that the polysilazane was more effectively converted to SiO_2.

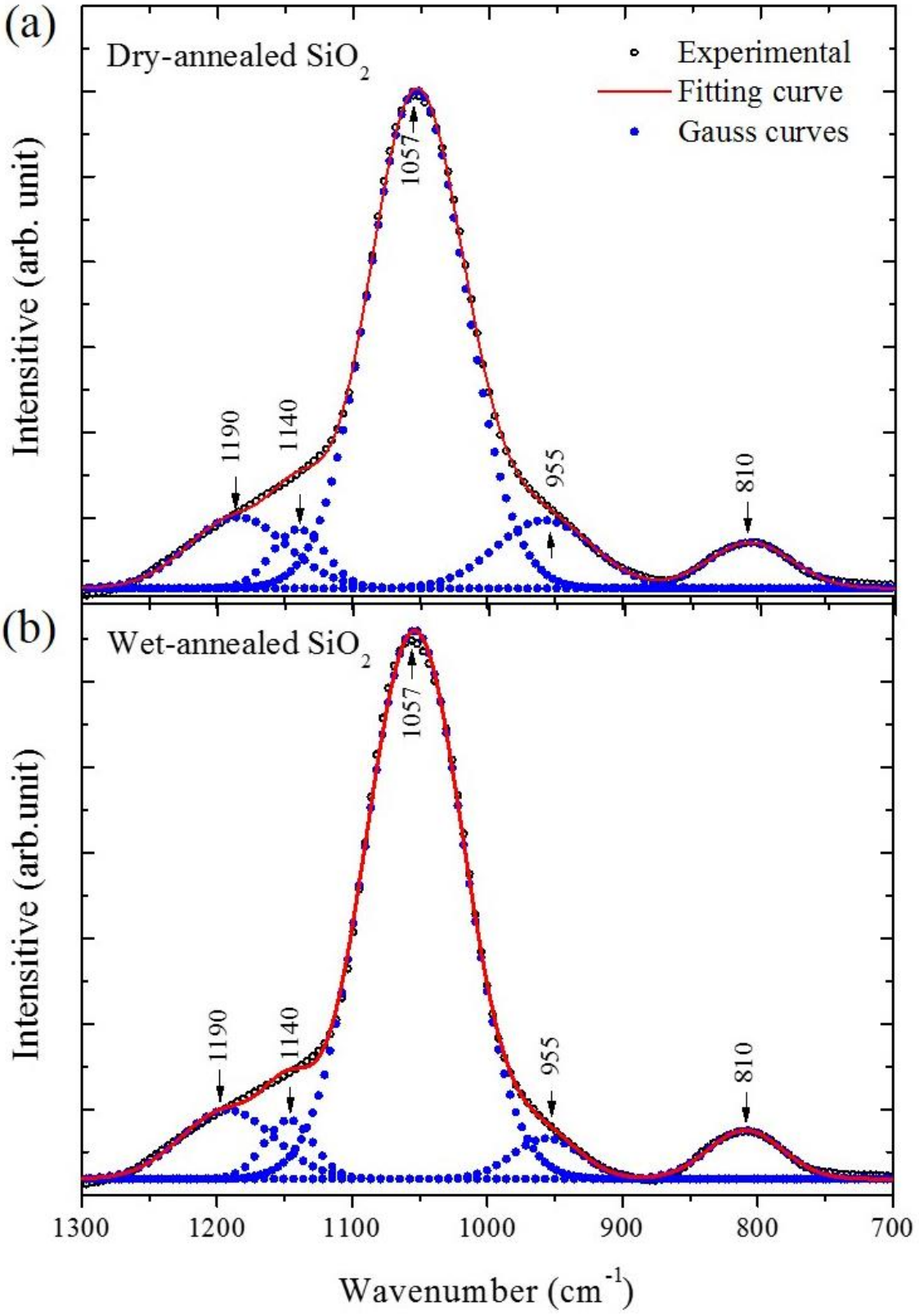


Figure 5-4. Deconvoluted FT-IR spectra of the (a) wet- and (b) dry-annealed SiO_2 films using a Gaussian-type function.

5.3.2 Electrical properties

The leakage current densities of the wet- and dry-annealed polysilazane-derived SiO_2 films at 450 °C for capacitor with structure of Pt/polysilazane-derived SiO_2/p^+-silicon are shown in Figure 5-5. It can be seen in the figure that the wet-annealed film had a leakage current density of 2.5×10^{-9} A/cm^2 at 1 MV/cm, which is more than one order of magnitude smaller than that of the dry-annealed SiO_2 film (3.7×10^{-8} A/cm^2 at 1 MV/cm) and only approximately five times larger than that of the thermal SiO_2 film shown in the figure. The low leakage current of the wet-annealed SiO_2 film may be attributed to fewer Si–OH bonds than those of the dry-annealed one, which is consistent with the FT-IR spectra. These results thus indicated that a low off and gate leakage current TFT could be obtained using a wet-annealed SiO_2 gate insulator.

The C–V curve measured at 100 KHz on MISM capacitors with Pt/polysilazane-

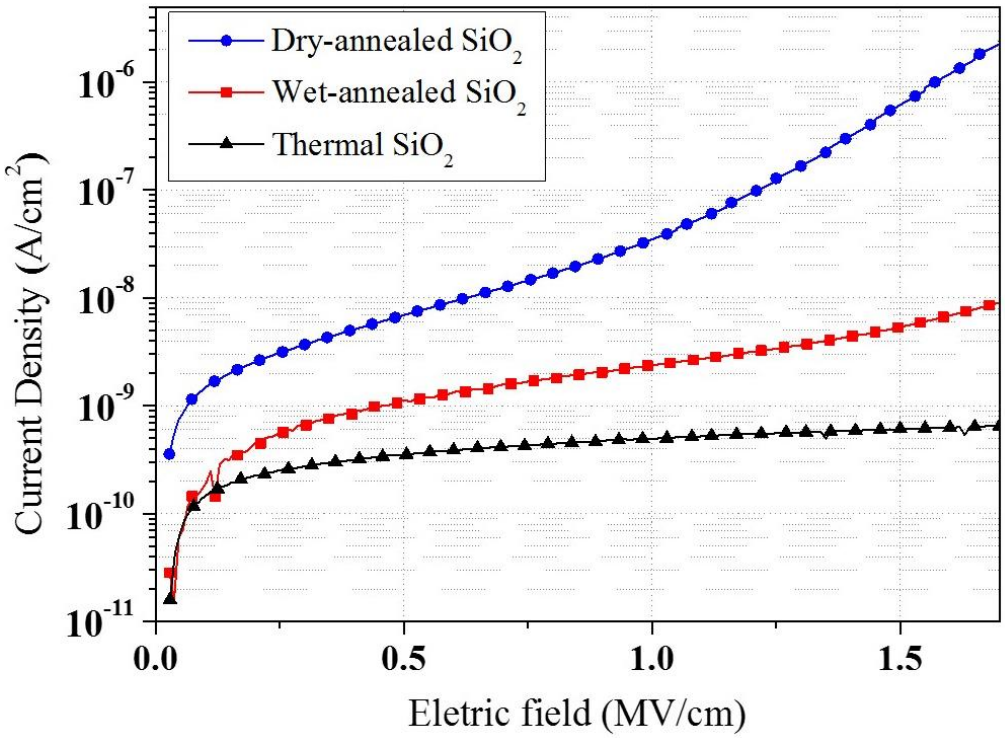


Figure 5-5. Leakage current densities of a thermal SiO_2 (100 nm thick) and wet- and dry-annealed SiO_2 films. The leakage current was measured on the capacitor composed of Pt/polysilazane-derived SiO_2/p^+-silicon.

derived SiO_2/n-Si/Al structure is shown in Figure 5-6. The accumulation capacitance of the insulators derived from these curves was 3.54×10^{-8} F/cm^2. The dielectric constant derived from this accumulation capacitance is about 4.6, which is consistent with the one obtained from Q-V measurement. The C–V curve also shows that the hysteresis is very small. It was supposed that hysteresis observed in C-V curve resulted from bulk traps in the gate insulator [11] and interface trap between the gate insulator and channel [12]. Upon applying a positive gate voltage the traps quickly filled by electrons from the semiconductor. When sweeping from positive to negative (backward sweep) the traps were emptied slowly causing higher capacitance. The elimination of hysteresis is suggested by to high quality of the SiO_2 gate insulator.

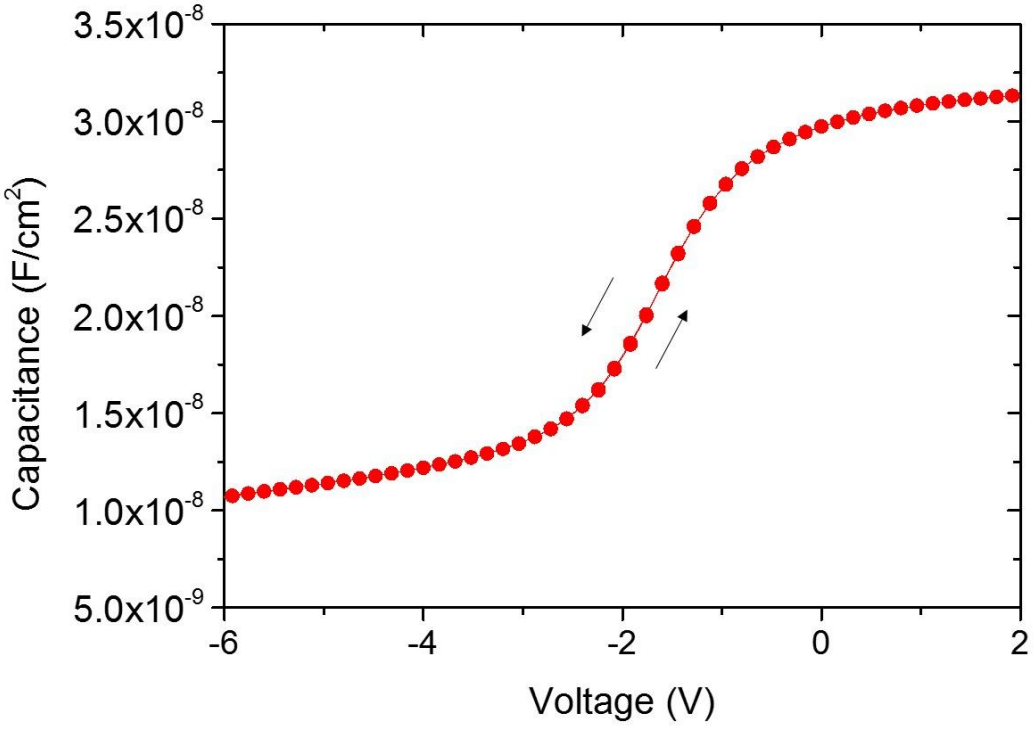


Figure 5-6. . C–V curves (measured at 100 KHz with sweep rate of 0.16 V/s) for MISM capacitors with Al/polysilazane-derived SiO_2/n-Si/Al structure.

5.3.4 Transistor characteristics

The transfer characteristics of the reverse-staggered TFTs with dry- and wet-annealed SiO_2 gate insulators are shown in Figure 5-6 (a). The channel width and

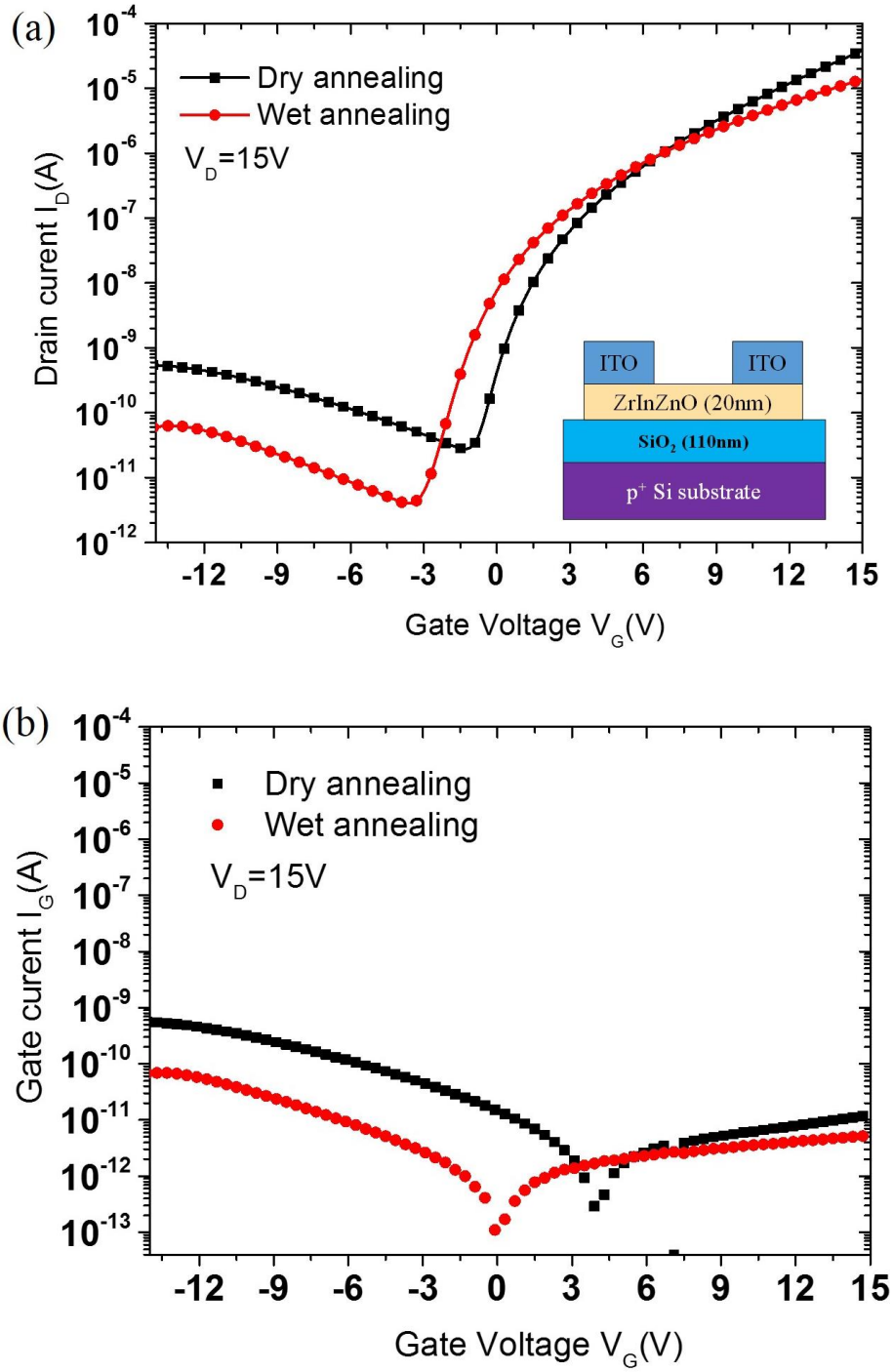


Figure 5-7. I_D–V_G transfer characteristics of reverser-staggered TFTs with wet- and dry-annealed SiO_2 gate insulators, W/L = 60/20 μm).

length were 60 and 20 μm, respectively. The wet-annealed SiO_2-derived TFT exhibited a lower gate leakage current and off-current. The off-current of 5.8×10^{-12} A at −5 V was lower by one order of magnitude than that of the dry-annealed one. Figure 5-6 (b) shows the gate leakage current (I_G) of the reverse-staggered TFTs. The

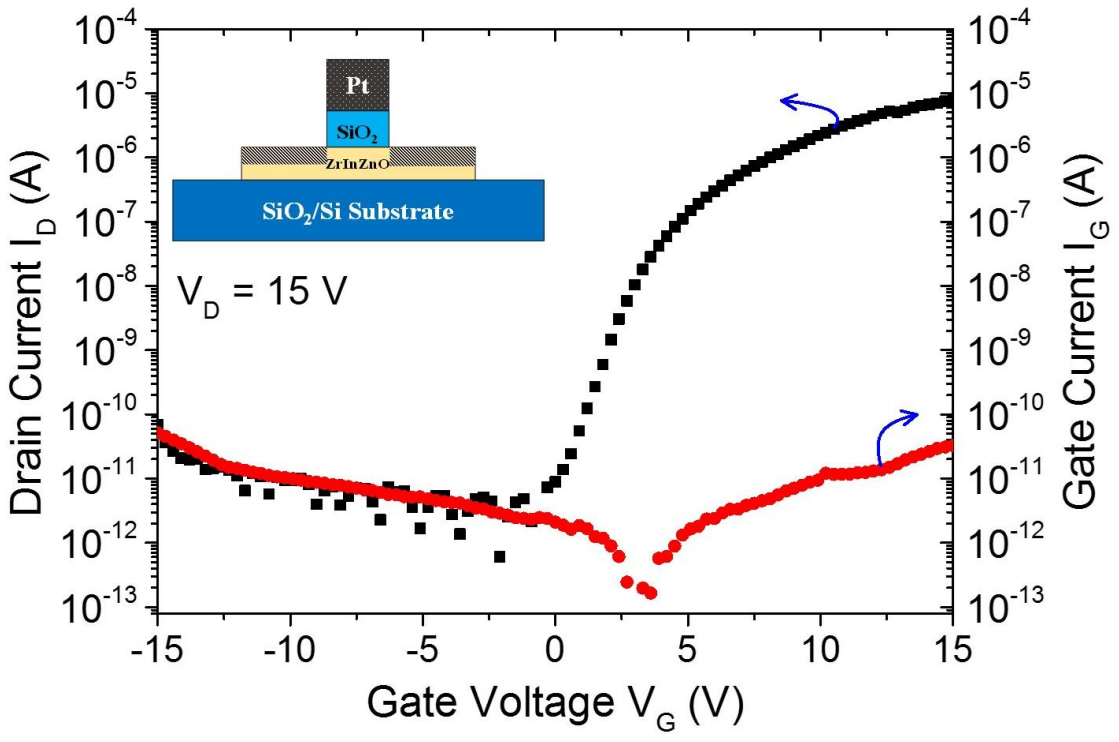


Figure 5-8. Transfer characteristics of self-aligned TFT with wet- annealed SiO_2 gate insulators, W/L = 60/20 μm).

gate current of the TFT with wet-annealed SiO_2 gate insulator was rather small, about 5×10^{-12} A at 15V, which is five times smaller than that of the TFT with dry-annealed SiO_2 gate insulator (1×10^{-11} (A) at 15V). These obtained results owe to the reduction in leakage current of the wet-annealed SiO_2 gate insulator.

Figure 5-8 shows transfer and gate leakage current characteristics of the self-aligned TFT employed wet-annealed SiO_2 as a gate insulator. The TFT also exhibited a low off-current of about 5×10^{-12} A at −5 V and a small gate current of 2.7×10^{-11} A at 15V.

The TFT parameters extracted from the transfer curves in Figure 5-7 and Figure 5-8 are tabulated in Table 5-1. The saturation mobility μ_{sat} was obtained from the transconductance with a high V_D [4, 13]:

$$\mu_{sat} = \frac{\frac{d\sqrt{I_D}}{dV_G}}{\frac{1}{2}\frac{W}{L}C_{ox}}, (1)$$

where C_{ox}, W, and L are the gate oxide capacitance per unit area, the width of the

channel, and length of the channel, respectively. The subthreshold swing SS was derived using the equation [14]:

$$SS = \frac{dV_G}{d(logI_D)}\Big|_{V_D=constant}. \qquad (2)$$

The threshold voltage was obtained from the *x*-axis intersect of the linear portion of the $(I_D)^{0.5}$ versus V_G plot.

Although the off-current and gate leakage current of wet-annealed SiO_2-derived TFT were decrease, the TFTs exhibited a substantial reduction in mobility and a slight degradation of subthreshold slope. It was supposed that the large subthreshold slope value for these transistors was contributed by the interface trap density between the gate insulator and the channel [1, 15] and the bulk traps in ZrInZnO channel layer. This in turn would deteriorate the mobility related to the interface. Currently, it is not made clear why the interface trap density is higher in the wet-annealed than in dry-annealed one. Further study is required to clarify this issue.

Table 5-1. TFT parameters extracted from the transfer curves in Figure 5-7 and Figure 5-8, including the threshold voltage (V_{th}), field-effect mobility (μ), subthreshold swing (SS), and on/off ratio

TFT structure	SiO_2 gate insulator	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	SS (V/dec)	On/Off ratio
Reverse- staggered	Dry-annealed	7.8	16.1	0.8	1.3×10^6
Reverse- staggered	Wet-annealed	5.5	3.8	0.82	3×10^6
Self-aligned	Wet-annealed	3.9	3.9	0.87	2×10^6

5.4 Conclusion

A polysilazane-derived SiO2 gate insulator prepared using a wet-annealing method was investigated. The leakage current density of the SiO2 film was 2.2×10^{-9} A/cm^2 at 1 MV/cm, which was more than one order of magnitude smaller than that of dry-annealed SiO_2 films. The solution-processed ZrInZnO TFT with both reserve staggered and self-aligned structures prepared using the wet-annealed SiO_2 film as

the gate insulator exhibited a rather small gate leakage current of less than 7×10^{-11} A/cm^2 at 15 V. The off current was also dramatically decreased owing to the good performance of the wet-annealed SiO_2 gate insulator. It is thus expected that wet-annealed SiO2 can be used as a dielectric material for oxide semiconductor TFTs.

Reference

[1] E. Fortunato, P. Barquinha, and R. Martins: Adv. Mater., **24** (2012) 2945.

[2] Y. J. Cho, J. H. Shin, S. M. Bobade, Y. B. Kim, and D. K. Choi: Thin Solid Films **517** (2009) 4115.

[3] H. U. Kim, and S. W. Rhee: J. Electrochem. Soc., **147** (2000) 1473.

[4] Y. Inoue, and O. Takai: Plasma Sources Sci. Technol. **6** (1996) 339.

[5] J. Batey, and E. Tierney: J. Appl. Phys. **60** (1986) 3136.

[6] H. T. C. Tu, S. Inoue, P. T. Tue, T. Miyasako, and T. Shimoda: IEEE Trans. Electron Devices: **60** (2013) 1149.

[7] J. P. Bange, L. S. Patil, and D. K. Gautam: Progress In Electromagnetics Research M **3** (2008) 165.

[8] N. Primeau, C. Vautey, and M. Langlet: Thin Solid Films **310** (1997) 47.

[9] Q. Hu, H. Suzuki, H. Gao, H. Araki, W. Yang, and T. Noda: Chem. Phys. Letters **378** (2003) 299.

[10] R. M. Almeida, and C. G. Pantano: J. Appl. Phys. **68** (1990) 4225.

[11] R. I. Hegde, D. H. Triyoso, S. B. Samavedam, and B. E. White: J. Appl. Phys. **101** (2007) 074113.

[12] Th. Lindner, G. Paascha and S. Scheinert: J. Appl. Phys. **98** (2005) 114505.

[13] M. Mativenga, J. K. Um, D. H. Kang, R. K. Mruthyunjava, J. H. Chang, G. N. Heiler, T. J. Tredwell, and J. Jang: IEEE Trans. Electron Devices **59** (2012) 2501.

[14] J. S. Lee, S. Chang, S. M. Koo, and S. Y. Lee: IEEE Electron Device Lett. **31** (2010) 225.

[15] Y. (A) Zeng, A. Softic, and M. H. White, Solid-State Electron. **46** (2002) 1579.

Chapter 6

General conclusion

The objective of this dissertation is applying the solution process to fabricate high conductive source and drain regions (S/D regions) of the ZrInZnO self-aligned structure TFT. By employing the solution process costs would be greatly decreased, because can simplify equipment, efficiently use materials and production energy. The ZrInZnO is a type of oxide semiconductor materials which have recently gained considerable attention in emerging electronic applications, such as flat-panel displays (FPDs), transparent and flexible displays including electronic papers (e-papers), organic light-emitting-diode displays (OLEDs) and liquid crystal displays (LCDs) because of their relative high mobility, excellent uniform in device characteristics and low-temperature fabrication. The utilization of the ZrInZnO in this study is due to its ability in improving the performance and bias-stress stability of the TFT. The TFT with self-aligned structure was studied here because this structure exhibits a low parasitic capacitances and an ability to scale down the size of the device.

By developing of the Sn:PPC material which is a mixture of Sn solution and polypropylene carbonate (PPC) solution, I succeeded to apply solution process in fabrication of the high conductive S/D regions of the ZrInZnO self-aligned TFTs. The Sn solution was prepared by dissolving tin acetylacetonate ($Sn(acac)_2$) in propionic acid (PrA), while the PPC solution was synthesized by dispersing PPC in diethylene glycol monoethyl ether acetate (DEGMEA). To fabricate high conductive ZrInZnO S/D regions the Sn:PPC solution was used to coat on ZrInZnO S/D regions, followed by annealing under conditions suitable to decompose PPC and to allow diffusion of Sn into the ZrInZnO. Sn acts as a donor in ZrInZnO, resulting in an

increase in the conductivity of the ZrInZnO S/D regions. Purpose of using PPC is to prevent the formation of the SnO_x, derived from the Sn solution, between S/D regions of the self-aligned TFT.

In chapter 2, characterization of the Sn:PPC solution was presented. It was found that the solute in the Sn:PPC solution was in an configuration with coordination of large PPC molecules with Sn clusters. The Sn cluster was in a configuration of coordinated PrA ligand, water and oxygen around the Sn atom. The size of the Sn clusters was about 1.6 nm, while PPC molecules in solution was about 1.9 nm, 5.5 nm, 37.6 nm and 721 nm.

In chapter 3, employing the Sn:PPC solution to fabricate high conductivity ZrInZnO for S/D regions of self-aligned TFT was described. The Sn:PPC solution was coated and annealed to make Sn diffuse into the ZrInZnO film. It was confirmed that Sn diffused into ZrInZnO film to a depth of 22 nm. Sn acts as a donor in ZrInZnO, which results in an increase in the conductivity of the ZrInZnO film. It was confirmed that resistivity of the Sn-diffused ZrInZnO was reduced to 1.8×10^{-2} Ω cm at annealing temperature of 300 ^{o}C under N_2 ambience when the Sn:PPC solution was used. The increase in resistivity of the sample annealed at temperature over 500 ^{o}C was due to the change in structure characteristic of the ZrInZnO film. To make high conductive ZrInZnO the ambience with oxygen should be avoided.

In chapter 4, the self-aligned ZrInZnO TFT was fabricated. The source and drain region of the TFT was doped by using the Sn:PPC solution. The self-aligned ZrInZnO TFT exhibited a mobility of 20 $cm^2 V^{-1} s^{-1}$, a threshold voltage of 1 V, a subthreshold swing of 0.2 V/decade, and an ON/OFF ratio of 7. These results are very promising for the development of high-operation-speed circuits using a solution-based process.

In chapter 5, an investigation of a polysilazane-derived SiO_2 gate insulator prepared using a wet-annealing method was reported. The leakage current density of the wet-annealing SiO_2 film was 2.2×10^{-9} A/cm^2 at 1 MV/cm, which was more than one order of magnitude smaller than that of dry-annealed SiO_2 films. The solution-processed ZrInZnO TFT with both reserve staggered and self-aligned structures

prepared using the wet-annealed SiO_2 film as the gate insulator exhibited a rather small gate leakage current of less than 7×10^{-11} A/cm^2 at 15 V. The off current was also dramatically decreased owing to the good performance of the wet-annealed SiO_2 gate insulator. It is thus expected that wet-annealed SiO2 can be used as a dielectric material for oxide semiconductor TFTs.

ADDITIONAL RESUTLS

Chapter 2: Characterization of the Sn:PPC solution

1. SEC-MALLS-VISCOMESTRY measurement

In order to understand molecular weight, molecular weight distribution and structure of PPC in a solution the size-exclusion chromatography (SEC) combined with multi-angle laser light scattering (MALLS) and viscometry (SEC-MALLS-VISCOMETRY) measurement was executed, which was supported by Dr. Takashi Masuda. Detailed experimental settings are explained in Ref. 1.

Preparing PPC solution:

PPC solution had a concentration of 0.2 wt% purified PPC, which was prepared by dissolving PPC in tetrahydrofuran (THF). The solution was stirred for 12 hours at 50 ^{o}C to complete dissolve PPC in THF. Choosing suitable solvents for the SEC-MALLS measurement is very important. We used diethylene glycol monothyl ether acetate (DEGMEA) as a solvent for the PPC solution to make the doping solution (Sn:PPC solution) because it has an adequate wettability, boiling point, and viscosity for coating in the solution process. However, DEGMEA is not applicable to the SEC-MALLS measurement because of poor solubility and rather high boiling point (214 ^{o}C). For this experiment we select THF as a solvent which boiling point of about 67 ^{o}C.

Results:

Figure 2-1(a) shows refractive index (RI) chromatogram of the PPC solution. The appearance of a broad peak around an elution volume of 8 mL in the chromatogram corresponds to the high molecular weight PPC. The purified PPC has molecular weight of about 23.4×10^4 g/mol. The peaks at higher elution volume is suggested to be due to unknown materials with molecular weight less than 10^3 g/mol.

The differential molecular weight fraction of PPC as a function of molecular weight is shown in Fig. 2-1(b). As can be seen, the molecular weight of PPC ranges broadly

from 10^4 to 10^7 g/mol. The peak at molecular weight of 20.7×10^4 g/mol confirms that most of PPC in solution has the same molecular weight as the purified PPC.

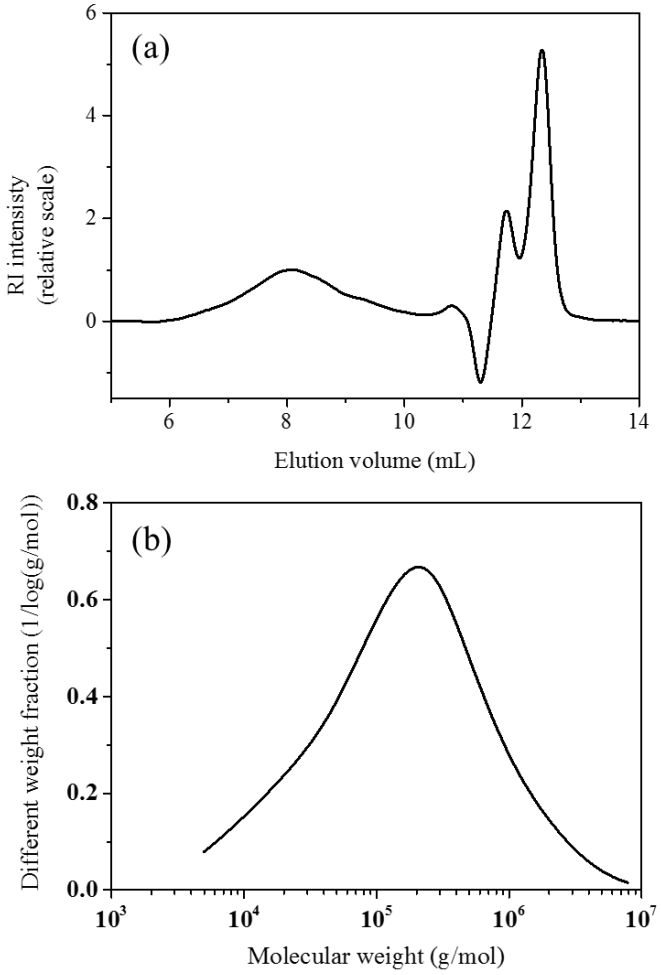


Figure 2-1. *(a) RI chromatograph and (b) molecular weight distribution of the PPC solution obtained by SEC-MALLS measurement.*

In order to explore the structure of PPC, we plotted the intrinsic viscosity $[\eta]$ and radius of gyration (R_g) as a function of molecular weight (M) and analyzed their scaling behaviors. Figures 2-2(a) and 2-2(b) show the logarithmic plots of $[\eta]$ vs M and R_g vs M for the PPC solution. These plots exhibit a scaling feature. Equation (2-1) described the linear function for the fitting of $[\eta]$ vs M in Fig. 2-2(a).

$$[\eta] = 0.0238M^{0.656}, \quad (2\text{-}1)$$

The scaling relation $[\eta] = KM^{\alpha}$, where α denotes the effective length of basic unit of PPC [$CH(CH_3)CH_2O(CO_2)$], is known as the Mark-Houwink-Sakurada equation [2]. The obtained α = 0.656 which is in the range from 0.5 for Flory theta solvent to 0.8 in a good solvent indicates that PPC in solvent THF exists as a random coils structure [2].

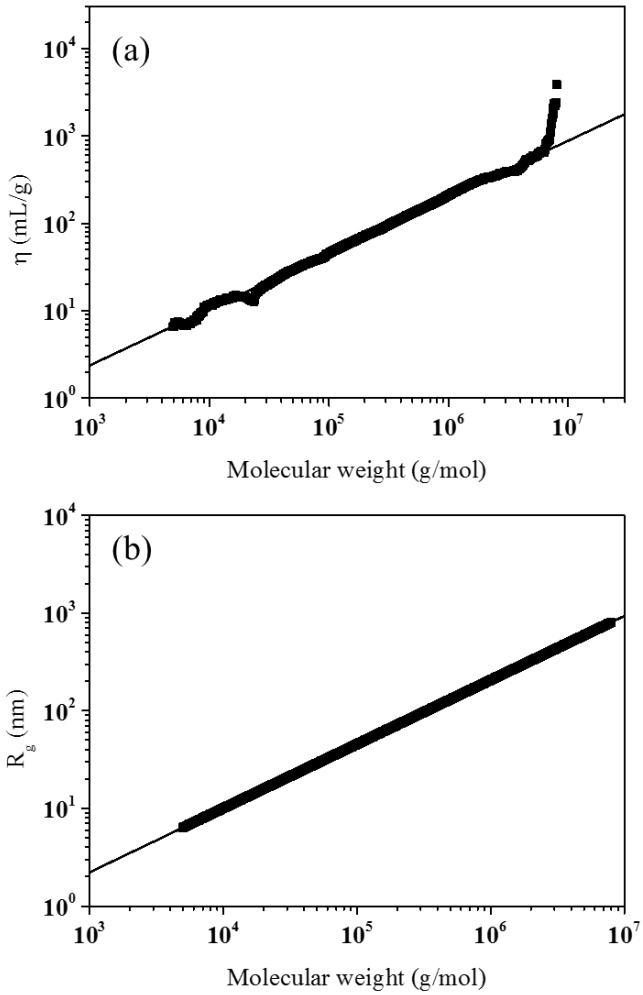


Figure 2-2. *Log-log plot of (a) [η] vs M and (b) R_g vs M for the PPC solution. The solid lines are the linear fits of [η] and R_g, respectively.*

Reference

[1] T. Masuda, Y. Matsuki, and T. Shimoda, Polymer **53**, 2973 (2012)

[2] M. P. Steven, Polymer chemistry: an introduction, third edition, Oxford University Press, 1999.

Chapter 4: Fabrication and characterization of self-aligned ZrInZnO TFT with source and drain regions doped by Sn:PPC solution

1. Source/drain series resistance (R_{SD})

The R_{SD} was extracted by using a channel resistance method [1]. This method involved plotting the total TFT on-resistance R_{tot} as a function of channel length L using the following equation:

$$R_{tot} = \frac{V_{DS}}{I_{DS}} = R_{SD} + \frac{L}{\mu_{eff} C_{ox} W (V_{GS} - V_{th})}, \quad (1)$$

where μ_{eff} and C_{ox} are the effective mobility and capacitance of gate insulator per unit area, respectively. Figure 4-1 shows the dependence of R_{tot} on L of the self-aligned ZrInZnO TFTs with W = 60 μm at V_{GS} = 12 – 15 V. Based on Eq. (1), R_{SD} was evaluated from the intersection point of the straight lines fitted to each R_{tot} (L, V_{GS}). The width-normalized R_{SD} ($R_{SD}W$) is evaluated to be 78.8 Ω cm. This low R_{SD} is resulted from low resistivity of the ZrInZnO S/D regions, which caused by the diffusion of tin into the S/D regions after being treated by the Sn:PPC solution. Since S/D current of the TFT is adversely impacted by R_{SD} [2-3], the increase in drain current of the TFT is contributed by the reduction in R_{SD}.

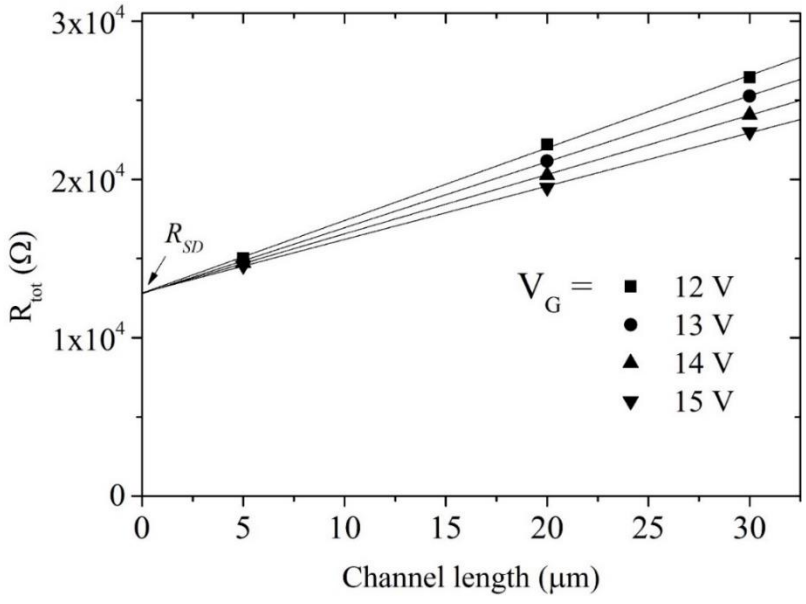


Figure 4-1. *Total TFT on-resistance R_{tot} as a function of channel length L*

2. Cut-off frequency of the self-aligned TFT and non-self-aligned TFT (inverted staggered):

The cut-off frequency of ZrInZnO TFTs with self-aligned structure and non-self-aligned (inverted staggered) structure was investigated. Figure 4-2 show cross-section schematic and optical microscopy image of the self-aligned and inverted staggered TFT with a channel width *W* and length *L* were 60 μm and 5 μm, respectively. The Pt gate, source and drain electrode, SiO_2 gate insulator, and ZrInZnO channel layer of both TFTs were fabricated as same conditions (refer to section 4.2_*Experimental procedure* for detailed information). The S/D regions of the self-aligned TFT were coated by the Sn:PPC solution 10 and annealed at 400 °C for 20 min under N_2. I supposed that the overlap areas between the gate electrode and source/drain region of the self-aligned TFT were about 0.1 × 60 μm for each side, which is due to diffusion of Sn into ZrInZnO channel during TFT fabrication process. Meanwhile, the overlap areas of the inverted staggered TFT estimated from the optical image were about 30 × 100 μm and 26 × 100 μm. Thus parasitic capacitance

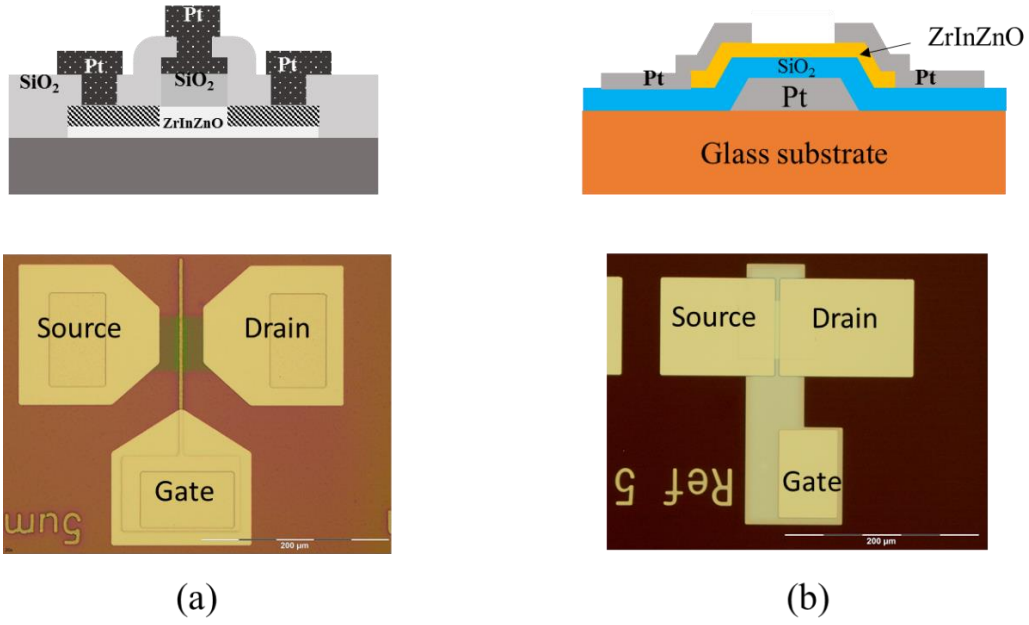


Figure 4-2. *Cross-section schematic and optical microscopy image of (a) self-aligned and (b) inverted staggered ZrInZnO TFT with a channel width and length of 60 μm and 5μm, respectively.*

of the self-aligned and inverted staggered TFTs with 115 nm-thick SiO_2 gate insulator were 0.0044 pF and 2.07 pF, respectively.

Figure 4-3 shows the transfer characteristics of the self-aligned and inverted staggered TFTs at drain voltage of 1 and 5 V. The channel width *W* and length *L* of the TFTs were 60 μm and 5 μm, respectively. The TFT parameters extracted from the transfer curves in Fig. 4-3 are detailed in Table 4-1 with cut-off frequency f_T. The inverted staggered TFT exhibited poorer TFT characteristics the self-aligned TFT. Figure 4-4 shows the output peak-to-peak voltage versus modulation frequency of the self-aligned and inverted staggered TFTs. To obtain the frequency properties of the self-aligned TFT we applied an ac voltage to drain electrode by using a function generator (Arbitrary waveform generator, Agilent 33220A). The peak-to-peak voltage was set as 2V. Bias drain (V_D) and gate (V_G) were applied with dc voltage sources set as 5 V. The output voltage was obtained using a digital oscilloscope. Meanwhile, for the inverted staggered TFT, we applied the ac voltage to the gate electrode. As can be seen in the Fig. 4-4, the value f_T of the self-aligned TFT is much higher than that of the inverted staggered TFT. However, the high value of f_T obtained for the self-aligned TFT is not only resulted from the reduction in parasitic capacitance but is also due to the increase in mobility. It was reported that a high f_T

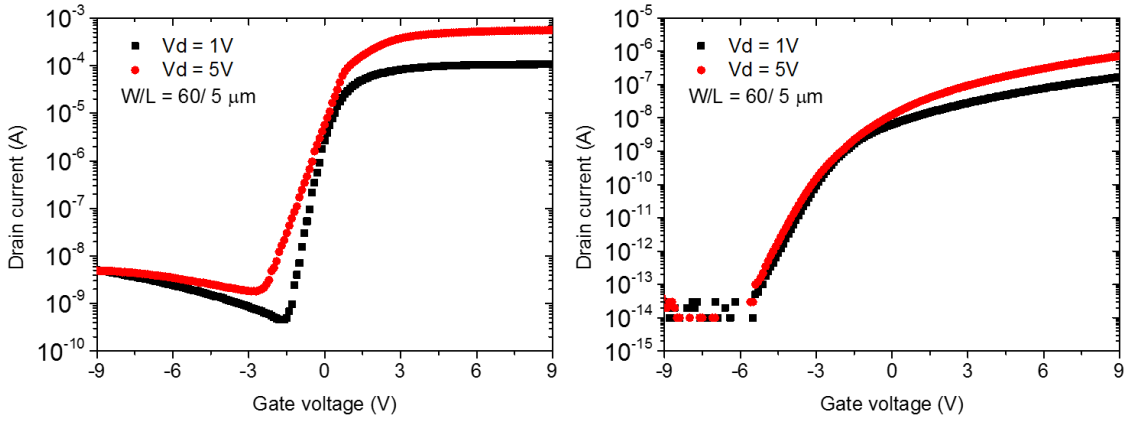


Figure 4-3. *Transfer characteristics of (a) self-aligned and (b) inverted staggered ZrInZnO TFT.*

Table 4-1. TFT parameters extracted from the transfer curves in Fig. 4-3 including the threshold voltage (V_{th}), field-effect mobility (μ), subthreshold swing (SS), on/off ratio, experimental and calculated cut-off frequency (f_T)

TFT structure	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	SS (V/dec)	On/Off ratio	Experimental f_T (Hz)	Calculated f_T (Hz)
Self-aligned	- 0.5	7.5	0.65	3.4×10^5	730×10^3	74.5×10^6
Inverted staggered	0.8	0.1	0.77	8.9×10^7	400	0.333×10^6

can be achieved by a transistor with high mobility, short channel length, low threshold voltage and low parasitic capacitance [4]. The cut-off frequency for a MOS transistor can be expressed as [5]:

$$f_T = \frac{g_m}{2\pi(C_i+C_p)} \qquad (4\text{-}1)$$

where g_m, C_i, and C_p are the transconductance, gate capacitance and parasitic capacitance, respectively. From Eq. 4-1, I calculated the f_T by using measured g_m and calculated C_p mentioned above. The calculated values of f_T for the self-aligned and inverted staggered TFTs were tabulated in Table 4-1. There are large differences between the experimental f_T and the calculated one. In the case of the self-aligned

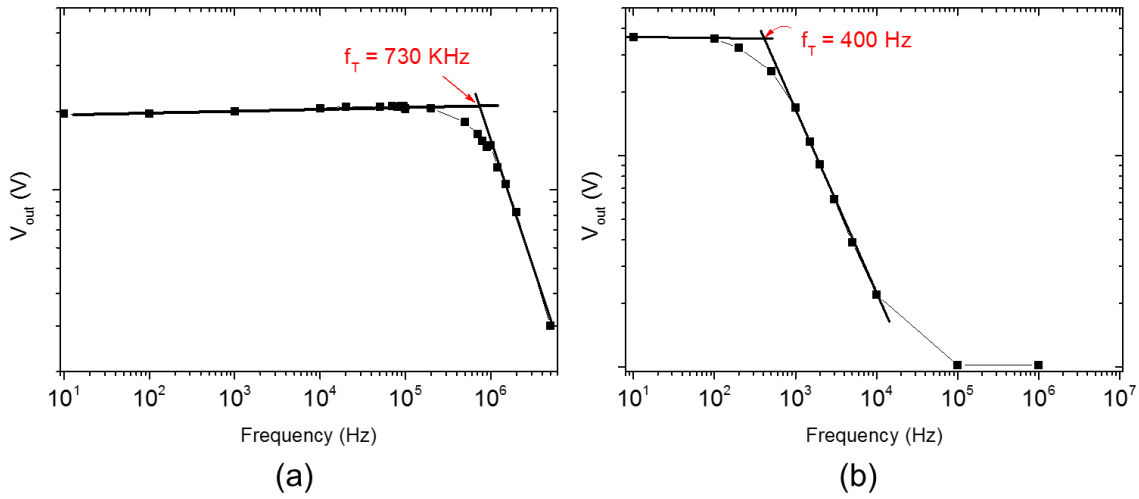


Figure 4-4. *Output peak-to-peak voltage versus modulation frequency of (a) self-aligned and (b) inverted staggered TFTs*

TFT, it was supposed that small experimental f_T is due to contribution of parasitic capacitance between the TFT electrodes and 500 nm-thick SiO_2/Si substrate. Therefore a glass substrate should be employed to improve the value of f_T.

3. Hydrogen diffusion from polysilazane-based SiO_2 gate insulator to ZrInZnO

In section 4.3.2 I presented the reduction in resistivity of the diffusion of ZrInZnO after being etched to removed SiO_2 gate insulator, which was suggested to be due to the diffusion of hydrogen atoms in polysilazane derived SiO_2 into the ZrInZnO during annealing process at 450 ^oC. To confirm this supposition I executed the FT-IR measurement for as fabricated ZrInZnO film and the ZrInZnO film etched by CF_4 for 16 min to remove SiO_2. The FT-IR absorbance spectra at 4000 – 500 cm^{-1} of the films were shown in Fig. 4-5. As can be observed in this figure, the peak corresponding to O-H vibration mode at approximately 3500 cm^{-1} of the ZrInZnO film etched by CF_4 for 16 min to remove SiO_2 was larger than that of as fabricated ZrInZnO film. This result confirmed that hydrogen was diffused into the ZrInZnO. It was suggested that hydrogen existed in ZrInZnO as –OH species, which is expected to work as a donor.

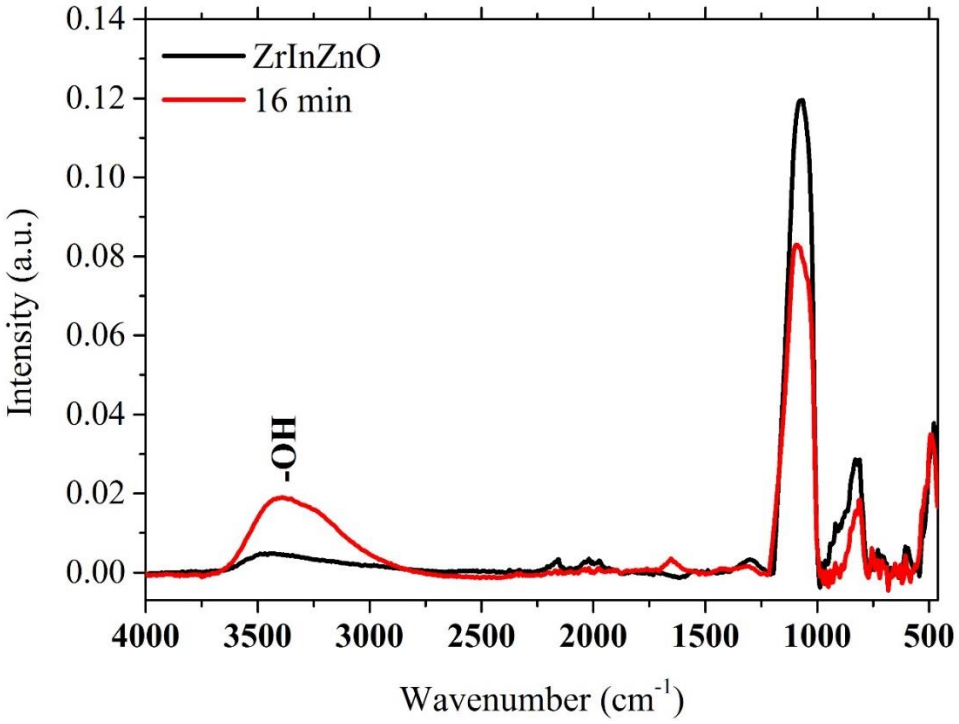


Figure 4-5. *FT-IR absorbance spectra of the ZrInZnO film and the ZrInZnO film etched by CF_4 for 16 min to remove polysilazane-derived SiO_2.*

Reference:

[1] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, IEEE Electron Device Lett. **1,** 3170 (1980).

[2] B. D. Ahn, H. S. Shin, H. J. Kim, J. S. Park, and, J. K. Jeong, Appl. Phys. Lett. **93**, 203506 (2008).

[3] J. S. Park, J. K. Jeong, Y. G. Mo and H. D. Kim, Appl. Phys. Lett. **90**, 262106 (2007).

[4] M. Kitamura, and Y. Arakawa, Appl. Phys. Lett. **95**, 023503 (2009).

[5] S. M. Sze, Semiconductor device physics and technology (second edition), John Willey & Sons, New York, (2002)

Chapter 5: Wet-annealed Polysilazane-derived SiO_2 gate insulator for further improvement

1. Bandgap of polysilazane-derived SiO_2

The band gap of the SiO_2 films was calculated from absorbance data by using the Tauc relation [1-2]:

$$(\alpha\hbar\nu)^{1/n} = A(\hbar\nu - E_g) \tag{5-1}$$

where A is a constant, α is absorption coefficient, E_g is band gap, $\hbar\nu$ is photon energy and n is an index characterizing the type of optical transition, it is equal to ½ for direct transitions and 2 for indirect transitions.

The absorbance data of the polysilazane-derived SiO_2 coated on quartz substrate was taken for λ = 190 – 900 nm using ultraviolet and visible (UV-vis) spectrophotometer

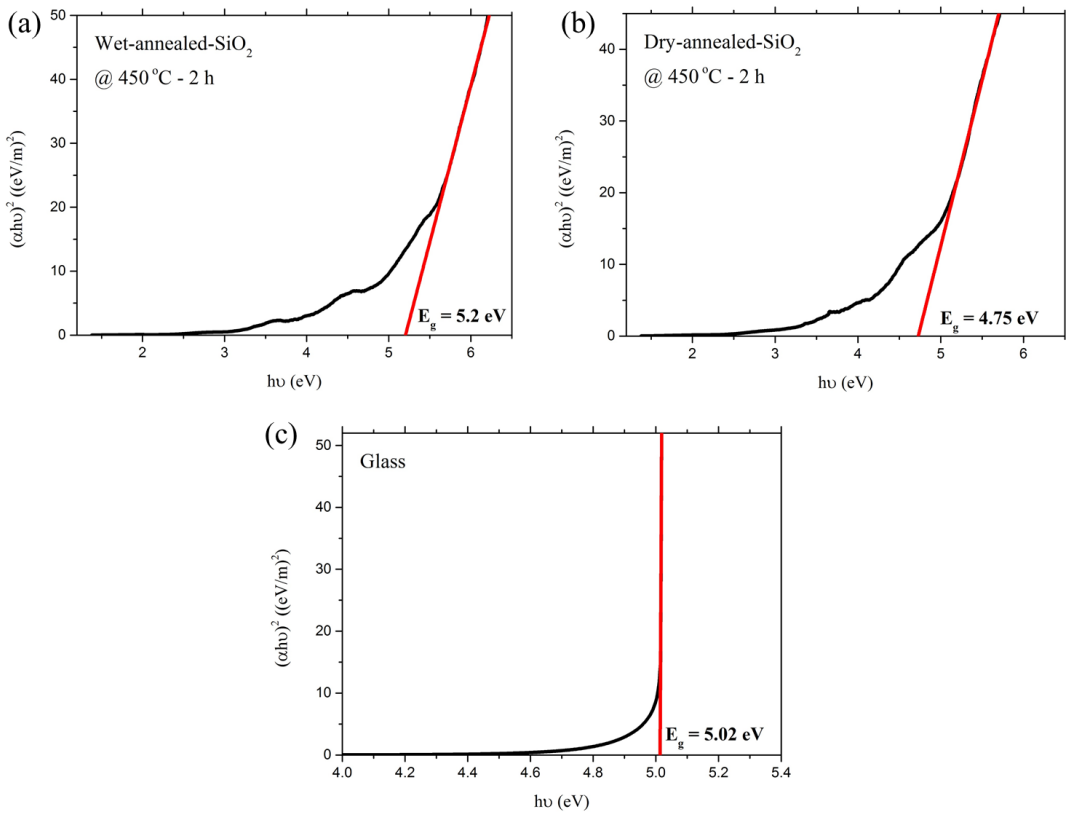


Figure 5-1. *Tauc's plot of* $((\alpha\hbar\nu)^2$ *against* $\hbar\nu$ *for 440 nm-thick wet-annealed* SiO_2 *and dry-annealed* SiO_2 *film, and 0.7 mm-thick glass substrate.*

(V-630, JASCO) at room temperature. The SiO_2 films were annealed at 450 ºC for 2 h.

Figure 5-1 shows Tauc's plot for determination of direct band gap of 440 nm-thick wet-annealed SiO_2 and dry-annealed SiO_2 film, and 0.7 mm-thick glass substrate. The band gap E_g of the wet-annealed SiO_2, dry-annealed SiO_2 film and fused glass substrate is calculated to be 5.2, 4.75 and 5.02 eV, respectively. The wet-annealed SiO_2 had larger value of band gap than the dry-annealed SiO_2. However, the band gap of the SiO_2 films obtained by this method is much smaller than that obtained by reflectivity measurements and photoconductivity measurements (8 – 11 eV) [3-5]. It was supposed that this is due to the limitation of our measurement system in which photon energy is limited at 6.5 eV. Other measurements, such as deep UV spectroscopic ellipsometry, reflectivity or photoconductivity should be carried out to confirm value of band gap of the polysilazane-derived SiO_2.

2. C-V measurement

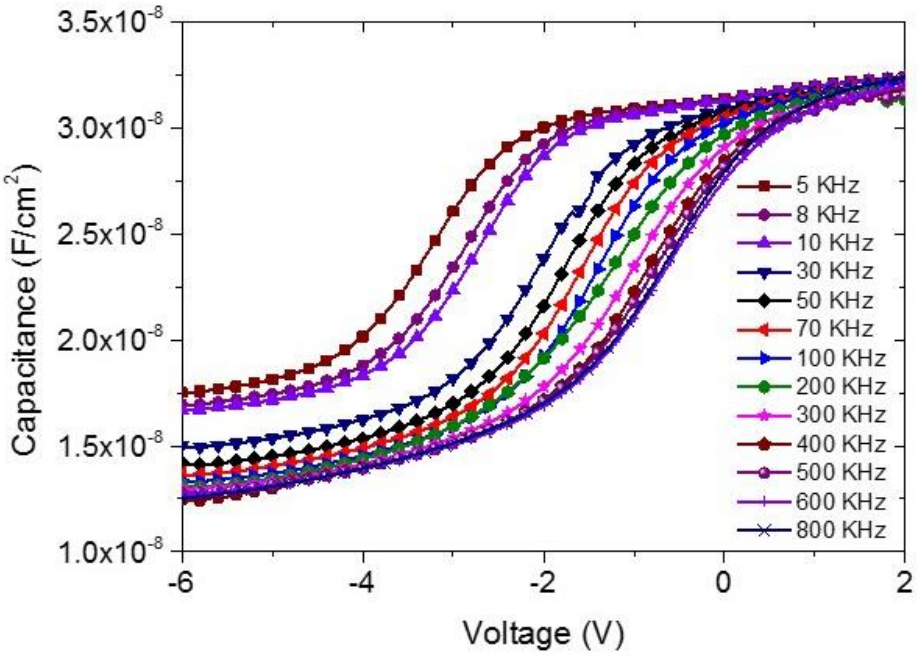


Figure 5-2. *C-V curves for NIMS capacitors with wet-annealed SiO_2 gate insulator measured at various frequency.*

Figure 5-2 shows C-V curves of MIMS capacitors with Al/wet-annealed-SiO_2/ n-Si/Al structure measured from inversion to accumulation at different frequencies (5 KHz – 800 KHz). The C-V curves exhibited a well-pronounced frequency dispersion. When the frequency was decreased, the C-V curves were shifted in the direction of negative bias. It was suggested that the dispersion of the C-V curves resulted from the existence of the interface traps between the wet-annealed SO_2 and semiconductor interface [6-10]. Under high frequency (f > 300 KHz) the dispersion was very small, which is due to the fact that the interface traps do not follow the ac gate voltage at a high frequency.

Reference:

[1] P. S. Kireev, Semiconductor Physics (second edition), Mir Publishers, Moscow, 1978.

[2] S. Ilican, Y. Caglar, and M. Caglar, J. Optoelectron. Adv. M., **10**, 2578 (2008).

[3] W.R. HUNTER, and S.A. MALO, J. Phys. Chem. Solids, **30**, 2739 (1969).

[4] E. LOH, Solid State Commun., **2**, 269 (1964).

[5] T.H. DiStefano and D.E. Eastman, Solid State Commun., **9**, 2259 (1971).

[6] I. Dokme, S. Altındal, Physica B **391**, 59 (2007).

[2] F. Bellenger, M. Houssa, A. Delabie, V. Afanasiev, Conard, M. Caymax, M. Meuris, K. De Meyer, and M. M. Heyns, J. Electrochem. Soc., **155**, G33 (2008).

[8] S. Huang, S. Yang, J. Roberts, and K. J. Chen, Jpn. J. Appl. Phys., **50**, 110202 (2011).

[9] J. C. Liao, Y. K. Fang, C. H. Kao, and C. Y. Cheng, IEEE Electron Device Lett., **29**, 477 (2008)

[10] M. D. Jacunski, M. S. Shur, and M. Hack, IEEE Trans. Electron Devices, **43**, 1433 (1996)

List of publication

Paper:

1. **H. T. C. Tu**, S. Inoue, P. T. Tue, T. Miyasako, T. Shimoda, "Investigation of Polysilazane-Based SiO_2 Gate Insulator for Oxide Semiconductor Thin-Film Transistors," IEEE Trans. Electron Devices **60**, 1149 (2013).
2. **H. T. C. Tu**, S. Inoue, T. Shimoda, "Wet-Annealed Polysilazane-derived SiO_2 Gate Insulator for ZrInZnO Thin-Film Transistors", Japanese Journal of Applied Physics (*under preparation*)
3. **H. T. C. Tu**, S. Inoue, K. Nishioka, N. Fujimoto, S. Karashima, T. Shimoda "Fabrication of source and drain regions of self-aligned ZrInZnO thin-film transistors using a solution of tin and poly (propylene carbonate)" Japanese Journal of Applied Physics (*in press*)
4. P. T. Tue, T. Miyasako, J. Li, **H. T. C. Tu**, S. Inoue, E. Tokumitsu, T. Shimoda, "High-performance solution-processed ZrInZnO thin-film transistors," IEEE Trans. Electron Devices **60**, 320 (2013).

Proceedings:

1. **H. T. C. Tu**, S. Inoue, P. T. Tue, T. Shimoda, "Solution-processed ZrInZnO thin film transistor with polysilazane-derived SiO_2 gate insulator" NMD-087-P, 4^{th} IWNA 2013, 14-16 November 2013, Vung Tau, Vietnam.
2. **H. T. C. Tu**, S. Inoue, K. Nishioka, N. Fujimoto, S. Karashima, T. Shimoda, " Fabrication of a Self-aligned ZrInZnO thin film transistor using propylene carbonate solution" P-1/H. T. C. Tu, SID 2014 DIGEST, 1-6 June 2014, San Diego California, USA.

International Conference:

1. **H. T. C. Tu**, S. Inoue and T. Shimoda, "Wet-annealed Polysilazane-based SiO_2 Gate Insulator for Amorphous Oxide Semiconductor Thin-Film Transistor", The 4th International Symposium on Organic and Inorganic Electronic Materials and Related Nanotechnologies (EM-NANO 2013), A3-3, 18 (oral presentation)

2. **H. T. C. Tu**, S. Inoue, P. T. Tue, T. Shimoda, "Solution-processed ZrInZnO thin film transistor with polysilazane-derived SiO_2 gate insulator" 4th IWNA 2013 International Workshop on Nanotechnology and Application, Vung Tau, Vietnam, November 14-16, 2013 (poster presentation)

3. **H. T. C. Tu**, S. Inoue, K. Nishioka, N. Fujimoto, S. Karashima, T. Shimoda, " Fabrication of a Self-aligned ZrInZnO thin film transistor using propylene carbonate solution" SID 2014 DIGEST, 1-6 June 2014, San Diego California, USA.