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| Title | Applying Write-Once Memory Codes to Asymmetric Multiple Access Channels |
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Abstract

Write-once memory (WOM) is a form of digital memory for the permanent storage of information. WOM codes were first designed by Rivest and Shamir, which allows reuse of such that WOM. Our work is inspired in part by application of WOM codes to reducing read latency in memories. We focus on applying WOM codes to a specific asymmetric multiple access channel (AMAC) noise model called the binary symmetric AMAC (BS-AMAC). The AMAC is a kind of the multiple access channel (MAC), which consists of two users simultaneously communicate over one common channel, however User 2 observes User 1 message.

At one specific rate pair, WOM codes can achieve the BS-AMAC maximum sum-rate. Further, any achievable rate pairs for a two-write WOM code are also an achievable rate pair for the BS-AMAC.

Numerous schemes for joint iterative decoding of two transmitted codewords at the receiver have been proposed. Successive interference cancellation is another well-known technique, however requires interaction between two decoders. Our scheme applying WOM codes to the BS-AMAC, which reduces the size of the achievable rate region, however induces effective decoding schemes: (1) symbolwise estimation and (2) a posteriori decoding, without using joint iterative decoding or successive interference cancellation. Achievable rates of our system using two decoding schemes are also given. These two decoding schemes are effective in cooperative wireless communications despite the fact that WOM codes are designed for data storage.

In order to build more reliable communication system, some capacityapproaching error correcting codes such as low-density parity check codes (LDPC) are needed. In our work, we applied the well-known DVB-S.2 LDPC codes to our system in order to approach the BS-AMAC capacity. A bit error rate (BER) performance of our system using a LDPC code is shown.

We also briefly discuss how the AMAC model can be applied to the relay channel.

key words: asymmetric multiple access channel, data storage code, write-once memory code, capacity, achievable rate region