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論文題目	Study of the Physical Properties of Graphene Nano-Ribbon Band-to-Band Tunnel Transistor （グラフェンナノリボン-バンド間トンネルトランジスタにおける物理特性の研究）			
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論文の内容の要旨

1 Background

The performance of Very Large Scale Integration circuits has been gradually improved by scaling down device dimensions. However, the heat dissipation issue is becoming more critical and harder to solve for CMOS while keeping the previous scaling down trend. Thus, due to the subthreshold swing (SS) of the Metal-oxide-semiconductor field effect transistor (MOSFET) is limited to 60 mV/decade, it is hard to scale the drain voltage V_D while increasing the speed and maintaining low off-state power dissipation. Tunnel Field Effect Transistors (TFET) have attracted much interest due to their low OFF current (I_{OFF}) and the possibility of reaching a SS below the limit (60 mV/decade) of standard CMOS technology. However, all experimentally realized TFETs based on conventional semiconductors exhibit low ON-state current (I_{ON}), which limits their usefulness in integrated circuits.

Due to the atomically thin nature, width tunable bandgap, and low effective mass, Graphene Nano-Ribbons (GNR) is seen as one of the most promising materials to overcome the limitations of conventional TFETs. However, realizing a reliable GNR-TFET is quite challenging. To introduce a reasonable energy gap to the GNR, the width should be around 10 nm, which is a very tough task to achieve. Also, GNR edge states and quantum condiments come to the pictures at such narrow ribbons. All of these challenging and difficulties should be taken into consideration during the fabrication of the GNR-TFET

2 Aim

There has not been any experimental report of GNR-TFET operation until now. Therefore, this dissertation investigates and studies the feasibility of realizing GNR-TFETs and aim to:

- Demonstration of band-to-band tunneling(BTBT) based GNR-TFET
- Demonstrate I_{ON} > conventional TFET

This includes understanding the physics of the GNR *p-n* junction because a TFET is, in principle, a reverse biased *p-i-n* junction. To achieve my target, first I planned to fabricate and study physical properties of GNR *p-n* junction, secondly fabricate and study GNR-TFET.

3 Experimental Results and discussion

[redacted] GNR *p-n* Junction

3.1.1 Realization of GNR *p-n* junction

In the current work, our GNR width is ~ 15-nm with an estimated E_g in the order of 44 meV. The GNR used here has been fabricated from single layer CVD graphene supported by a SiO_2/Si substrate. Two independent top gates, with separation of ~ 40 nm, are used to define the GNR *p-n* junction under investigation (see Fig. 1a). To confirm the functionality of each gate and the performance of the GNR, the I_d measured as a function of gate voltage (V_{Tg}) at constant V_d. Room temperature measurement (shown in Fig. 1b), in general, demonstrates that all the gates including back-gate show good I_d modulation. To achieve all the possible coping combinations of the device, one of the top gate voltages (V_{Tg1} and V_{Tg2}) is swept from - 4V to 4V (-5V to 5V at low temperature) with the other top gate voltage stepped in the same range. V_d is fixed at 3 mV for all measurements at 25 K and above, and 12 mV below due to the high current suppression at lower temperatures. The contour plot of I_d as a function of both top gate voltages illustrates the key features of our device (see Fig. 1c). First, four distinct regions belonging to the four possible configurations (*pn, np, pp, and nn*) are clearly visible. Secondly, the low current region is slightly slanted, which means that there is a weak capacitive interaction between the two top gates. Therefore, GNR *p-n* junction successfully realized.

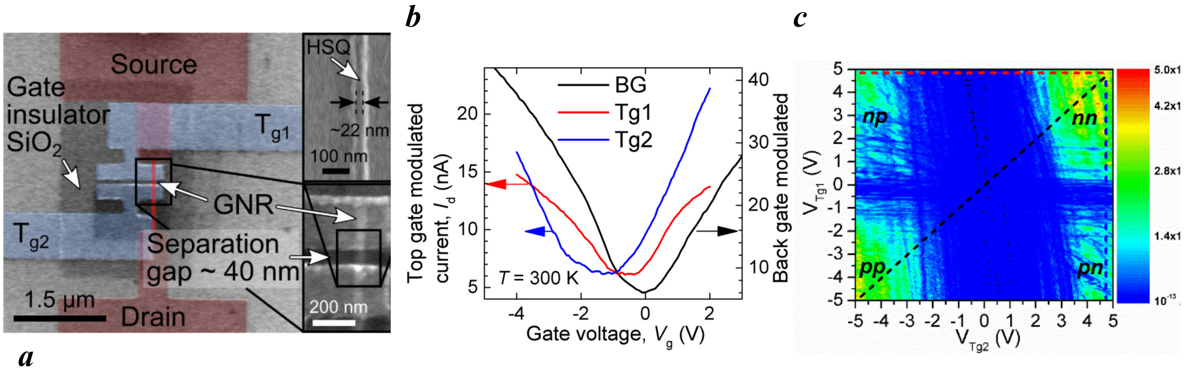

Figure 1. (a)SEM image of the two top gate device structures. Fake colours are applied for better understanding. (b) Back gate (bg) modulation and Top gate modulation. (c) Contour plot of drain current as function of the top gate voltages at T = 10 K. Drain voltage Vd is 12 mV. The clearly defined doping regions induced by the electrostatically

doping are indicated by np, nn, pn, and pp, respectively.

3.1.2 Transport characteristics of GNR *p-n* junction

The drain current (I_d) at 10 K is shown for different gating configurations in Fig. 2. When using the global back gate (Fig. 2a), a symmetric modulation is observed with some random oscillation around the CNP at V_g = -0.5 V with ON/OFF ratio ~ 10^5. The symmetric modulation is consistent with the 300 K measurement shown in Fig. 1b. In contrast to the global back gate (Fig. 2a), when fixing one of the top gates and sweeping the other one, a remarkable step change in the drain current is observed. For fixed V_{Tg1} = 4.9 V (Fig. 2b, corresponding to np biasing), the step change with a rate of ~ 42 mV/dec over a range five order of magnitude in drain current (~$5x10^5$) is observed at $V_{Tg2} \approx$ -1 V. The OFF-state current is at least one order of magnitude lower than for the back gate modulated current. In case of a fixed V_{Tg2} = 4.9 V (Fig. 2c, *pn* biasing), the rate of the step change at $V_{Tg1} \approx$ -0.8 V is ~32 mV/dec but only over a range of four order of magnitude in drain current (~$1.1x10^4$). Furthermore, the current is only very slightly affected by the V_{Tg1} outside of the suppression region.

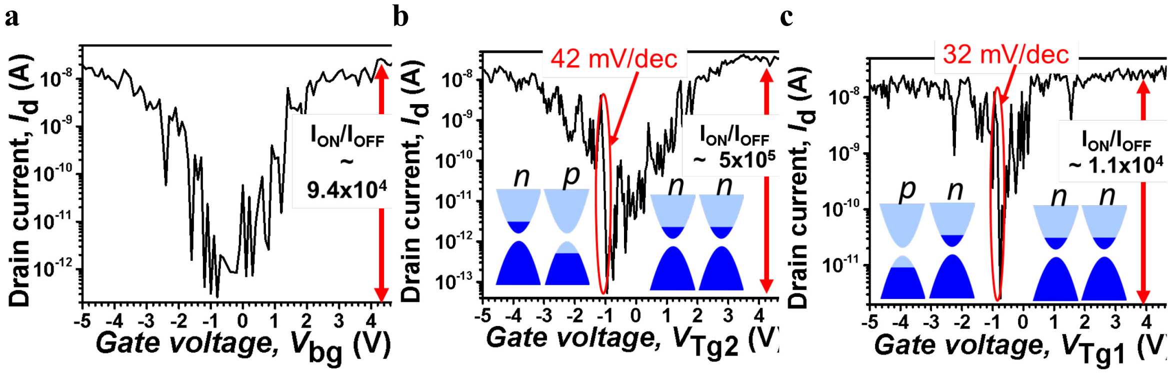

Figure. 2 Drain current as a function of gate voltage at T = 10K and V_d = 10 mV: (a) Back gate voltage sweep (b) T_{g2} sweep at V_{Tg1} = 4.9 V. The device is switched from nn configuration to pn configuration by sweeping V_{Tg2} from 5 V to -5 V (forward biasing (c) V_{Tg1} sweep at V_{Tg2} = 4.9 V (reverse biasing) showing similar characteristics with 32 mV/decade in the sharp switching region over four orders of magnitude

3.1.3 Origin of sharp switching

The sharp switching was observed in the np and pn biasing condition at low temperature (Fig. 2b and c), when one of the gates is biased so that the valence band edge in the variable gate region is lifted into the bias window and at the same time above the conduction band edge in the fixed gate region. We can thus sketch the simplified band structure of the p-n junction as shown in Fig. 3. In the uniformly nn-doped state, a large drift current is enabled. As the energy of the band edges in the T_{g2} region are shifted up, the drift current is reduced and a thermally activated leakage current dominates the transport. Finally, as the band overlap occurs, the tunneling width W_T is abruptly reduced. As the tunneling window is formed in the bias window (between E_{FD} and E_{FS}), the large number of available charge carriers enables the increase of the drain current over five orders of magnitude with the sharp slope. As the tunneling energy window is further increased (V_{Tg2} is further decreased), the sharp switching saturates because the transport through the remaining parts of the channel limit the allowed current.

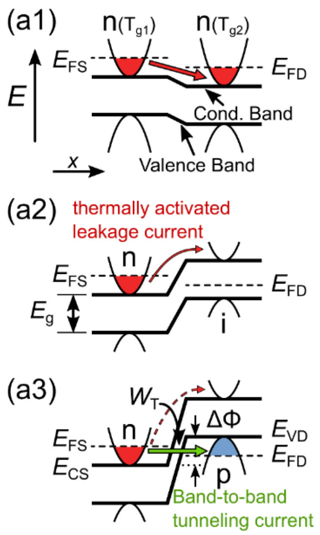

Figure 3. Proposed band structure model of p-n junction.

[redacted]Triple-Gate GNR-TFET

BTBT behavior was reported in the GNR *p-n* junction with two top gates. However, to make the device usable as a switch with superior behavior to the silicon MOSFET, it is necessary to control the intrinsic region. This can be achieved by fabricating a third top gate. Here we report, for the first time, band-to-band tunneling in a sub-10 nm GNR controlled triple top gate transistor. AFM image of the fabricated device is shown in Fig. 4a. the narrower GNR at the center of the channel and wider graphene acting as extension of the source and drain contacts are covered by the SiO_2 and top gates but still visible. Detailed dimensions of the device are presented in Table 1.

Table 1. Tri-gate device dimensions

L_{ch}	L_{Tg1}	L_{Tg2}	L_{Tg2}	d
500 nm	280 nm	70 nm	280 nm	30 nm

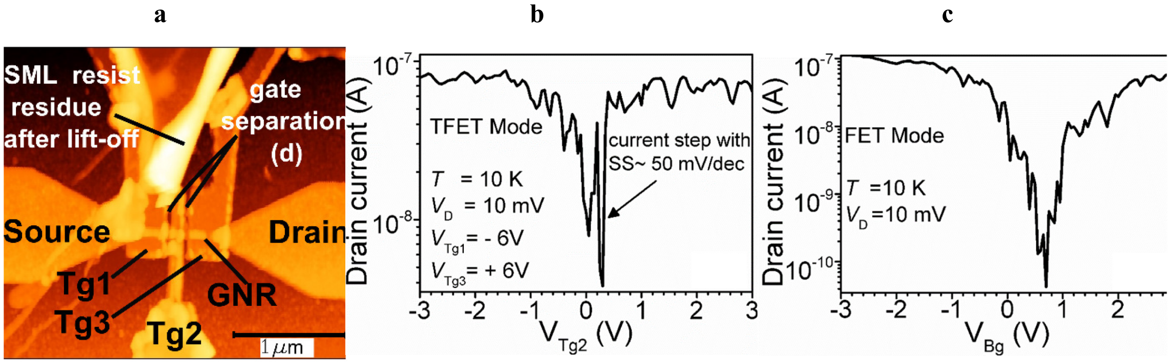

Figure 4 (a) AFM image of the measured device shows the separation d ~ 30 nm between the top gates above the GNR, and the HSQ etching mask of ~ 30 nm width. (a) Drain current as a function of the back-gate voltage (FET mode). Top gates are floating. (b) TFET mode: The middle gate voltage (V_{Tg2}) is swept from -3 V to 3 V, while the V_{Tg1} and V_{Tg3} are fixed at -6 V and 6 V, respectively.

3.2.1 Transport characteristics

To ensure that the carrier transport characteristics through our device is due to the BTBT, we compare the characteristics of the device in the TFET (realized by top gates) (shown in Fig. 4b) and FET (realized by back gate) configurations (shown in Fig. 4c), respectively. In all measurements shown here the source-drain voltage (V_D) is fixed at 10 mV ($V_D < E_g/2$) to decrease the ambipolarity and I_{OFF}. As can be seen in Fig. 4c, in the case of FET mode, the drain current (I_D) shows clear ambipolar behavior with high I_{ON}/I_{OFF} ratio of ~ 2.5x10^3. In contrast, in the TFET mode I_D shows a steep current jump followed by a remarkable current saturation (I_{ON}) when V_{Tg2} is swept in the positive direction (*n*-type conduction), see Fig. 4b. However, the clearly different transfer characteristics between the two modes indicate that the carrier's injection mechanisms are different. Therefore, to clarify the difference between the two modes, I will discuss the temperature dependence of the SS next.

3.2.2 Temperature dependence of subthreshold slope

The I_D-V_{Tg2} characteristics of our device operated in TFET mode between 10 and 300 K are shown in Fig. 5a. At low temperature, the current has a sharp slope (SS ~ 47 mV/dec). By increasing the temperature, the current transition slope decreases (larger SS). The extracted values of SS from the I_D-V_{Tg2} curves in Fig. 5b show temperature independence up to 40 K, followed by a gradual increase with temperature up until 100 K (SS ~ 180 mV/dec). Above 100 K, an exponential increase of SS is observed, finally reaching 8.4 V/dec at 300 K. On the other hand, in the FET mode, the SS shows linear temperature dependence over the whole range of temperatures (10 to 300 K), similar to the thermal limit of the

MOSFET (see Fig. 5c). This remarkable inversion of the SS, together with the temperature independence at low temperature in the TFET configuration is a substantial evidence that the drain current does not originate from the thermionic emission and is due to BTBT.

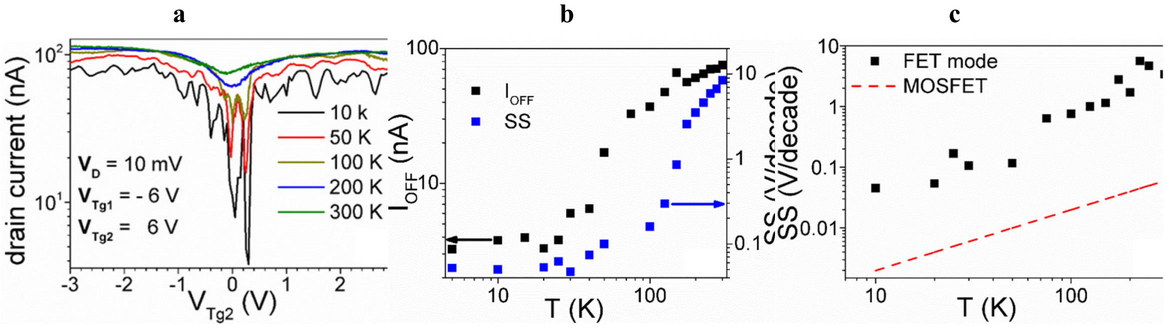

Figure 5. (a) I_D-V_{Tg2} at different temperatures for TFET mode. V_{Tg1} and V_{Tg3} are fixed at – 6 V and + 6 V, respectively, and V_D is 10mV. (b) The extracted values of I_{OFF} and SS from I_D-V_{Tg2} curves in (a). (c) SS as a function of temperature of our device in FET mode and the thermal limit of the MOSFET

論文審査の結果の要旨

　現在の大規模集積回路では、微細化されたMOSFETのオフリーク電流による待機時消費電力の増大が深刻な問題となっている。そのため新たなスイッチングデバイスとして、オフリーク電流が低く、S 係数< 60 mV/decの急峻なスイッチングが可能なトンネルトランジスタ(TFET)が注目されている。しかし、現在研究が進められている半導体ベースのTFETでは、バンドギャップが大きいため、そのON電流はMOSFETに比べて２～３桁小さく、高速回路動作を実現できないという大きな問題が存在する。

　これに対して、本研究では、バンドギャップが0である原子層材料グラフェンを、微細加工技術によりグラフェンナノリボンに加工し、量子閉じ込め効果により小さなバンドギャップを形成することで、ON状態で高いトンネル電流を実現するグラフェントンネルトランジスタ(GTFET)を提案するとともに、その基本動作原理の検証を試みた。まず、大面積CVDグラフェン膜を用いて、電子線直接描画により、幅約30nmのグラフェンナノリボン上に２つの制御ゲート電極を有する素子を試作し、グラフェントンネルトランジスタ実現の上で重要となるp型・n型領域を電気的に形成し、非常に小さなクロストークの範囲で独立に制御できることを示した。このグラフェンPN接合素子を用いて、バンド間トンネル電流をオン･オフ比 ～ 5 x 10^5で急峻にスイッチングできることを初めて実証した。次に、サブ20 nm微細加工用電子線レジストHSQを用いて、幅約15 nmグラフェンナノリボンチャネルと、電極間隔23 nmの３つの近接制御ゲート電極を有するGTFET素子を作製し、低温領域（T＜

40 K）でS係数～47 mV/decの急峻スイッチングを観測することに成功した。また、測定されたS係数の温度依存性データは、アレニウスプロットで評価した極細GNRチャネルのバンドギャップ値Eg ～ 70 meVを用いたバンド間トンネリング理論モデルとよく一致することを見出した。

以上、本論文は、これまでグラフェン特有のクライントンネリング現象のため、実験的検証が困難であったグラフェンナノリボン PN 接合におけるバンド間トンネリング現象の観測と、そのトンネル電流をゲート電極で制御して動作する GTFET の基本動作原理を初めて実験的に検証することに成功した独創性の高い研究であり、学術上・応用上両方の観点から価値の高いものである。よって博士（マテリアルサイエンス）の学位論文として十分価値あるものと認めた。