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Suppression of drain-induced barrier lowering by double-recess overlapped gate structure in normally-off AlGaN-GaN MOSFETs

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We investigated drain-induced barrier lowering (DIBL) in normally-off AlGaN-GaN metal-oxide-semiconductor field-effect transistors (MOSFETs) with a double-recess overlapped gate structure. It is found that the double-recess overlapped gate structure can suppress DIBL; the threshold voltage is constant without lowering for high drain-source voltages, and sub-threshold characteristics remains excellent. We elucidate the mechanism of the DIBL suppression by considering a local potential in the MOSFETs. In addition, it is also found that the double-recess overlapped gate structure is beneficial for current collapse suppression. *Published by AIP Publishing.*
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AlGaN-GaN field-effect transistors (FETs)[1] are attractive for use in high-power and high-frequency applications.[2] While AlGaN-GaN FETs in many cases are normally-on devices with a negative threshold voltage, normally-off devices with a positive threshold voltage are highly desirable for fail-safe operations. In order to realize normally-off AlGaN-GaN FETs, several methods have been studied using a thin-AlGaN layer,[3,4] gate recess,[5–13] a p-type (Al)GaN cap layer,[14,15] fluoride plasma treatment,[16] selective electrochemical oxidation,[17] and interface charge engineering.[18] In particular, the gate recess method has been frequently employed, where the AlGaN barrier under the gate is recess-etched. There are two categories of the gate recess method: the partial recess method,[5–9] in which a thin AlGaN layer remains in the recess region, and the full recess method,[10–13] in which etching through to the GaN removes the AlGaN barrier completely in the recess region. Although the partial recess method is suitable to obtain normally-off FETs with a low on-resistance and a high drain current, since the remaining AlGaN layer thickness significantly affects the threshold voltage,[19] extremely high precision control of the etching depth is required for threshold voltage control. This is a crucial problem in manufacturing stability. On the other hand, the full recess method, in which the etching depth does not affect the threshold voltage, is advantageous for threshold voltage control and manufacturing stability. The major disadvantage of AlGaN-GaN metal-oxide-semiconductor FETs (MOSFETs) obtained by the full recess method is a high on-resistance caused by a low electron mobility at the oxide/etched-GaN interface. Thus, in order to realize a low on-resistance in fully-recessed AlGaN-GaN MOSFETs, a short gate length is desirable. In general, however, short-gate FETs often suffer from short-channel effects, such as negative threshold voltage shifts and degradation of sub-threshold characteristics owing to drain-induced barrier lowering (DIBL),[20–22] which are quite serious for normally-off AlGaN-GaN MOSFETs. In order to suppress DIBL, it is effective to relieve the electric field at the gate-drain edge. Lu *et al.* investigated AlGaN-GaN MOSFETs with a single-recess overlapped gate structure (SRO), where the gate electrode overlaps both fully-recessed and non-recessed regions, showing a low on-resistance, a high threshold voltage, and a high breakdown voltage.[23] Although DIBL was not studied in Ref. 23, the gate structure is considered to be effective for DIBL suppression due to the fact that the high breakdown voltage is realized by relieving the electric field at the gate-drain edge. In this work, we investigated DIBL in AlGaN-GaN MOSFETs with a double-recess overlapped gate structure (DRO), where the gate electrode overlaps both fully-recessed and partially-recessed regions, comparing with SRO. As a result, it is found that DRO can more strongly suppress DIBL than SRO. In addition, it is also found that DRO is more beneficial for current collapse suppression.

We fabricated short-gate AlGaN-GaN MOSFETs with DRO, SRO, and a reference non-overlapped gate structure (Ref.), whose schematic cross sections are shown in Figs. 1(a)–1(c), respectively. The fabrication process is as follows. For an n-GaN(5 nm)/$Al_{0.2}Ga_{0.8}N$(22 nm)/GaN(2 μm) heterostructure grown by metal-organic chemical vapor deposition on a semi-insulating SiC substrate, device isolation was achieved by ion implantation. Ohmic recess and following gate recess were carried out by conventional dry etching using BCl_3/Cl_2 mixture gas. The ohmic recess depth is ∼10 nm. For the gate recess of DRO, as shown in Fig. 1(a), a fully-recessed region (∼40 nm depth, ∼150 nm length) and a partially-recessed region (∼22 nm depth, i.e., AlGaN remaining thickness ∼5 nm, ∼1.5 μm length) are formed, while only a fully-recessed region is formed for the gate recess of SRO and Ref., as shown in Figs. 1(b) and 1(c). By using atomic force microscope, it is confirmed that the designed etching depth profiles are realized. As a gate dielectric, a 20-nm-thick Al_2O_3 film was deposited by atomic layer deposition using trimethylaluminum and oxygen plasma.

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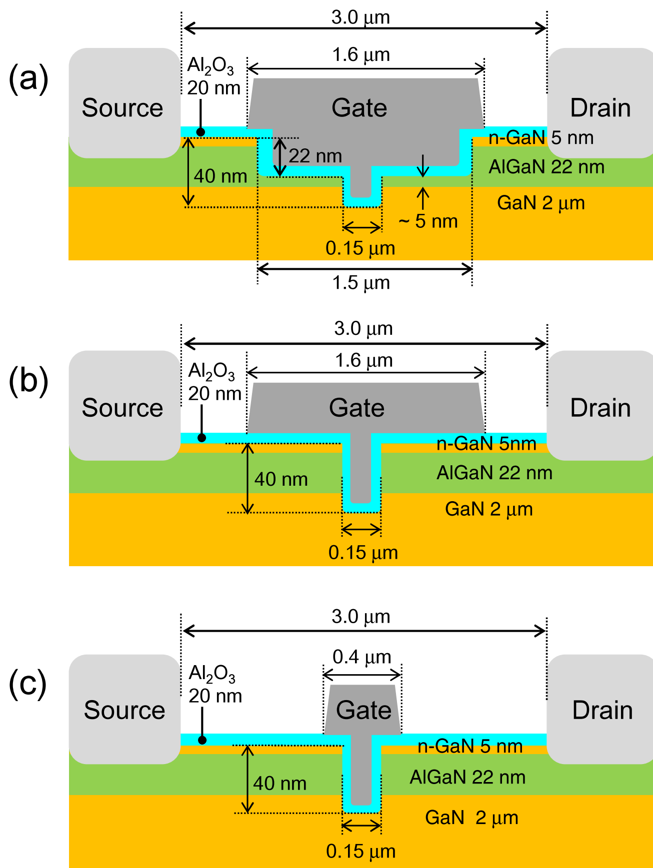

FIG. 1. Schematic cross sections of AlGaN-GaN MOSFETs with (a) DRO, (b) SRO, and (c) Ref.

Aluminum-based ohmic electrodes were formed on the ohmic recess region after Al_2O_3 film removal, where transmission line model measurements show a contact resistance of $\sim 0.3\ \Omega$ mm. Finally, Ni gate electrodes were formed on the Al_2O_3 gate insulator, as shown in Figs. 1(a)–1(c), where the gate-length is ~ 150 nm corresponding to the fully-recessed region.

Figure 2 shows linear-scale gate characteristics (drain current I_D vs. gate-source voltage V_{GS}) of the AlGaN-GaN MOSFETs with (a) DRO, (b) SRO, and (c) Ref. The drain-source voltages are V_{DS} = 1, 5, 10, and 15 V and the voltage sweep is $V_{GS} = +4 \rightarrow -3$ V. For SRO and Ref., we observe negative threshold voltage shifts owing to DIBL, where the latter exhibits more significant shifts. In contrast, for DRO, DIBL is suppressed; almost no shifts are observed. Figure 3 shows threshold voltages V_{TH} depending on V_{DS}. We can confirm no DIBL for DRO in the range of V_{DS} = 1-15 V. On the other hand, for SRO, we find that DIBL occurs in the range of V_{DS} = 1-7 V, but is suppressed in the range of $V_{DS} > 7$ V. For Ref., more significant DIBL occurs in the range of V_{DS} = 1-15 V. Both types of the recess overlapped gate structures, DRO and SRO, are effective for DIBL suppression. However, while SRO does not suppress DIBL in the low V_{DS} range, DRO completely suppresses DIBL.

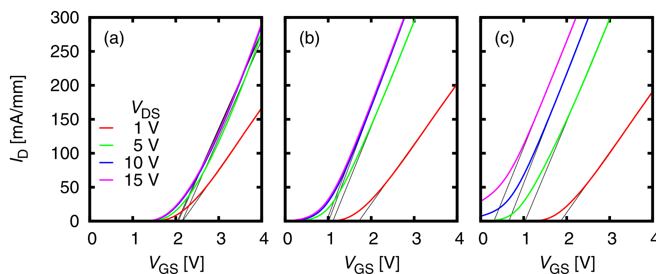

FIG. 2. Linear-scale gate characteristics (I_D-V_{GS}) for (a) DRO, (b) SRO, and (c) Ref. The drain-source voltages are V_{DS} = 1, 5, 10, and 15 V, and the voltage sweep is $V_{GS} = +4 \rightarrow -3$ V.

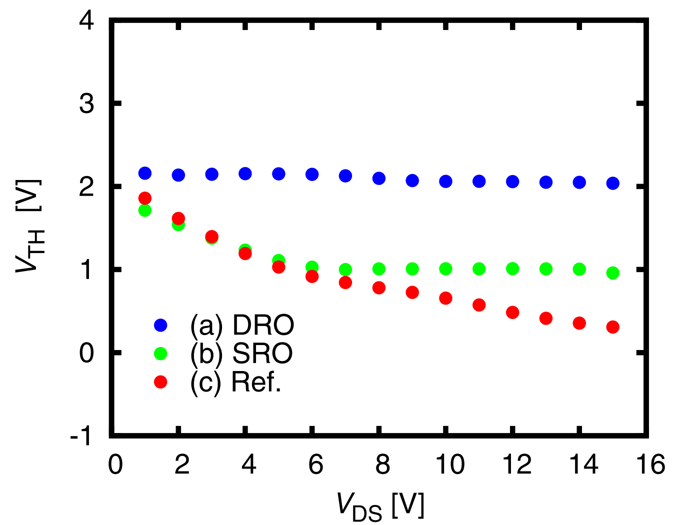

FIG. 3. Threshold voltages V_{TH} depending on V_{DS} for (a) DRO, (b) SRO, and (c) Ref.

The effect of DIBL suppression for DRO is noticeable in the sub-threshold regime. Figure 4 shows logarithmic-scale gate characteristics for (a) DRO, (b) SRO, and (c) Ref., at V_{DS} = 15 V under the voltage sweep of $V_{GS} = +4 \rightarrow -3$ V. Figure 5 shows sub-threshold slope $SS = [\partial(\log I_D)/\partial V_{GS}]^{-1}$ as functions V_{GS} for (a) DRO, (b) SRO, and (c) Ref., at V_{DS} = 1, 5, 10, and 15 V. For DRO, we observe excellent sub-threshold characteristics and the minimum $SS \sim 90$ mV/decade. In contrast, we find poor sub-threshold characteristics for SRO and very poor one for Ref., both resulting in large leakage currents at $V_{GS} = 0$ V. The degradation in sub-threshold characteristics due to DIBL is a very serious problem in normally-off devices. DRO is effective for suppressing not only the negative threshold voltage shifts, but also the degradation in sub-threshold characteristics.

In order to elucidate the mechanism of the DIBL suppression in the DRO MOSFET, we employ a local FET model shown in Fig. 6(a), where local FET1 and FET2 are defined. The FET1 corresponding to the fully-recessed gate region has a local threshold voltage V_{TH1}, and the FET2 to the partially-recessed overlapped gate region has a local

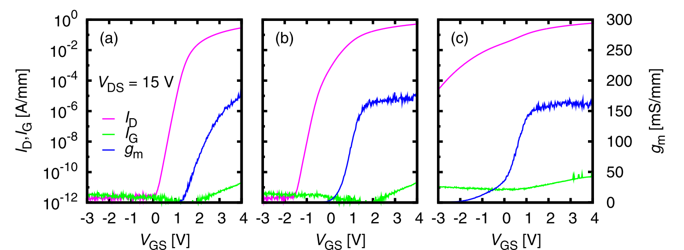

FIG. 4. Logarithmic-scale gate characteristics (I_D-V_{GS}) for (a) DRO, (b) SRO, and (c) Ref. The drain-source voltage is V_{DS} = 15 V, and the voltage sweep is $V_{GS} = +4 \rightarrow -3$ V. I_G: gate current, g_m: transconductance.

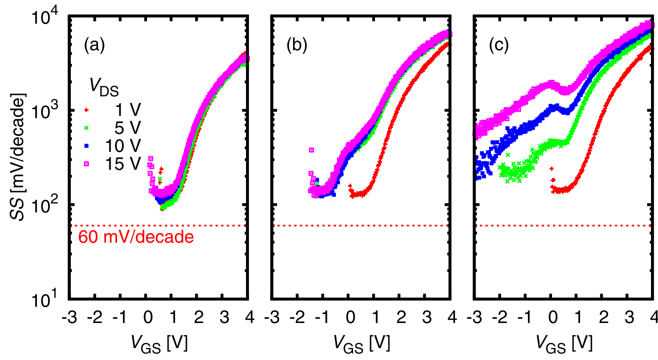

FIG. 5. Sub-threshold slope characteristics (SS-V_{GS}) at $V_{DS} = 1$, 5, 10, and 15 V, for (a) DRO, (b) SRO, and (c) Ref.

V_{TH2}. Since $V_{TH1} > V_{TH2}$, the total threshold voltage V_{TH} of the DRO MOSFET is dominated by the local FET1, $V_{TH} \sim V_{TH1}$. We define the local potential V_X at the connection point between the FET1 and FET2, where the effective drain-source voltage of the FET1 is V_X and that of the FET2 is $V_{DS} - V_X$. It should be noted that the effective gate-source voltage of the FET2 is $V_{GS} - V_X$. Let us consider the near-threshold regime $V_{GS} \sim V_{TH} \sim V_{TH1}$, where the FET1 is in the near-threshold regime. For a high V_{DS}, due to current continuity, the FET2 also must be in the near-threshold regime $V_{GS} - V_X \sim V_{TH1} - V_X \sim V_{TH2}$; thus V_X is clamped at $\sim V_{TH1} - V_{TH2}$. On the other hand, for a low $V_{DS} < V_{TH1} - V_{TH2}$, since the FET2 cannot be in the near-threshold regime, the effective drain-source voltage of the FET2, $V_{DS} - V_X$, should almost vanish due to current continuity; thus, $V_X \sim V_{DS}$. In the same way, we can also consider the local FET1 and FET2 for the SRO MOSFET, where the FET2 corresponds to the non-recessed overlapped gate region. As a result, for the DRO and SRO MOSFETs, V_X and $V_{DS} - V_X$ depend on V_{DS} as shown in Fig. 6(b). For V_{DS} higher than the threshold voltage difference $V_{TH1} - V_{TH2}$, V_X clamped at $\sim V_{TH1} - V_{TH2}$ makes the FET1 immune to DIBL, leading to the DIBL suppression for DRO and SRO. For DRO, DIBL can be more effectively suppressed, owing to the small $V_{TH1} - V_{TH2}$ caused by the partial recess in the overlapped gate region. The above mechanism is confirmed by device simulations. Figure 6(c) shows examples of simulated potential distributions along the channel of the DRO and SRO MOSFETs at $V_{DS} = 10$ and 15 V, in which we find that the effective drain-source voltage of the FET1 is clamped. Moreover, by the device simulations, it is confirmed that the potential distribution is not significantly affected by details of the sub-threshold characteristics of the local FETs.

From Fig. 3, the threshold voltage V_{TH1} without DIBL is ~ 2 V, which is much smaller than the calculated ~ 10 V by assuming only GaN polarization charges. This difference in V_{TH1} is attributed to insulator/semiconductor interface fixed charges. For GaN-based MIS devices, in general, interface fixed charges affect the threshold voltage.[24–30] In many cases, positive insulator/semiconductor interface fixed charges tend to be generated and to cancel negative polarization charges. The obtained $V_{TH1} \sim 2$ V suggests that positive Al_2O_3/GaN interface fixed charges with a density of $\sim 2 \times 10^{13}$ cm^{-2} are generated almost canceling the negative polarization charges of the Ga-face GaN. From the value of V_{DS} at which DIBL suppression occurs, we obtain the threshold voltage differences $V_{TH1} - V_{TH2} \sim 1$ V and ~ 7 V for DRO and SRO, respectively. Therefore, we obtain $V_{TH2} \sim 1$ V for DRO. For SRO, considering $V_{TH1} \sim 1$ V owing to DIBL, we obtain $V_{TH2} \sim -6$ V. These values of V_{TH2} for DRO and SRO are consistent with separate experiments for partially-recessed and non-recessed AlGaN-GaN MOSFETs.

DRO is also beneficial for current collapse suppression. Figures 7(a)–7(c) show pulsed I_D-V_{DS} characteristics for DRO, SRO, and Ref., respectively. The solid (red) and the dashed (blue) curves are obtained by pulsed measurements from the zero-bias condition ($V_{DS} = 0$ V, $V_{GS} = 0$ V) and from a bias condition ($V_{DS} = +25$ V, $V_{GS} = -10$ V), respectively. The used pulse-width is 5 μs and pulse-cycle is 1 ms.

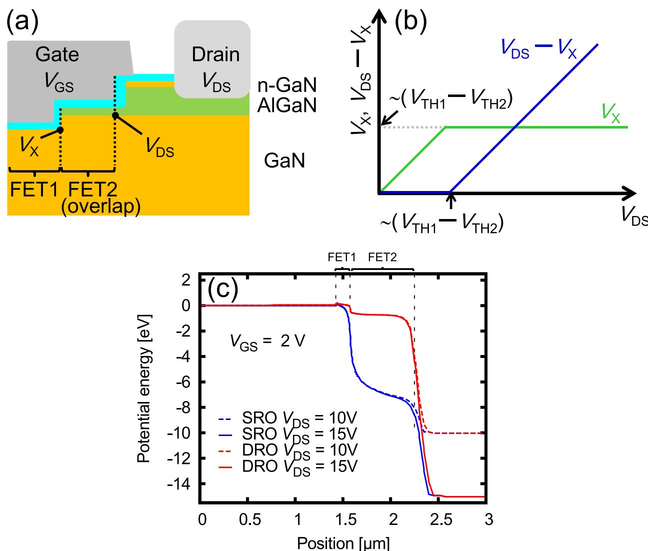

FIG. 6. (a) A local FET model of the DRO MOSFET with local FET1 and FET2. (b) The local potential V_X and $V_{DS} - V_X$ in the near-threshold regime, as functions of V_{DS}. (c) Simulated potential distributions along the channel of the DRO and SRO MOSFETs at $V_{DS} = 10$ and 15 V.

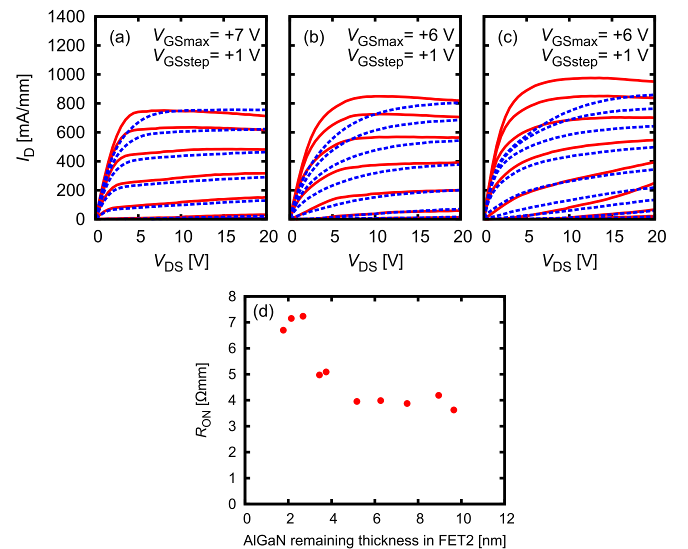

FIG. 7. Pulsed drain characteristics (I_D-V_{DS}) for (a) DRO, (b) SRO, and (c) Ref. The solid (red) and the dashed (blue) curves are obtained by pulsed measurements from the zero-bias condition ($V_{DS} = 0$ V, $V_{GS} = 0$ V) and from a bias condition ($V_{DS} = +25$ V, $V_{GS} = -10$ V), respectively. (d) R_{ON} as a function of the AlGaN remaining thickness in the FET2.

From the degree of dispersion between the zero-biased and biased characteristics, we find that Ref. and SRO exhibit serious current collapse, even though SRO seems to be slightly effective for current collapse suppression. On the other hand, we find that the current collapse is strongly suppressed for DRO. This shows that DRO is effective to suppress not only DIBL, but also current collapse. The suppressed current collapse for DRO is attributed to small effective drain-source voltages of the local FET1. As in the case of the near-threshold regime described earlier, the effective drain-source voltage of the local FET1 is limited, and the electric field at the gate-drain edge is relieved. This reduces the electron density trapped at the insulator/semiconductor interface, leading to the current collapse suppression. From Figs. 7(a)–7(c), we obtain on-resistances $R_{ON} \sim 4$, ~ 4, and $\sim 3\ \Omega$ mm for DRO, SRO, and Ref., respectively. The DRO MOSFET exhibits a rather low on-resistance $\sim 4\ \Omega$ mm and a moderate threshold voltage ~ 2 V, compared with reported fully-recessed AlGaN-GaN MOSFETs.[10–13,23] For the DRO MOSFETs, there is a trade-off between a low R_{ON} and DIBL/current collapse suppression. A deep recess etching in the FET2, which is beneficial for DIBL/current collapse suppression, may lead to a high R_{ON}, when the resistance of the FET2 is increased by the etching. In fact, Fig. 7(d) shows R_{ON} as a function of the AlGaN remaining thickness in the FET2 obtained by separate experiments, where R_{ON} rapidly increases for the thicknesses $\lesssim 4$ nm, while the employed thickness ~ 5 nm in this work can avoid such increase in R_{ON}. On the other hand, if we employ a larger AlGaN remaining thickness, the DIBL/current collapse suppression will become weak. However, our separate experiments show that the DIBL suppression is not significantly deteriorated for the thickness $\lesssim 9$ nm, suggesting that precise control of the etching depth is not so required for the DRO MOSFETs. It should be noted that a large voltage is applied to the FET2 in the DRO MOSFET under a high V_{DS}. Therefore, for very high voltage applications, it is necessary to employ technologies to enhance the operation voltage of the FET2, such as field-plate for the FET2.

In summary, we investigated DIBL in normally-off AlGaN-GaN MOSFETs with DRO, compared with SRO. It is found that DRO can more strongly suppress DIBL than SRO. We elucidate the mechanism of the DIBL suppression; DRO is effective for the DIBL suppression owing to the small threshold voltage difference between the local FETs, caused by the partial recess in the overlapped gate region. In addition, we found that DRO is also beneficial for current collapse suppression.

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