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Multi-level Non-Volatile Organic Transistor-based Memory using Lithium-ion-encapsulated Fullerene as a Charge Trapping Layer

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ABSTRACT

We report on multi-level non-volatile organic transistor-based memory using pentacene semiconductor and a lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) as a charge trapping layer. Memory organic field-effect transistors (OFETs) with a $Si^{++}/SiO_2/Li^+@C_{60}$/Cytop/Pentacene/Cu structure exhibited a performance of p-type transistor with a threshold voltage (V_{th}) of -5.98 V and a mobility (μ) of 0.84 $cm^2\ V^{-1}\ s^{-1}$. The multi-level memory OFETs exhibited memory windows (ΔV_{th}) of approximate 10 V, 16 V, and 32 V, with a programming gate voltage of 150 V for 0.5 s, 5 s, and 50 s, and an erasing gate voltage of -150 V for 0.17 s, 1.7 s, and 17 s, respectively. Four logic states were clearly distinguishable in our multi-level memory, and its data could be programmed or erased many times. The multi-level memory effect in our OFETs is ascribed to the electron-trapping ability of the $Li^+@C_{60}$ layer.

INTRODUCTION

Organic materials have attracted much research interest in electronics, owing to their unique and attractive features such as mechanical flexibility, low-cost, and suitability for large-area fabrication.[1–17] Among the different types of organic electronic devices including organic solar cells,[1–3] organic light-emitting diodes,[4–6,10] organic sensors,[7–10] and electronic circuit applications,[11,12] organic memories have received considerable attention because of their potential applications for flexible data/code storage, in both static and dynamic memories.[13] In addition to devices using resistor[13] and capacitor structures,[14] organic field-effect transistor (OFETs)-based memory devices have been intensively investigated in recent years, because of their simple structure using a single transistor, reduced data storage losses, and easy integration in electronic circuits.[15–17] The memory effect in transistor devices corresponds to a polarization of the gate dielectric caused by the application of an external voltage, which induces charges in the channel of transistor, and consequently increases the drain current (I_D). The magnitude of the remnant polarization after removal of the external voltage determines the magnitude of the programmed I_D, which in turn distinguishes a programmed state from the initial state. Based on this concept, ferroelectric materials such as poly(m-xylylene adipamide) [18] and poly(vinyledene fluoride/trifluoroethylene) [19,20] have been employed as gate dielectric layers, the remnant polarization of the ferroelectric polymer being responsible for the memory effect in the transistors. The memory effect in OFETs is also obtained using metal nanoparticles (NPs) as a floating gate.[21–23] Charges can be injected into the NPs by applying a programming voltage, and will remain stored after voltage removal. The stored charges affect the I_D of the OFETs and cause a shift of the threshold voltage (V_{th}), which corresponds to a change in logic state. The stability of each state after removal of the programming voltage is determinant for long-term operation of the memory OFETs. Another approach to obtain the memory effect in the OFETs is to use polymers as a charge trapping layer. This polymer layer

will then trap charges, affecting V_{th} in a manner similar to that of the floating gate of memory OFETs. The advantage of both the NPs floating gate and the charge-trap polymer memory OFETs lies in their simple fabrication process. In addition, the solution process ability and low temperature fabrication process are suitable for low cost and large-area fabrication.[24–26]

Expansion of the storage capacity of memory OFETs could be done by producing multi-level memory OFET, which exhibited several ON states.[21–26] In a multi-level memory OFET, the transfer curve can be shifted by applying different programming voltages to the gate. The different logic states of multi-level memory OFETs are thus defined by either the magnitude of I_D or the shift in V_{th}. In order to fabricate multi-level memory OFETs, ferroelectric polymers were used as a gate dielectric layer.[27–29] In 2015, Khan *et al* reported a good in performance ferroelectric multi-level memory with a dual gate structure.[29] The use of polymers as a charge-trapping layer also led to clear differences in logic states. For example, memory OFETs using polystyrene (PS) or poly(methyl methacrylate) (PMMA) as a charge trapping layer were reported by Guo *et al*. [30] These memory OFETs exhibited clear shifts in V_{th} with memory windows of 17 V, 36 V, and 53 V for programming voltages of -70 V, -100 V, and -120 V, respectively. However, these devices operated only under visible light irradiation, which could limit their range of applicability. Recently, Chiu *et al*. reported the use of star-shaped poly((4-diphenylamino)benzyl methacrylate) for charge-trapping, which enabled memory OFETs to exhibit a multi-level effect.[31] However, this memory exhibited a write-once-read-many behavior, in which the data could not be erased. These results led us to focus on the use of materials with charge-trapping abilities as a means to create multi-level memory OFETs with clearly distinguishable logic states, whose data could be programmed and erased many times.

Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) contains a Li cation inside a fullerene cage. This material could be a potentially interesting material for the charge trapping layer of multi-level memories, because of its multiple oxidation/reduction peaks observed in cyclic

voltammogram. [33]. In addition, its three-fold degenerated lowest unoccupied molecular orbital (LUMO) is expected to accept up to six electrons, and the number of electrons injected into the $Li^+@C_{60}$ can be controlled by an applied voltage.[32,33] Moreover, $Li^+@C_{60}$ has higher electron acceptability than pristine C_{60} [34,35] indicating a higher stability of the trapped electrons. Therefore, there is much potential in the use of $Li^+@C_{60}$ as an electron trapping material to fabricate multi-level memories.

In this article, we demonstrate multi-level memory OFETs using $Li^+@C_{60}$ as the charge trapping layer. Clear differences in four logic states (one erased state and three programed states) can be obtained using $Li^+@C_{60}$ as the charge trapping layer. The shifts in V_{th} (ΔV_{th}) from the erased state defining each of the programmed states were approximately 10 V, 16 V, and 32 V, obtained with a programing voltage of 150 V for 0.5 s, 5 s, and 50 s, respectively. These states accurately returned to the erased state by application of a voltage of -150 V for 0.17 s, 1.7 s, and 17 s, respectively. The repeatability of these shifts was confirmed by endurance cycle testing the device. In the latter part of this report, the unique operation mechanism of the memory OFETs was analyzed. The multi-level effect in our devices was attributed to the multiple oxidation/reduction peaks in cyclic voltammogram of $Li^+@C_{60}$ layer. In addition, since the electrons are trapped at $Li^+@C_{60}$ layer, instead of the silicon dioxide (SiO_2)/polymer interface [30,31], the SiO_2 dielectric layer could be replaced by a polymer layer. Thus, we believe that it is possible to fabricate a flexible multi-level memory OFETs in the future.

EXPERIMENTAL SECTION

Figure 1 shows a schematic illustration of the memory OFETs used in our study. These multi-level memory OFETs were fabricated using heavily doped silicon wafers (n^+Si, resistivity: 1–10 ○Ω·cm) coated with a 400-nm SiO_2 film. These wafers were cleaned ultrasonically in acetone for 10 min, pure water for 5 min, isopropyl alcohol for 10 min, and subsequently

subjected to UV-O_3 treatment for 30 min. The salt of $Li^+@C_{60}$ bis(trifluoromethylsulfonyl)imide ($Li^+@C_{60}$ NTf_2^-) was purchased from Idea International Co. Ltd. This layer was fabricated by spin-coating onto the SiO_2 at 1,000 rpm for 30 s, using a solution of $Li^+@C_{60}$ NTf_2^- salt in chlorobenzene at a concentration of 2.4 mg/ml, and dried at 140 °C for 30 min. Then, a 10-nm-thick CYTOP layer (Asahi Glass) was spin-coated at 2500 rpm for 60 s, using a 0.5 wt % CYTOP solution, and dried at 100 °C for 2 h. $Li^+@C_{60}$ cannot be dissolved by the solvent of CYTOP, and therefore the $Li^+@C_{60}$ layer was not damaged after CYTOP fabrication. (See Supporting Information, Fig.S1) The thickness of the CYTOP layer was measured by atomic force microscopy (AFM). A 50-nm-thick pentacene layer (Aldrich) was thermally deposited onto the CYTOP layer at a pressure of 1.6×10^{-6} Torr and a deposition rate of 0.3 Å/s. The copper (Cu) source/drain electrodes were deposited on the pentacene layer through a shadow mask, at a pressure of 2.5×10^{-5} Torr and a rate of 0.3 Å/s. The length (L) and width (W) of the channel were 50 μm and 2000 μm, respectively. The thickness of the Cu electrodes was 50 nm. For comparison, memory OFETs without the $Li^+@C_{60}$ layer were also fabricated.

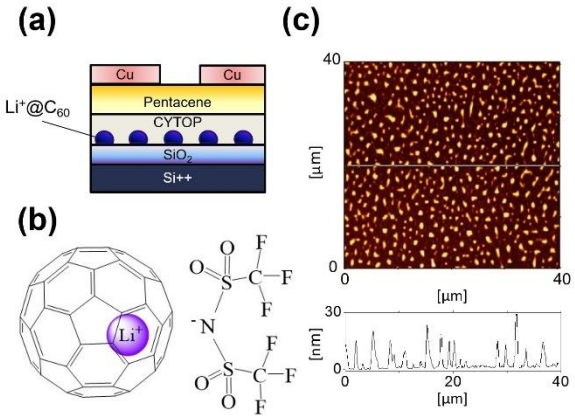

Fig. 1. (Color online) (a) Schematic illustration of the cross section of a memory OFET, (b) chemical structure of $Li^+@C_{60}$, and (c) AFM topographic image with a cross section profile of the $Li^+@C_{60}$ surface.

The capacitance per unit area of the gate dielectric (C_i) was measured in a sample with a device structure of Si^{++}/SiO_2 (400 nm)/$Li^+@C_{60}$/Cytop (10 nm)/Cu (50 nm) (0.014 cm^2 area) using an Agilent 4284A LCR meter.

The electrical characteristics of the memory devices were measured with a semiconductor characterization system (Keithley) in a dry nitrogen atmosphere, at room temperature.

RESULTS AND DISCUSSION

The output characteristics of the memory OFET are shown in Fig. 2(a). The I_D of transistor was measured while the source-drain voltage (V_D) was varied from 0 to -60 V in -10 V steps, for different gate voltages (V_G). As shown in this figure, the I_D of transistor increased linearly at low drain voltages (V_D), and saturated at high V_D, because the conducting channel in the pentacene layer was pinched off. This curve therefore shows that the OFET behaved as a typical p-channel OFET.

Figure 2(b) shows the transfer characteristics of the memory OFET and the gate current (I_G) measured during evaluation. The transfer characteristics were measured by sweeping V_G from 40 V to -80 V. The field-effect hole mobility (μ) of the devices can be calculated from the saturation regime, using the conventional metal-oxide semiconductor equation: [36]

$$I_{D,sat} = \frac{WC_i}{2L}\mu(V_G - V_{th})^2,$$

where $I_{D,sat}$ is the saturated drain current, W and L are the width and length of the channel, respectively, and C_i is the capacitance per unit area of the gate dielectric. The value of C_i for the CYTOP/$Li^+@C_{60}/SiO_2$ dielectric was 7.8 nF cm^{-2} at 1 kHz. The V_{th} of the memory OFETs was calculated from the intercept of the linear plot of $(I_D)^{0.5}$ versus V_G. The V_{th}, μ, and the on/off ratio were -5.98 V, 0.84 cm^2 V^{-1} s^{-1}, and 2.18×10^5, respectively. In addition, a trivial hysteresis was observed in the characteristics of the OFETs. These results and the low value of I_G indicate that

the memory OFETs exhibit good operational characteristics as typical OFETs, when compared with reported pentacene OFETs.[22,25,37,38]

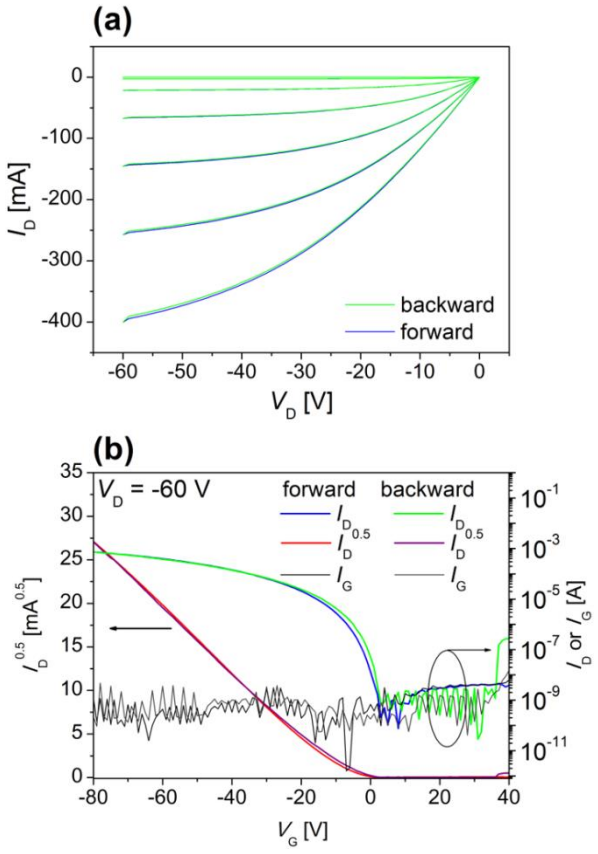

Fig. 2. (Color online) Characteristic curves of the memory OFETs at V_D = -60 V. (a) Output characteristics. (b) I_D–V_G, I_G–V_G, and $(I_D)^{0.5}$–V_G curves.

A multi-level memory OFET requires several ON states, which are distinguished by the shift of V_{th}. The shift of V_{th} should be controlled by applying different gate programming/erasing voltages. Another requirement is the repeatability of the voltage-current curve under the same applied voltage, both for programming and erasing. Repeatability ensures that the different logic states of multi-level memories can be replicated, even after several programming or erasing repetitions. Figures 3(a) and (b) show the programming and erasing characteristics of our memory OFETs. During programming or erasing, the source and drain electrodes were grounded. Before programming, the OFET was set into erased state by applying a negative voltage of -150 V to the gate for 5 s, which results in V_{th} of -19.79 V (black line). At programming voltages

below 100 V, the transfer curve did not shift much (See Supporting Information, Fig. S2). When a voltage of 150 V was applied to the gate for 0.5 s, the transfer curve shifted to the positive V_G region with a V_{th} of -9.99 V (red line), reflecting a memory window (ΔV_{th}) of approximately 10 V. Subsequently, a negative voltage of -150 V was applied to the gate for 0.17 s, to erase memory. The transfer curve shifted back to the erased state. The memory OFETs were then programmed with a voltage of 150 V for 5 s or 50 s, followed by erasing with a voltage of -150 V for 1.7 s or 17 s, respectively. The transfer curve shifted to positions with a V_{th} of -3.40 V (green line) and 12.40 V (blue line), and then returned to the erased state. The estimated values of ΔV_{th} were 16 V and 32 V. Figure 3(c) shows the values of V_{th} obtained by applying different programming times. This clearly indicates that our memories exhibited multi-level characteristics, with four distinguishable logic states. More other logic states could be observed by changing programming conditions (See Supporting Information, Fig. S3). Figure 3(d) shows the endurance cycles of our memory OFETs under repeated programmed and erased states at a read voltage (V_{read}) of -60 V. The repeatability of the magnitude of I_D for each state indicates that each logic state could be reliably replicated after erasing. However, at each state, a deviation of the I_D was observed, which would be caused by a hysteresis in transfer curve after programming. According to these results, we conclude that the memory OFETs using $Li^+@C_{60}$ clearly exhibit the desired multi-level characteristics.

The different shifts of V_{th} were caused by the different numbers of trapped electrons, which were injected from the Cu electrodes through the pentacene when a positive programming voltage was applied to the gate. These electrons can be trapped at the pentacene/CYTOP interface, inside the CYTOP bulk, at the CYTOP/SiO_2 interface, or inside $Li^+@C_{60}$ islands. Kalb *et al.* reported a transistor with an ITO/CYTOP/pentacene/Au structure, where the transfer curve did not shift even after applying a bias gate voltage of ±70 V for 2 h.[24] This indicates that the large shift in ΔV_{th} observed in our devices is not due to charge trapping neither at the

pentacene/CYTOP layer nor inside the CYTOP bulk. On the other hand, electrons can be trapped at the interface between CYTOP and SiO_2, and thus originate the memory effect.[26] In addition, the $Li^+@C_{60}$ layer should be (at least partially) responsible for the memory effect, because of its electron-trapping ability.

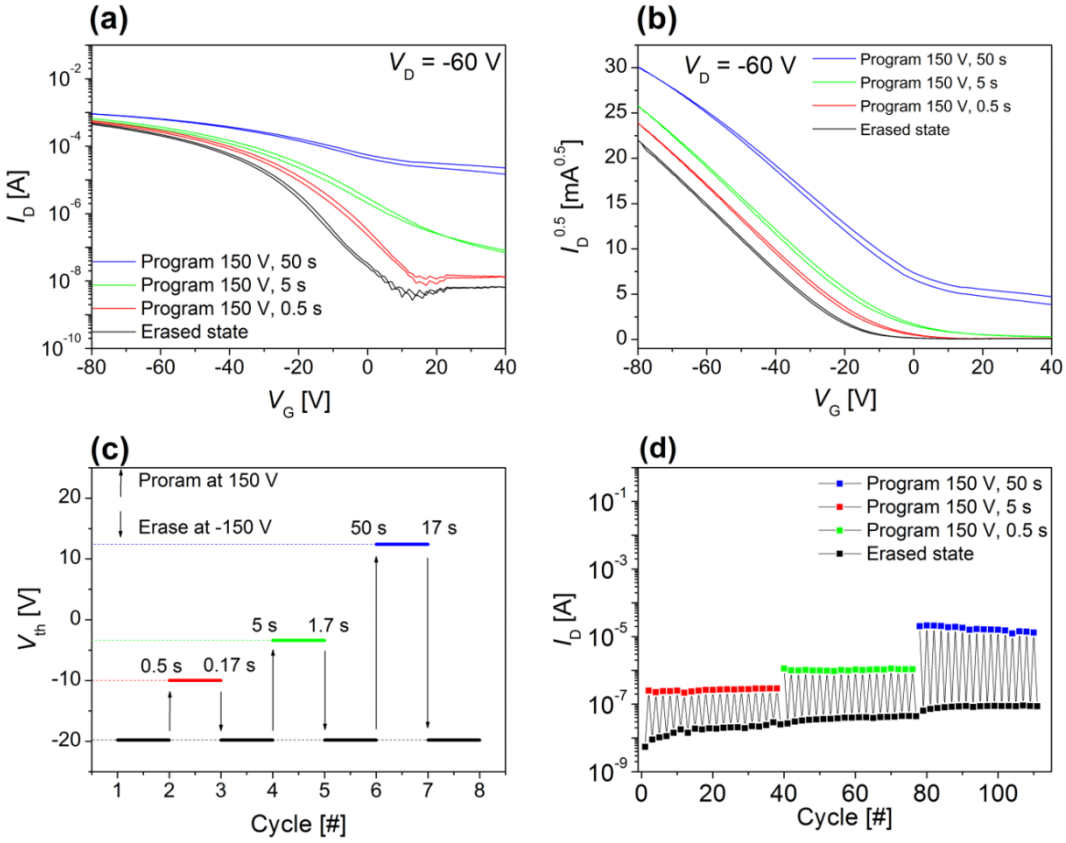

Fig. 3. (Color online) (a) I_D–V_G and (b) $(I_D)^{0.5}$–V_G curves of memory OFETs under different programming and erasing conditions. For programming/erasing, a gate pulse voltage of 150 V/-150 V is applied, with the source-drain electrodes connected to the ground. (c) Different V_{th} obtained by applying different gate voltage durations. (d) Endurance cycles, with repeated programmed and erased states.

To clarify the origin of the multi-level memory effect of the memory OFETs with $Li^+@C_{60}$, we fabricated OFETs using regular fullerene as charge trapping layer and OFETs without $Li^+@C_{60}$, and their memory characteristics were used for comparison. The memory OFET with regular fullerene charge trapping layer was not suitable for a memory application due

to its lower electron-acceptability than that of $Li^+@C_{60}$. (See the Supporting Information, Fig. S4) In the term of the OFET without $Li^+@C_{60}$, this OFET exhibited a performance with a μ of 0.32 $cm^2V^{-1}s^{-1}$, a V_{th} of -11.57 V and an on/off ratio of 7.41×10^5. Under a programming voltage of 150 V, the memory OFETs without $Li^+@C_{60}$ did not show any shift of the transfer curve, implying that electrons were not being trapped at the CYTOP/SiO_2 interface in the multi-level memory OFETs. The programming voltages were then increased up to 200 V. Figure 4 shows the obtained $(I_D)^{0.5}$–V_G curves of the memory OFETs without $Li^+@C_{60}$ at V_D = -60 V. With a programming voltage of 200 V applied for less than 250 s, the transfer curves were not considerably shifted, because not many electrons were being trapped by the charge trapping CYTOP layer. After programming for more than 350 s, the number of trapped electrons seemed to increase and then saturate, causing a large shift of V_{th}. Memory OFETs without $Li^+@C_{60}$ do not therefore show a clear difference in logic states and do not exhibit several ON states required for multi-level memories. However, the memory OFETs without $Li^+@C_{60}$ exhibit a one-bit memory characteristic, which is in line with the results reported by Dao in 2012.[26] We therefore conclude that the electron-trapping ability of the $Li^+@C_{60}$ layer is at the origin of the multi-level effect in our memory OFETs.

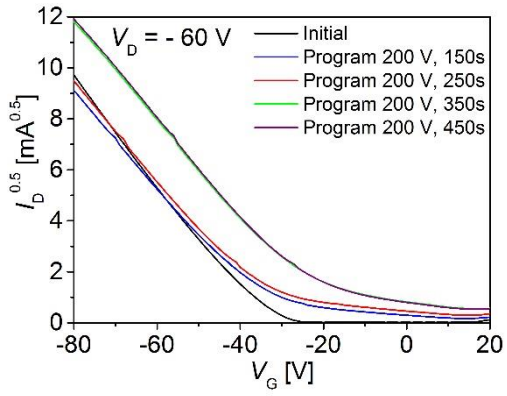

Fig. 4. (Color online) $(I_D)^{0.5}$–V_G curves of the memory OFETs without $Li^+@C_{60}$.

In our multi-level memory OFETs, the density of trapped electrons in $Li^+@C_{60}$ layer (ΔN) was calculated using the equation $\Delta N = \varepsilon \cdot \Delta V_{th}/(d \cdot e)$ [39] where ε, d are the permittivity (1.86×10^{-13} F·cm^{-1}) and thickness of the Cytop layer (10 nm), e is the elementary charge, and ΔV_{th} is the V_{th} shift. As shown in Table 1, the trapped electrons in the $Li^+@C_{60}$ layer increased with the pulse duration. Based on an assumption that all $Li^+@C_{60}$ molecule could trap the same number of electrons, the average number of trapped electrons was estimated by dividing the density of trapped electron ΔN by the density of $Li^+@C_{60}$ molecules in the trapping layer. The density of $Li^+@C_{60}$ molecule per area in the charge trapping layer was estimated to be 9.00×10^{14} cm^{-2} from the average height of $Li^+@C_{60}$ domains (8.0 nm) on SiO_2 substrate, and the density of $Li^+@C_{60}$ bulk, which is roughly estimated to be 1.88 g·cm^{-3} [32]. Thus, the average numbers of trapped electrons per $Li^+@C_{60}$ molecule were estimated to be 2.40×10^{-2}, 3.84×10^{-2}, and 7.67×10^{-2} under a programming voltage of 150V for 0.5, 5 and 50 seconds, respectively. This small values of average numbers of trapped electrons would be due to the assumption based on that all $Li^+@C_{60}$ molecules in the $Li^+@C_{60}$ domains equally contribute to trap the electrons. At the surface of $Li^+@C_{60}$ domain, however, each $Li^+@C_{60}$ molecule could trap one, two, three or more electrons, since the multi peaks observed in the cyclic voltammogram of $Li^+@C_{60}$ [33] show the small differences in the potential voltages of 0.14, -0.61 and -0.81 V. According to these results, a proposed operation mechanism for the memory OFET is that electrons are injected from the source/drain electrodes into the $Li^+@C_{60}$ layer by applying a positive voltage to the gate, and remain trapped there. When no electron is trapped on the $Li^+@C_{60}$ molecule, the LUMO has a three-fold degeneracy. (Fig. 5 (a)) Then, one, two and three electrons will occupy at the LUMO level of -4.54, (Fig. 5 (b)) -3.79 (Fig. 5 (c)) and -3.59 eV, (Fig. 5 (d)) depending on the programming time. In the case of more than three electrons were trapped in one $Li^+@C_{60}$ molecule, the fourth electron may be trapped at the LUMO level with the lowest potential energy. The $Li^+@C_{60}$ layer with trapped electrons enhances the intrinsic carriers in the memory OFET

channel, thus causing a shift of V_{th} to a positive value. This shift caused by the trapped electrons is consistent with the shift in memory OFETs using a charge trapping layer.[25,26] We suggest that the multi-level memory effect corresponds to a different number of trapped electrons at the $Li^+@C_{60}$ layer under different programming conditions correspond an operation mechanism already proposed for the multi-level effect in other OFETs.[26] This would result from the high electron acceptability of the three-fold degenerated LUMO of $Li^+@C_{60}$, and the high stability of the trapped electrons in the $Li^+@C_{60}$ cage, which is attributed to the reduction of $Li^+@C_{60}$.[33,34] On the other hand, the trapped electrons are de-trapped by applying a negative voltage to the gate, which causes V_{th} to move back to its erased state. The de-trap in our device can be explained as the removal of electrons from the $Li^+@C_{60}$ cage by an externally applied voltage, an effect already reported in the literature.[33]

Table 1. Numbers of trapped electrons at Li+@C60 layer under different programming voltages

Programming conditions	ΔV_{th} (V)	ΔN (cm^{-2})
150 V, 0.5 s	10	2.16×10^{13}
150 V, 5 s	16	3.46×10^{13}
150 V, 50 s	32	6.91×10^{13}

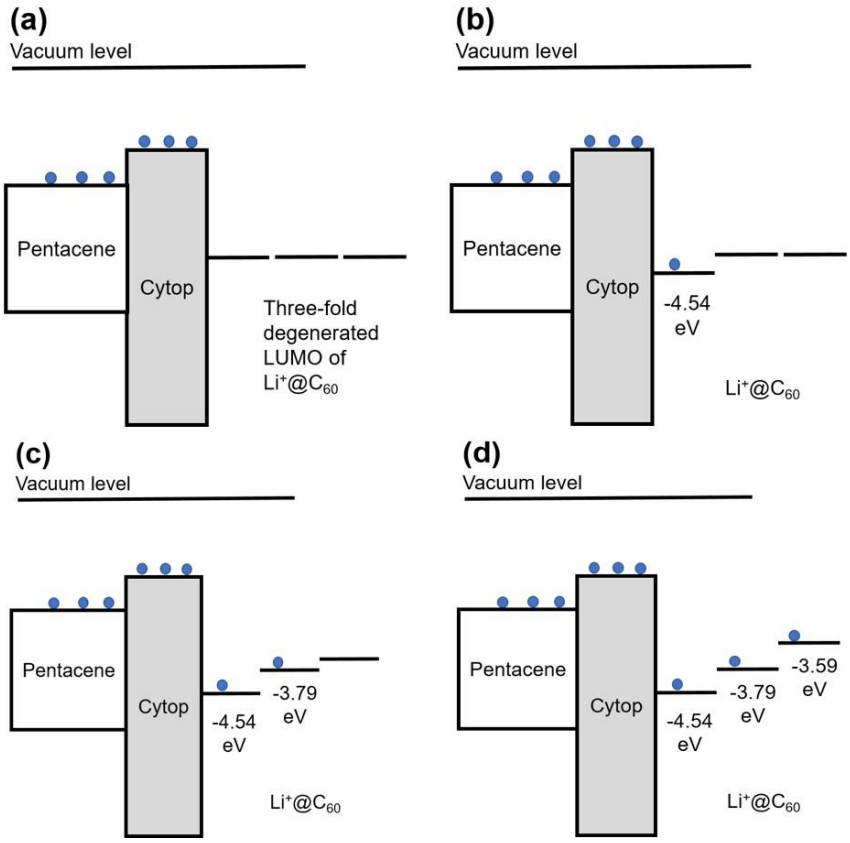

Fig. 5. (Color online) The occupation of electrons in a single $Li^+@C_{60}$ to the three-fold degeneration of LUMO states. (a) unoccupied, (b) one-electron trapping, (c) two-electron trapping, and (d) three-electron trapping. The symbol "•" stands for electron.

To evaluate the long-term operation of the memory OFETs, the retention times of both the programmed and erased states were measured (Fig. 6). After programming and erasing, the I_D of each state was measured for 50,000 seconds, at a V_D of -60 V and a V_G of 0 V. The different logic values were defined by the low I_D (erased state) and high I_D (programmed states) values. A clear difference in logic states was observed for more than 50,000 seconds, which is longer than reported results.[40] The I_D of the erased states increased some thousands of seconds later, which may be caused by a chemical interaction between a few $Li^+@C_{60}$ and the pentacene layer. Under the application of V_D = -60 V to the gate electrode during the long-time operation, a few $Li^+@C_{60}$ cations could migrate to the pentacene layer, according to the electric field. Consequently, the $Li^+@C_{60}$ may react with pentacene, causing the increase in I_D. In our

preliminary experiment, the increase of I_D was observed when the pentacene layer was directly deposited on the $Li^+@C_{60}$ layer (See Supporting Information, Fig. S5).

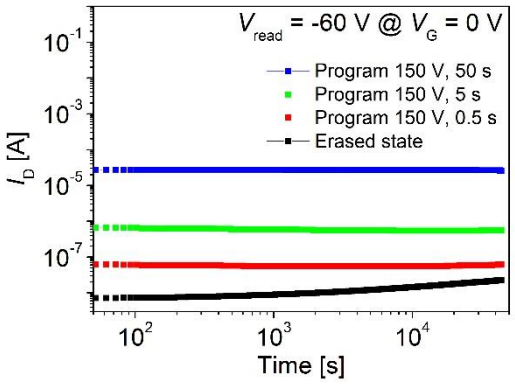

Fig. 6. (Color online) Retention characteristics of the transistor memories. Programming and erasing were performed by gate pulse voltages of 150 V for 0.5 s, 5 s, and 50 s, and -150 V for 0.17 s, 1.7 s, and 17 s, respectively, while V_D = 0 V. During the retention measurement, values of V_D = -60 V and V_G = 0 V were used.

CONCLUSIONS

We demonstrated multi-level non-volatile memory transistors using $Li^+@C_{60}$ as a charge trapping layer. The produced OFETs exhibited good performance, with a low V_{th} of -5.98 V and a high μ of 0.84 $cm^2 V^{-1} s^{-1}$. For three programmed states, a voltage of 150 V was applied to the gate for 0.5 s, 5 s, and 50 s, causing approximate shifts of the transfer curve of 10 V, 16 V, and 32 V, respectively. To return to the erased state, a negative voltage of -150 was used for 0.17 s, 1.7 s, and 17 s. A clear difference in the four logic states (one erased state and three programed states) was observed during more than 50,000 seconds. The multi-level effect was found to originate in the electron-trapping ability of the $Li^+@C_{60}$ layer, by comparison with OFETs without a $Li^+@C_{60}$ layer. The operation mechanism analysis showed that the multi-level effect would be attributed to the injection of electrons into the three-fold degenerated LUMO of $Li^+@C_{60}$ molecule, which can accept up to 6 electrons. Additional research work is being

conducted, focused on reduction of operation voltage, increasing the on/off ratio, improving the long-time operation of the devices, and applying for flexible memory devices. We believe that our frontier results will help the evolution of the $Li^+@C_{60}$ research field, and reveal its potential for electric applications.

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