Behavior of the potential-induced degradation of photovoltaic modules fabricated using flat mono-crystalline silicon cells with different surface orientations

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This paper deals with the dependence of the potential-induced degradation (PID) of flat, p-type mono-crystalline silicon solar cell modules on the surface orientation of solar cells. The investigated modules were fabricated from p-type mono-crystalline silicon cells with a (100) or (111) surface orientation using a module laminator. PID tests were performed by applying a voltage of −1000 V to shorted module interconnector ribbons with respect to an Al plate placed on the cover glass of the modules at 85 °C. A decrease in the parallel resistance of the (100)-oriented cell modules is more significant than that of the (111)-oriented cell modules. Hence, the performance of the (100)-oriented-cell modules drastically deteriorates, compared with that of the (111)-oriented-cell modules. This implies that (111)-oriented cells offer a higher PID resistance.

1. Introduction

The potential-induced degradation (PID) of Si-wafer-based photovoltaic (PV) modules has been identified as one of the most important reliability issues. Very large scale PV systems, which can generate a high electric power, have been installed worldwide over the last decade. PV modules in such systems can be exposed to high electrical potential differences from their grounded frames. These may trigger PID, which can cause significant performance losses in the modules.[1–3)]

The PID of p-type crystalline Si (c-Si) PV modules is characterized by a reduction in the shunt resistance R_p[1)] and the enhancement of depletion region recombination.[4,5)] The PID of p-type c-Si PV modules can be attributed to alkali metal ions, e.g., Na^+, migrating from a

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module cover glass owing to high voltages.[3] Naumann *et al.*[6] have revealed that Na accumulates in the silicon nitride (SiN_x)/Si interface of c-Si solar cells in PID-affected regions. It has also been reported that both PID shunts and Na accumulation occur locally.[7,8] Moreover, they have found that stacking faults existing in c-Si contaminated by Na play an important role in PID.[9] Some research groups have proposed physical models that can explain the shunting based on Na-decorated intrinsic stacking faults.[9–11] Recently, Ziebarth *et al.*[12] have provided further detailed discussion about the diffusion of Na in intrinsic stacking faults and the short-circuiting of p–n junctions by theoretical calculations based on the density functional theory. Very recently, Wilson *et al.*[13] have investigated in detail the drift characteristics of Na ions in SiN_x films where an electric field exists.

The PID of c-Si PV modules is influenced by module components, such as a cover glass, encapsulant, and cells. It has been demonstrated that no significant PID occurs in c-Si PV modules with a quartz cover glass,[4] aluminosilicate chemically strengthened glass,[14] or an acrylic thin film[15] instead of conventional tempered glass. PID can be prevented by the use of a high-electric-resistance encapsulant,[4,16] by inserting a polyethylene[17] or an ionomer[18] thin film between an ethylene-vinyl acetate copolymer (EVA) encapsulant and a front cover glass or cells, or by increasing the cross-linkage level or the thickness of the encapsulant.[19] PID resistance is also affected by the refractive index[2,20,21] or thickness[2] of an SiN_x antireflective coating (ARC) layer on the emitter layer of a c-Si PV cell. PID can therefore be also suppressed by the composition control of the ARC layers. However, it is not very desirable to change the refractive index from conventional and optimized values because of the enhancement of parasitic absorption. Mishina *et al.*[22,23] have shown that a high PID resistance can be realized by using PV cells with ARC layers having a conventional refractive index prepared by plasma-enhanced chemical vapor deposition (PECVD) using a hollow cathode. Hara *et al.*[24] have reported that TiO_2 thin films deposited on the inner surfaces of a cover glass can prevent PID for c-Si modules. Du *et al.*[25] have shown that the PID of c-Si solar cells can be effectively reduced without influencing their efficiency by inserting phosphorus silicate glass (PSG) layers between the front n^+ emitters and the SiN_x ARC layers. PID-affected modules can recover from the degradation by applying a positive bias.[2,3] The recovery is explained by a diffusion-driven process.[9,10,26]

Recently, Chen *et al.*[27] have reported that the shape of the textured surface of c-Si can influence its PID resistance. They have demonstrated that cells having groove-rounded texture exhibit a higher PID resistance.[27] Detailed discussion has, however, not been made thus far. Groove-rounded cells generally have partially residual (100)-oriented surfaces as well

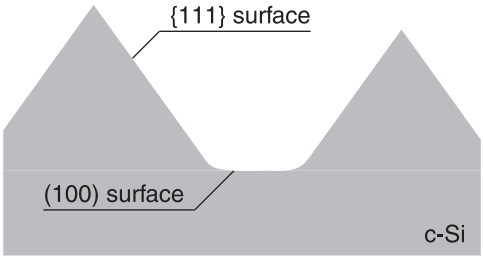

Fig. 1. Schematic diagram of a rounded groove between micrometer-sized pyramids. The rounded groove is characterized by a residual (100) surface.

as {111}-oriented ones belonging to micrometer-sized pyramids, as illustrated in Fig. 1. The higher PID resistance of groove-rounded textured cells may be affected by the surface orientation of c-Si cells.

In the present work, we investigate the effect of the surface orientation of c-Si cells on PID resistance, by comparing the results of PID tests on modules fabricated using p-type flat (100)- and (111)-oriented cells. On the basis of the obtained results, we also discuss the higher PID resistance of groove-rounded textured cells demonstrated by Chen *et al*. Our findings may provide an improved explanation of the effect of the surface morphology of cells on PID resistance.

2. Experimental procedure

(100)- or (111)-oriented, one-side polished p-type c-Si wafers were cut to 20×20 mm^2-sized substrates. The front surface of the substrates was coated with a liquid PSG source (Tokyo Ohka Kogyo, SC-913) by spin coating, and the substrates were subsequently annealed at 850 °C for 25 min in N_2 atmosphere in order to form n^+ emitters. The emitters on the flat c-Si surfaces had a sheet resistance of ~30 Ω/sq. After the removal of the phosphorus silicate glass remaining on the c-Si surfaces, SiN_x ARC films with a thickness of ~70 nm were deposited onto the n^+ emitter surfaces by catalytic CVD (Cat-CVD),[28] which is also referred to as hot-wire CVD. The thickness and refractive indices of the SiN_x ARC films on the (100) and (111) substrates were almost the same, and we considered that the films deposited on both substrates had the same properties. Ag paste was printed onto the front surfaces of the c-Si substrates by screen printing, followed by the screen printing of Al and Ag pastes on their rear sides. The samples were then fired at a peak temperature of 800 °C in air atmosphere in a tube furnace to form electrical contact. After the metalization, edge isolation was carried out by shaving the edges of the cells with sandpaper.[29]

Interconnector ribbons were soldered onto the cell's front and rear Ag contacts. We pre-

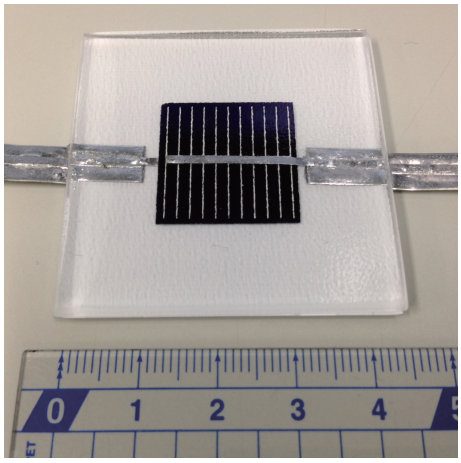

Fig. 2. (Color online) Appearance of a fabricated module. The cell has a size of 20×20 mm^2, and the module has a size of 45×45 mm^2.

pared stacks composed of cover glass/EVA encapsulant/c-Si cell/EVA encapsulant/typical backsheet [poly(vinyl fluoride) (PVF)/poly(ethylene terephthalate) (PET)/PVF]. The cover glass has a size of 45×45 mm^2 and contains alkali metals such as Na. The modules were fabricated from the stacks in a module laminator. Our lamination process consisted of two steps: a degassing step for 5 min and an adhesion step for 15 min. The stacks were placed with the cover glass side down on a stage heated at 135 °C during lamination. The flat-cell modules generally show an energy conversion efficiency of approximately 13%. The appearance of a typical module is shown in Fig. 2.

The PID tests were performed by applying a voltage of −1000 V to shorted module interconnector ribbons with respect to an Al plate placed on the cover glass of the modules in a chamber maintained at 85 °C using a power supply (Kikusui Electronics, TOS7200). We carried out a PID test on three identical modules under different preparation conditions. This test method and similar ones have been widely used and established as the ways that can easily produce PID-affected modules in a short time by many researchers.[5,8,14–17,19,21–24,30–32] We use the term "PID stress" here to refer to such voltage and temperature stress. In this experiment, humidity in the heating chamber was not controlled during stressing; however, the relative humidity in a similar setup[30] is small (~2%RH). We therefore neglected its effect on the performance degradation of the modules, such as moisture ingress into the modules and the corrosion of metal parts. Note that, at the present stage, it is not known how long the PID test stress corresponds to the duration that generates PID in outdoor large-scale PV systems. We used this PID test just for intercomparison between the test samples.

In order to evaluate the degradation, current density–voltage (J–V) measurements were

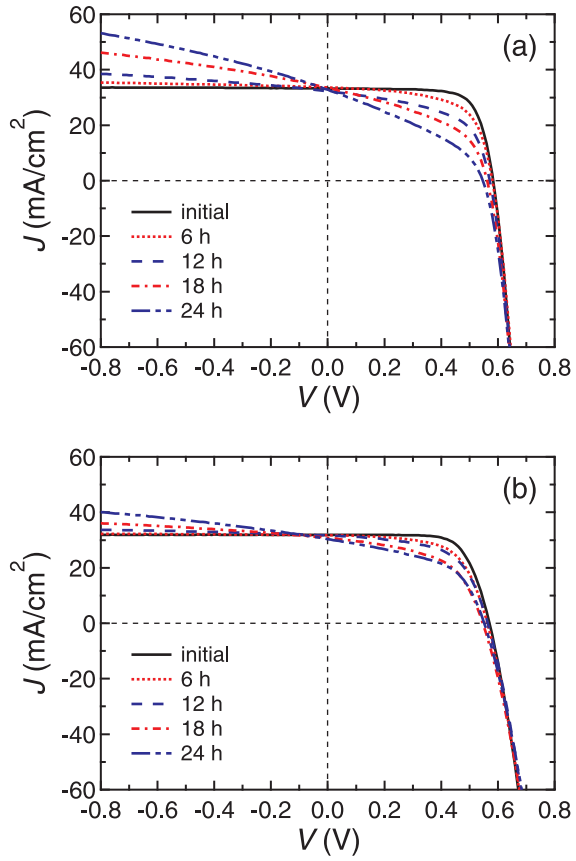

Fig. 3. (Color online) Representative 1-sun-illuminated J–V curves of the modules with (a) (100)- and (b) (111)-oriented p-type c-Si cells before and after the PID tests.

conducted under dark and 1-sun-illuminated conditions for the modules before and after the PID tests. The saturation current density J_0, the parallel resistance R_p, and the ideality factor n were determined by fitting the dark J–V data to the following single-diode equation:

$$J(V) = J_0 \left\{ \exp\left[\frac{q(V - JR_s)}{nkT} \right] - 1 \right\} + \frac{V - JR_s}{R_p}, \quad (1)$$

where q is the elementary charge, R_s the series resistance, k the Boltzmann constant, and T the absolute temperature. Here, we did not restrict n to ≤ 2, since $n > 2$ has often been observed in PID-affected p-type c-Si PV modules.[5,11] J_0, R_p, and R_s were restricted only to >0. Single-diode fitting was performed with the statistical software Igor Pro 6 (WaveMetrics, Inc.).

3. Results and discussion

Figure 3 shows the representative 1-sun-illuminated J–V curves for the modules with (100)- and (111)-oriented cells before and after the PID tests. The J–V characteristics shown in Fig. 3 were obtained from the modules with median $P_{max}/P_{max,0}$ values after the PID test per-

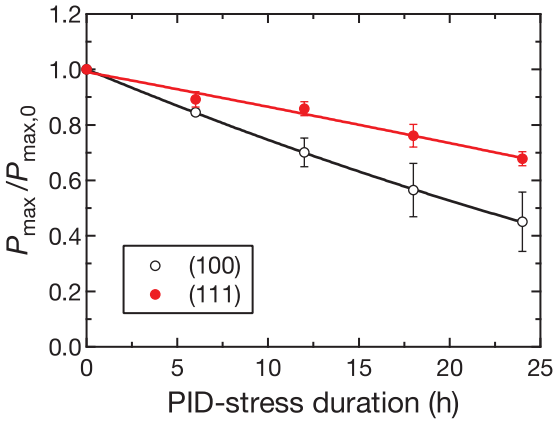

Fig. 4. (Color Online) Dependences of the normalized maximum powers $P_{max}/P_{max,0}$ of the modules with (100)- and (111)-oriented cells on PID stress duration. Each data point shows the mean for three modules, and each error bar corresponds to the standard error of the mean.

formed for 24 h, where P_{max} is the maximum power and $P_{max,0}$ is the initial maximum power. Both modules with (100)- and (111)-oriented cells show the typical degradation behavior of the J–V curves characterized by shunting with sublinear characteristics under reverse bias after the PID tests.

Figure 4 shows the dependences of the normalized maximum powers $P_{max}/P_{max,0}$ of the modules fabricated using the (100)- and (111)-oriented cells on PID stress duration. As can be seen in Fig. 4, the $P_{max}/P_{max,0}$ values of both (100) and (111) modules decrease with PID stress duration, demonstrating that PID occurs regardless of surface orientation. The decrease in the $P_{max}/P_{max,0}$ of the modules with the (100)-oriented cells is, however, more significant than that of the modules with the (111)-oriented cells. The $P_{max}/P_{max,0}$ values of the (100)- and (111)-oriented cell modules decreased to about 0.44 and 0.70 after the PID test, respectively. This implies that the PID behavior of p-type c-Si PV modules depends on the surface orientation of the cells, and cells with the (111) surface orientation have higher PID resistance than those with the (100) surface orientation.

Figure 5 shows the dependences of the J_0, n, and $1000/R_p$ of the modules with the (100) and (111) cells on PID stress duration. The J_0, n, and $1000/R_p$ of the (100) modules are increased by PID stress more significantly, compared with those of the (111) modules. In particular, inverse R_p has a clear dependence on the surface orientation of the cells. This indicates that the cells with a (111)-oriented surface tend to be less influenced by shunts caused by PID stress than those with the (100)-oriented surface. PID-affected modules show significantly high n values exceeding 2, as shown in Fig. 5. These high n values have been

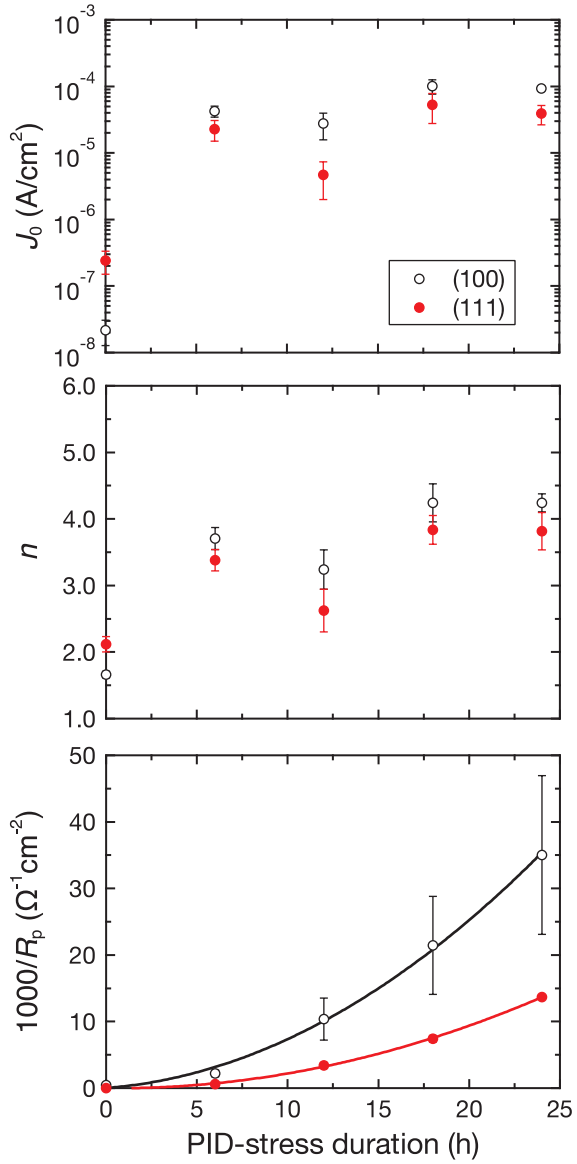

Fig. 5. (Color Online) Dependences of J_0, n, and $1000/R_p$ values of the modules with (100)- and (111)-oriented cells on PID stress duration. Each data point shows the mean for three modules, and each error bar corresponds to the standard error of the mean. Note that we do not restrict n values to ≤ 2. Note that the $1000/R_p$ values for (111)-oriented cell modules were almost the same and their error bars were negligible.

observed in the PID of c-Si PV modules[5,11] and originate from a significantly high defect density in the depletion region introduced by PID stress.[10] We can observe that $n > 2$ in the unaffected (111)-oriented cell modules. Note that regions damaged by laser cutting or diamond scratching produce n values higher than 2.[33] Our solar cells have edge regions damaged during edge isolation using sandpaper. From this, the high n values of the unaffected modules may be attributed to recombination in damaged edge regions.

It has been reported that PID shunts originate from Na-decorated intrinsic stacking faults

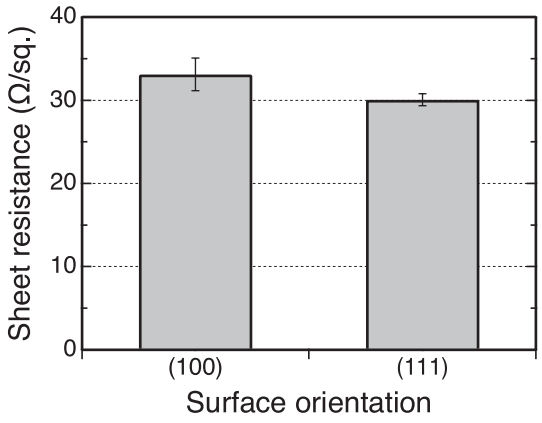

Fig. 6. Sheet resistances of n^+ emitters formed on c-Si substrates with different surface orientations. These n^+–p junctions were fabricated under the conditions same as those under which the solar cells were fabricated. Sheet resistance was measured by the four point-probe method at room temperature. Each data point shows the mean for three samples, and each error bar corresponds to the standard error of the mean.

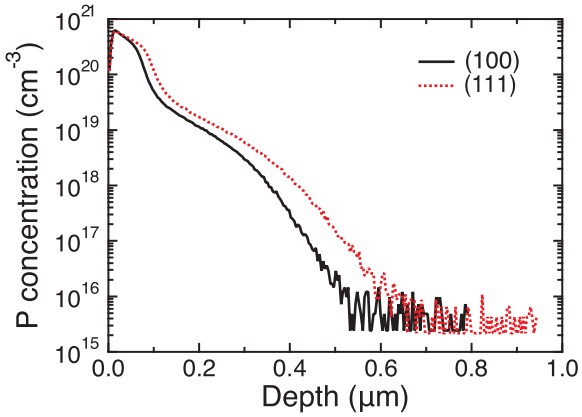

Fig. 7. (Color online) D-SIMS profiles of P atoms in the (100) and (111) substrates with a median of sheet resistance. The profiles were obtained using a Cs^+ primary ion beam with an acceleration voltage of 15 kV.

penetrating the n^+ emitter of solar cells.[10] These Na-decorated stacking faults behave as electrically conductive two-dimensional layers that can cause the short-circuiting of the p–n junction.[12] On the basis of these facts, PID behavior can be related to the number of such stacking faults penetrating the n^+ emitter of the solar cells. First, we should therefore consider the depth of the p–n junction formed by phosphorus diffusion, since an increased junction depth lowers the number of intrinsic stacking faults that can penetrate the n^+ emitter of cells. Actually, Berghold *et al.*[2] have reported that the PID of c-Si PV modules depends on the sheet resistance of n^+ emitters. As shown in Fig. 6, we were not able to observe a clear difference between the sheet resistances of the n^+ emitters on the (100) and (111) substrates; however, the sheet resistance of the (111)-oriented substrates was slightly lower than that of the (100)-

oriented substrates. Additionally, we observed the depth profiles of P atoms in the (100) and (111) substrates with the medians of sheet resistance, by dynamic secondary ion mass spectrometry (D-SIMS) using a CAMECA IMS-7f apparatus with a Cs^+ primary ion beam. The depth profiles of P atoms are shown in Fig. 7. The p–n junction depths are slightly different between the (100)- and (111)-oriented substrates, and that of the (111)-oriented substrate with the median sheet resistance is slightly deeper. This slightly deeper junction of the (111)-oriented substrates might cause a higher PID resistance. However, the findings of Berghold *et al.*[2] imply that the PID resistance does not strongly depend on the sheet resistance of n^+ emitters below 55 Ω/sq. Thus, we can probably neglect the effects of the differences in sheet resistance and junction depth on the PID resistance of the modules. Moreover, according to a previous study,[34] the diffusion coefficients of P in Si(100) and Si(111) are almost the same, and the difference in junction depth obtained may not be significant. We therefore have to discuss the effects of other factors on PID behavior.

We consider the number of intrinsic stacking faults in unaffected cells as the second candidate. One lattice point is included in four {111}-related planes. In (100) substrates, these four types of planes can penetrate the p–n junction. On the other hand, in (111) substrates, one of the four planes does not penetrate the p–n junction, since it is parallel to the p–n junction interface. Assuming that intrinsic stacking faults are generated with the same probability per {111}-related plane, fewer PID-related stacking faults exist in (111) cells than in (100) cells. This can be one reason for the higher PID resistance of the c-Si PV modules with the (111)-oriented cells. Much additional work is, however, required to elucidate this phenomenon.

In a previous study,[27] it has been shown that groove-rounded textured cells have a higher PID resistance. This cannot be explained by our experimental results, since the results show that the modules with (111)-oriented flat cells offer a higher PID resistance and, on the basis of the results, we predict that the PID resistance of groove-rounded textured cells will be rather low. Hence, we have to consider other factors for the higher PID resistance of groove-rounded textured cell modules.

We show three possible reasons for the change in the PID resistance of groove-rounded cells as follows: One may be thicker ARC layers covering their grooves. Figure 8 shows schematic diagrams of the ARC films on sharp and rounded grooves. Generally, ARC layers are formed by CVD through the decomposition of source gases and the reaction of the generated radicals. Given that the numbers of radicals supplied to the groove regions are equivalent, the effective thickness of the ARC layer on the rounded grooves becomes larger

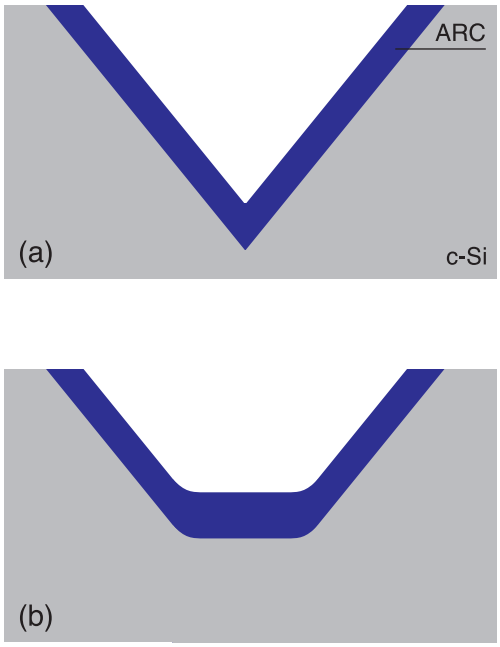

Fig. 8. (Color Online) Schematic diagrams of ARC films on (a) the sharp-shaped and (b) the rounded grooves.

than that on the sharp grooves, as illustrated in Fig. 8. The thicker the ARC layer, the weaker the electric field in the layer, and the longer the distance to the emitter surface from the ARC surface. The relatively thicker ARC layers on the rounded grooves might therefore provide higher PID resistance. The second reason may be a smaller surface area. The above results of the dependence on surface orientation were obtained for the substrates with the same surface area. However, the surface area of the groove-rounded cells is slightly smaller than that of the conventional textured cells. Hence, the number of PID-related stacking faults that terminate at the Si surface may decrease with decreasing surface area of the grooves. This might result in a slightly higher PID resistance of groove-rounded cells. The last reason may be the change in an electric field around the surface. Smoother and slightly shallower textured surfaces cause change in the electric field distribution around surfaces during PID stressing. This might affect the PID resistance of the cells; however, the effect of the electric field distribution on PID resistance has not yet been investigated in detail. At the present stage, we cannot quantitatively discuss these effects.

4. Conclusions

In this work, by the PID acceleration test, we have investigated the dependence of the surface orientations of flat c-Si cells on PID behavior. The results have demonstrated that the R_p of

the (100)-oriented cells is decreased more significantly by PID stress than that of the (111)-oriented cells. This suggests that (111)-oriented cells have a higher PID resistance. The higher PID resistance of (111)-oriented cells may be caused by fewer PID-related intrinsic stacking faults. Thus, the higher PID resistance of groove-rounded textured cells cannot be explained by the dependence on surface orientation. It might be attributed to the thicker ARC layer on the rounded grooves and/or the smaller surface area at the front of the cells.

Acknowledgments

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