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# Indium Tin Oxide Sputtering Damage to Catalytic Chemical Vapor Deposited Amorphous Silicon Passivation Films and Its Recovery

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## Abstract

We investigated the influence of indium tin oxide (ITO) sputtering damage to various types of amorphous silicon (a-Si) passivation films deposited by catalytic chemical vapor deposition. Intrinsic (i-) a-Si, n-type (n-) a-Si/i-a-Si, and p-type (p-) a-Si/i-a-Si stacked films were prepared on crystalline Si, and ITO was sputtered at various temperatures and RF powers, followed by post-annealing at 200 °C. Effective minority carrier lifetime ( $\tau_{\text{eff}}$ ) of almost all the samples decreases drastically after sputtering, while  $\tau_{\text{eff}}$  of the samples with ITO sputtered at room temperature recovers significantly by post-annealing. Annealing before sputtering and sputtering at lower RF power leads to more effective recovery of  $\tau_{\text{eff}}$ . The samples with ITO sputtered to an n-a-Si/i-a-Si stack show large  $\tau_{\text{eff}}$  recovery, while the samples with ITO sputtered to a p-a-Si/i-a-Si stack show much smaller  $\tau_{\text{eff}}$  recovery.  $\tau_{\text{eff}}$  recovery after ITO sputtering thus depends on the types of a-Si passivation films, which may be related to the modification of band alignment by the existence of ITO.

Keywords: Passivation, Sputtering, Cat-CVD, ITO, Silicon heterojunction solar cells

## 1. Introduction

Silicon heterojunction (SHJ) solar cells have attracted much attention because of their high conversion efficiency and several industrial benefits due to low-temperature process for cell fabrication [1–5]. A SHJ solar cell contains a crystalline silicon (c-Si) wafer and amorphous Si (a-Si) films, and the termination of dangling bonds by hydrogen atoms contained in the a-Si films results in good a-Si/c-Si interfacial quality. Thanks to the existence of a-Si passivation films, SHJ solar cells generally have high open-circuit voltage. a-Si films are conventionally formed by plasma-enhanced chemical vapor deposition (PECVD), in which gas molecules are decomposed in a plasma. On the other hand, catalytic CVD (Cat-CVD) is known as a method for the preparation of high-quality a-Si passivation films, since gas molecules are decomposed on a heated catalyzing wire, and thus, there is no plasma damage to substrates and films [6–9].

Due to low conductivity of doped a-Si, SHJ solar cells need transparent conductive oxide (TCO), such as indium tin oxide (ITO), for sufficient lateral carrier transport [10]. Sputtering method is, in general, one of the conventional processes to form ITO films. However, because of high-energy ion bombardment to a-Si passivation films, the passivation quality of a-Si films degrades [11–15]. The previous investigation of ITO sputtering damage for PECVD a-Si films has revealed that sputtering at room temperature (R.T.) and successive post-annealing are effective for the good passivation quality of a-Si films [16]. However, the effect of sputtering damage to Cat-CVD a-Si films has not been sufficiently studied so far. Our motivation in this work is to verify

whether the sputtering damage to various types of Cat-CVD a-Si passivation films is generated by ITO sputtering. We have also investigated the recovery of the passivation quality by tuning ITO deposition condition and/or performing a post-annealing.

## 2. Experimental procedure

To evaluate how passivation quality changes depending on the types of a-Si films, we prepared three kinds of samples, whose structures are schematically shown in Fig. 1. The deposition conditions of a-Si and ITO films are summarized in Table I. Note that substrate temperature and RF power during ITO sputtering were systematically changed from R.T. to 150 °C, and from 20 to 100 W, respectively, for optimizing the sample passivation quality. Due to the change of ITO deposition rate depending on RF power, deposition duration was varied from 15 to 100 min to keep a film thickness. Process pressure and Ar flow rate were fixed to 0.5 Pa and 13.6 sccm, respectively. A Sn-doped (5wt%) In<sub>2</sub>O<sub>3</sub> target with a diameter of 5 cm was used for the RF magnetron sputtering to deposit ITO films. At the beginning of the experiment, we used 290- $\mu$ m-thick floating-zone-grown n-type c-Si (100) wafers with a resistivity of 1–5  $\Omega$  cm, and a bulk carrier lifetime ( $\tau_b$ ) of > 10 ms. c-Si wafers were cleaved into 2 cm $\times$ 2 cm-sized pieces, and dipped in 5wt% HF for 30 seconds to remove native oxide and then in 4wt% H<sub>2</sub>O<sub>2</sub> for 30 seconds for the formation of ultra-thin oxide layers to avoid epitaxial growth [8, 17–19]. After that, a-Si films were deposited on the c-Si wafers immediately. For the structure shown in Fig. 1(a), 20-nm-thick intrinsic (i-) a-Si layers were deposited on both sides of c-Si wafers by Cat-CVD. For the structures shown in Figs. 1(b) and 1(c), 10-nm-thick i-a-Si layers were deposited on the front side of c-Si wafers, followed by the deposition of 10-nm-thick n-type (n-) a-Si and p-type (p-) a-Si layers, respectively.

20-nm-thick i-a-Si layers were deposited on the rear side of the c-Si wafers to improve their passivation quality. All the samples were then annealed at 200 °C for 10 hours in air. 70-nm-thick ITO layers were deposited by RF magnetron sputtering on the front side of the c-Si wafers, followed by post-annealing at 200 °C for up to 5 hours in air. The thicknesses of a-Si and ITO films were measured by spectroscopic ellipsometry (J. A. Woollam Co., WVASE32) through analyses using parametric semiconductor model and Cauchy model, respectively [20]. In order to evaluate the i-a-Si/c-Si interface passivation quality by measuring effective minority carrier lifetime ( $\tau_{\text{eff}}$ ), microwave photoconductivity decay ( $\mu$ -PCD) measurement (KOBELCO LTA-1510 EP) was performed using a pulse laser with a wavelength of 904 nm and a photon density of  $5 \times 10^{13} \text{ cm}^{-2}$ .

### 3. Results

#### 3.1. ITO sputtering on i-a-Si

Fig. 2 shows the  $\tau_{\text{eff}}$  for the samples with ITO films sputtered at R.T.–150 °C in the case of using the structure shown in Fig. 1(a). All the samples initially show good passivation quality before ITO sputtering. ITO sputtering on them leads to the degradation of the  $\tau_{\text{eff}}$  of all the samples because of RF plasma damage, which is quite similar to the case of PECVD films [12]. Hence, the influence of sputtering damage on the passivation quality of Cat-CVD a-Si passivation films is also considered to be a serious problem. After the post-annealing for 5 hours, the sample with ITO sputtered at R.T. and 50 °C show much higher  $\tau_{\text{eff}}$  than the sample with ITO sputtered at 100 and 150 °C. This means that ITO sputtering at lower substrate temperature is effective for more significant  $\tau_{\text{eff}}$  recovery. One possible reason for this phenomenon is that the

samples with ITO sputtered at lower temperature experience less hydrogen effusion during sputtering, resulting in more effective termination of dangling bonds by hydrogen during post-annealing [16].

Fig. 3 shows the  $\tau_{\text{eff}}$  for the structure shown in Fig. 1(a) with and without annealing before ITO sputtering. The sample with annealing before sputtering shows higher  $\tau_{\text{eff}}$  than that without annealing before sputtering after performing post-annealing, meaning the effectiveness of prior annealing before sputtering. This may be due to reduced defects on an a-Si/c-Si interface by hydrogen termination during annealing before ITO sputtering.

Fig. 4 shows the  $\tau_{\text{eff}}$  of the structure shown in Fig. 1(a) at various sputtering RF power as a function of post-annealing duration. It can be clearly seen that the sample with ITO deposited at lower RF power shows more effective recovery of  $\tau_{\text{eff}}$ . This is probably related to more significant sputtering damage at higher sputtering power to a-Si passivation layers and resulting less degree of recovery. On the contrary, the  $\tau_{\text{eff}}$  of the sample with ITO sputtered at low RF power continues to increase and exceeds the initial  $\tau_{\text{eff}}$  if the sample is annealed for long period. This indicates that ITO sputtering at lower RF power leads to more effective recovery of  $\tau_{\text{eff}}$ .

### 3.2. ITO sputtering on n-a-Si/i-a-Si

Fig. 5 shows the  $\tau_{\text{eff}}$  of the samples with ITO films sputtered at R.T. and 100 °C for the structure shown in Fig. 1(b). The  $\tau_{\text{eff}}$  of the sample with ITO sputtered at R.T. decreases drastically after sputtering, while the  $\tau_{\text{eff}}$  of the sample with ITO sputtered at 100 °C slightly decreases. This might be because the sample with ITO sputtered at 100 °C experiences additional annealing during sputtering. Both of the samples show

rapid  $\tau_{\text{eff}}$  recovery exceeding initial  $\tau_{\text{eff}}$  after post-annealing. In the case of ITO sputtering to n-a-Si/i-a-Si,  $\tau_{\text{eff}}$  is found to recover easily regardless of substrate temperature during ITO sputtering.

### 3.3. ITO sputtering on p-a-Si/i-a-Si

Fig. 6 shows the  $\tau_{\text{eff}}$  of the samples with ITO films sputtered at R.T. and 100 °C for the structure shown in Fig. 1(c). The  $\tau_{\text{eff}}$  of both samples decreases drastically after sputtering, and the  $\tau_{\text{eff}}$  of the sample with ITO sputtered at 100 °C remains low even after long post-annealing. On the contrary, the  $\tau_{\text{eff}}$  of the sample with ITO sputtered at R.T. recovers gradually by post-annealing, although  $\tau_{\text{eff}}$  does not recover to the initial  $\tau_{\text{eff}}$ .

Fig. 7 shows the  $\tau_{\text{eff}}$  of the samples for the structure shown in Fig. 1(c) with ITO sputtered at various sputtering RF powers as a function of post-annealing duration. Similar to the previous result concerning RF power dependence, the sample with ITO sputtered at low RF power shows effective  $\tau_{\text{eff}}$  recovery. On the contrary, the sample with ITO sputtered at high RF power shows no improvement in the passivation quality even after post-annealing. We have found that ITO sputtering with low RF power is effective for  $\tau_{\text{eff}}$  recovery for the p-a-Si/i-a-Si/c-Si structure.

## 4. Discussion

According to the experimental results shown above, we have found that the trend of  $\tau_{\text{eff}}$  recovery from ITO sputtering damage depends significantly on the types of a-Si films. We should therefore consider why the  $\tau_{\text{eff}}$  recovery depends on types of a-Si films. Minority carriers, holes, in c-Si near the a-Si/c-Si interface of ITO/n-a-Si/i-a-Si/c-Si

structure are driven back due to downward band bending originating from the existence of ITO, which leads to a high minority carrier lifetime. On the other hand, minority carriers tend to be accumulated near the a-Si/c-Si interface for the ITO/p-a-Si/i-a-Si/c-Si structure, and carrier recombination is enhanced at the interface [21]. Therefore, the reason for different trend of  $\tau_{\text{eff}}$  recovery depending on the types of a-Si films may be related to the modification of a-Si/c-Si band alignment due to the existence of ITO. In order to confirm whether the band alignment difference influences the sample passivation quality, the ITO films were etched off by dipping in 30wt% hydrochloric acid for 2 minutes from the n-a-Si/i-a-Si/c-Si and p-a-Si/i-a-Si/c-Si structures, followed by  $\tau_{\text{eff}}$  measurement. Fig. 8 shows the  $\tau_{\text{eff}}$  of the samples with and without ITO films. Note that  $\tau_{\text{eff}}$  is normalized by using  $\tau_{\text{eff}}$  before ITO sputtering ( $\tau_{\text{eff},0}$ ). For the samples with ITO sputtered to n-a-Si/i-a-Si stacked layers,  $\tau_{\text{eff}}$  before ITO removal exceeds initial  $\tau_{\text{eff}}$  regardless of substrate temperature during sputtering. ITO removal from them does not induce significant change in  $\tau_{\text{eff}}$  value. This fact indicates that the modification of the band structure of n-a-Si/i-a-Si stacked layer due to the existence of ITO does not affect the sample passivation quality. On the other hand, the sample with ITO sputtered to p-a-Si/i-a-Si stacked layers before ITO removal shows lower  $\tau_{\text{eff}}$  compared with initial  $\tau_{\text{eff}}$  value, especially for the sample with ITO sputtered at 100 °C. The removal of ITO results in the recovery of  $\tau_{\text{eff}}$  to initial  $\tau_{\text{eff}}$ . This result indicates that the sputtering damage to p-a-Si/i-a-Si/c-Si is fully recovered by performing post-annealing. To clearly understand the effect of post-annealing on  $\tau_{\text{eff}}$  recovery, we measured the  $\tau_{\text{eff}}$  of the samples after post-annealing and successive ITO removal. Fig. 9 shows the normalized  $\tau_{\text{eff}}$  of the samples for the structures shown in Figs. 1(b) and (c) after post-annealing for 0, 5, and 20 h and successive ITO removal. The samples without post-annealing show



lower  $\tau_{\text{eff}}$  values, while the  $\tau_{\text{eff}}$  of the samples are recovered to the initial values by 5- or 20-h post-annealing. Post-annealing after ITO sputtering is thus effective for the recovery of  $\tau_{\text{eff}}$  from sputtering damage. Favre *et al.* reported lower  $\tau_{\text{eff}}$  by the existence of ITO on p-a-Si particularly at a low excess carrier density ( $\Delta n$ ) region, which has been explained as the effect of carrier recombination at the ITO/p-a-Si interface [11]. On the basis of this consideration, the worse passivation quality of ITO/p-a-Si/i-a-Si stacked layers might be due to carrier recombination at the ITO/p-a-Si interface. To confirm the hypothesis, we measured the  $\tau_{\text{eff}}$  of the samples by quasi-steady state photoconductivity (QSSPC). Fig. 10 shows the  $\tau_{\text{eff}}$  of the samples before and after the removal of ITO films as a function of  $\Delta n$ . The  $\tau_{\text{eff}}$  of all the samples decreases at higher  $\Delta n$  region, which is caused by Auger recombination. A reduction in  $\tau_{\text{eff}}$  at lower  $\Delta n$  region is observed for the structure with p-a-Si, while such a  $\tau_{\text{eff}}$  reduction is not observed after the removal of ITO films. On the other hand,  $\tau_{\text{eff}}$  at lower  $\Delta n$  region is not reduced for the structure with n-a-Si. As mentioned above, reduction in  $\tau_{\text{eff}}$  at lower  $\Delta n$  region can be explained as carrier recombination at ITO/p-a-Si interface. Note that this is not the case for the structure with n-a-Si, because holes are not accumulated near ITO/n-a-Si interface due to downward band bending. In the SHJ solar cells, carrier recombination at the ITO/p-a-Si interface is essential for the collection of photo-generated carriers. It is thus inevitable that the sample with ITO/p-a-Si/i-a-Si stack layers shows worse passivation quality comparing with the sample with ITO/n-a-Si/i-a-Si stacked layers.

## 5. Conclusions

The passivation quality of Cat-CVD a-Si films are degraded by ITO sputtering damage.  $\tau_{\text{eff}}$  can recover by using ITO sputtered at R.T. and performing post-annealing.

Annealing before sputtering is effective for  $\tau_{\text{eff}}$  recovery. Lower sputtering RF power leads to less sputtering damage to a-Si passivation films. Long post-annealing is effective to obtain sufficiently high  $\tau_{\text{eff}}$ . The degradation of passivation quality by sputtering to n-a-Si/i-a-Si stacked layers easily recovers after short post-annealing. On the other hand, the degradation of passivation quality by sputtering to p-a-Si/i-a-Si stacked layers do not recovers sufficiently even after long post-annealing. The trend of  $\tau_{\text{eff}}$  recovery thus depends on the type of a-Si films. The modulation of the band alignment of a-Si/c-Si by the existence of ITO affects the passivation quality. This may be inevitable for SHJ solar cells if the worse passivation quality for the structure with ITO/p-a-Si/i-a-Si stacked layers is due to carrier recombination at the ITO/p-a-Si interface.

## References

- [1] M. Tanaka, M. Taniguchi, T. Matsuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa, Y. Kuwano, Development of new a-Si/c-Si heterojunction solar cells: ACJ-HIT (artificially constructed junction-heterojunction with intrinsic thin-layer), *J. Appl. Phys.* 31 (1992) 3518.
- [2] A. Descoedres, Z. C. Holman, L. Barraud, S. Morel, S. De Wolf, C. Ballif, >21 % efficient silicon heterojunction solar cells on n- and p- type wafers compared, *IEEE J. Photovolt.* 3 (2013) 83.
- [3] M. Taniguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, E. Maruyama, 24.7% record efficiency HIT solar cell on thin silicon wafer, *IEEE J. Photovolt.* 4 (2013) 96.
- [4] K. Masuko, M. Shigematsu, T. Hashiguchi, D. Fujishima, M. Kai, N. Yoshimura, T. Yamaguchi, Y. Ichihashi, T. Mishima, N. Matsubara, T. Yamanishi, T. Takahama, M. Taguchi, E. Maruyama, S. Okamoto, Achievement of more than 25% conversion efficiency with crystalline silicon heterojunction solar cell, *IEEE J. Photovolt.* 4 (2014) 1433.
- [5] T. Mishima, M. Taguchi, H. Sakata, E. Maruyama, Development status of high-efficiency HIT solar cells, *Sol. Energy Mater. Sol. Cell.* 95 (2011) 18.
- [6] H. Matsumura, K. Higashimine, K. Koyama, K. Ohdaira, Comparison of crystalline-silicon/amorphous-silicon interface prepared by plasma enhanced chemical vapor deposition and catalytic chemical vapor deposition, *J. Vac. Sci. Technol. B* 33 (2015) 031201.

- [7] S. Tsuzaki, K. Ohdaira, T. Oikawa, K. Koyama, H. Matsumura, Improvement in passivation quality and open-circuit voltage in silicon heterojunction solar cells by the catalytic doping of phosphorus atoms, *Jpn. J. Appl. Phys.* 54 (2015) 072301.
- [8] Q. Wang, M. Page, Y. Ai, W. Nemeth, L. Roybal, H. Yuan, Hydrogenated amorphous Si deposition for high efficiency a-Si/c-Si heterojunction solar cells, in: *Proc. 39th IEEE Photovolt. Spec. Conf.*, 2013, pp. 188–190.
- [9] K. Koyama, K. Ohdaira, and H. Matsumura, Extremely low surface recombination velocities on crystalline silicon wafers realized by catalytic chemical vapor deposited  $\text{SiN}_x/\text{a-Si}$  stacked passivation layers, *Appl. Phys. Lett.* 97 (2010) 082108.
- [10] M. Filipič, Z. C. Holman, F. Smole, S. De Wolf, C. Ballif, M. Topič, Analysis of lateral transport through the inversion layer in amorphous silicon/crystalline silicon heterojunction solar cells, *J. Appl. Phys.* 114 (2013) 074504.
- [11] W. Favre, J. Coignus, N. Nguyen, R. Lachaume, R. Cabal, D. Muñoz, Influence of the transparent conductive oxide layer deposition step on electrical properties of silicon heterojunction solar cells, *Appl. Phys. Lett.* 102 (2013) 181118.
- [12] B. Demarex, S. De Wolf, A. Descoedres, Z. C. Holman, C. Ballif, Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering, *Appl. Phys. Lett.* 101 (2012) 171604.
- [13] M. Tamakoshi, N. Matsuki, Impact of sputter-induced ion bombardment at the heterointerfaces of a-Si:H/c-Si solar cells with double-layered  $\text{In}_2\text{O}_3:\text{Sn}$  structures, *Jpn. J. Appl. Phys.* 54 (2015) 08KD09.
- [14] R. Rößler, C. Leendertz, L. Korte, N. Mingirulli, B. Rech, Impact of the transparent conductive oxide work function on injection-dependent a-Si:H/c-Si band bending and solar cell parameters, *J. Appl. Phys.* 113 (2013) 144513.

- [15] I. P. Sobkowicz, A. Salomon, P. R. Cabarrocas, Apparent doping-dependence of the a-Si:H/c-Si interface degradation upon ITO sputtering, in: Proc. 40th IEEE Photovolt. Spec. Conf., 2014, pp. 645–648.
- [16] D. Zhang, A. Tavakoliyaraki, Y. Wu, R. A. C. M. M. van Swaaij, M. Zeman, Influence of ITO deposition and post annealing on HIT solar cell structures, Energy Proc. 8 (2011) 207.
- [17] T. Oikawa, K. Ohdaira, K. Higashimine, H. Matsumura, Application of crystalline silicon surface oxidation to silicon heterojunction solar cells, Current Appl. Phys. 15 (2015) 1168.
- [18] K. Ohdaira, T. Oikawa, K. Higashimine, H. Matsumura, Suppression of the epitaxial growth of Si films in Si heterojunction solar cells by the formation of ultra-thin oxide layers, Current Appl. Phys. 16 (2016) 1026.
- [19] S. De Wolf, M. Kondo, Abruptness of a-Si:H/c-Si interface revealed by carrier lifetime measurement, Appl. Phys. Lett. 90 (2007) 042111.
- [20] Guide to Using WVASE32TM:Software for Vase and M-44 Ellipsometers, J.A.Woollam Co., Inc., 1989, 159-165.
- [21] M. Bivour, C. Reichel, M. Hermle, S. W. Glunz, Improving the a-Si:H(p) rear emitter contact of n-type silicon solar cells, Sol. Energy Mater. Sol. Cell. 106 (2012) 11-16.

## Figure captions

Fig. 1 Schematic of the sample structure with (a) ITO/i-a-Si, (b) ITO/n-a-Si/i-a-Si, and (c) ITO/p-a-Si/i-a-Si stacked films.

Fig. 2  $\tau_{\text{eff}}$  for the structure shown in Fig. 1(a) as a function of substrate temperature during ITO sputtering. RF power during sputtering was fixed to 50 W. The left, center, and right figures indicate  $\tau_{\text{eff}}$  after a-Si deposition and 10 h annealing, after following ITO sputtering, and after successive 5 h post-annealing, respectively.

Fig. 3  $\tau_{\text{eff}}$  for the structure shown in Fig. 1(a) with and without annealing before ITO sputtering. RF power and substrate temperature during sputtering were fixed to 50 W and R.T. respectively.

Fig. 4  $\tau_{\text{eff}}$  for the structure shown in Fig. 1(a) at various sputtering RF power as a function of post-annealing duration. Substrate temperature during sputtering was fixed to R.T.. Opened markers indicate the  $\tau_{\text{eff}}$  of the sample with annealing before sputtering.

Fig. 5  $\tau_{\text{eff}}$  of the samples with ITO sputtered at R.T. and 100 °C for the structure shown in Fig. 1(b). RF power during sputtering was fixed to 50 W.

Fig. 6  $\tau_{\text{eff}}$  of the samples with ITO sputtered at R.T. and 100 °C for the structure shown in Fig. 1(c). RF power during sputtering was fixed to 50 W.

Fig. 7  $\tau_{\text{eff}}$  of the structure shown in Fig. 1(c) at various sputtering RF powers as a function of post-annealing duration. Substrate temperature during sputtering was fixed to R.T.. Opened makers indicate the  $\tau_{\text{eff}}$  of the sample with annealing before sputtering.

Fig. 8  $\tau_{\text{eff}}$  of the samples for the structures shown in Figs. 1(b) and (c) before and after ITO removal.  $\tau_{\text{eff}}$  is normalized by using initial  $\tau_{\text{eff},0}$ , and the sample before ITO removal experienced 20-h post-annealing.

Fig. 9  $\tau_{\text{eff}}$  of the samples for the structures shown in Figs. 1(b) and (c) after ITO removal. Left, center, and right figures indicate the  $\tau_{\text{eff}}$  of the samples with 0, 5, and 20-h post-annealing and following ITO removal, respectively.  $\tau_{\text{eff}}$  is normalized by using initial  $\tau_{\text{eff},0}$ .

Fig. 10  $\tau_{\text{eff}}$  of the samples for the structures shown in Figs. 1(b) and (c) before and after ITO removal as a function of  $\Delta n$  measured by QSSPC. ITO films were deposited at a RF power of 50 W and a substrate temperature of 100 °C, followed by post-annealing for 15 h.

Table I Deposition conditions for a-Si and ITO films.

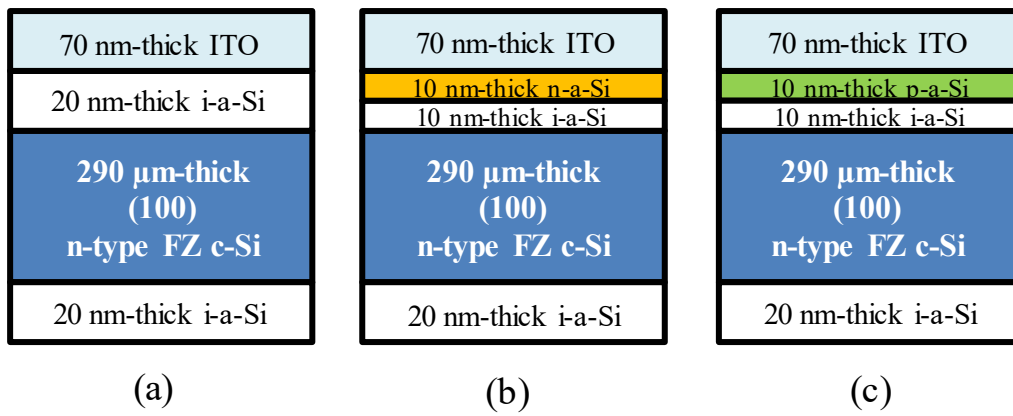


Fig. 1



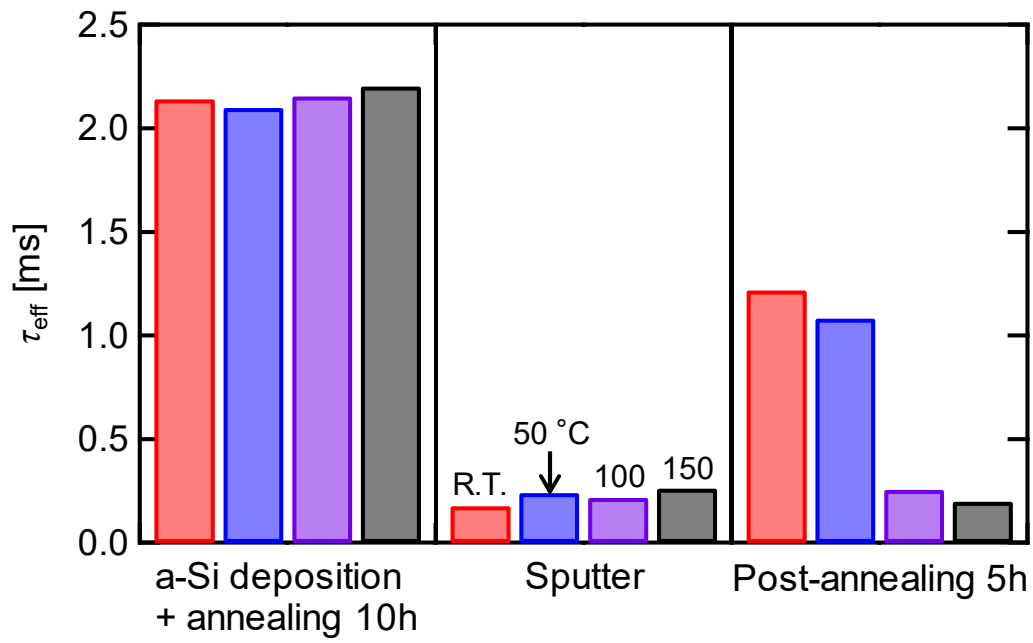


Fig. 2

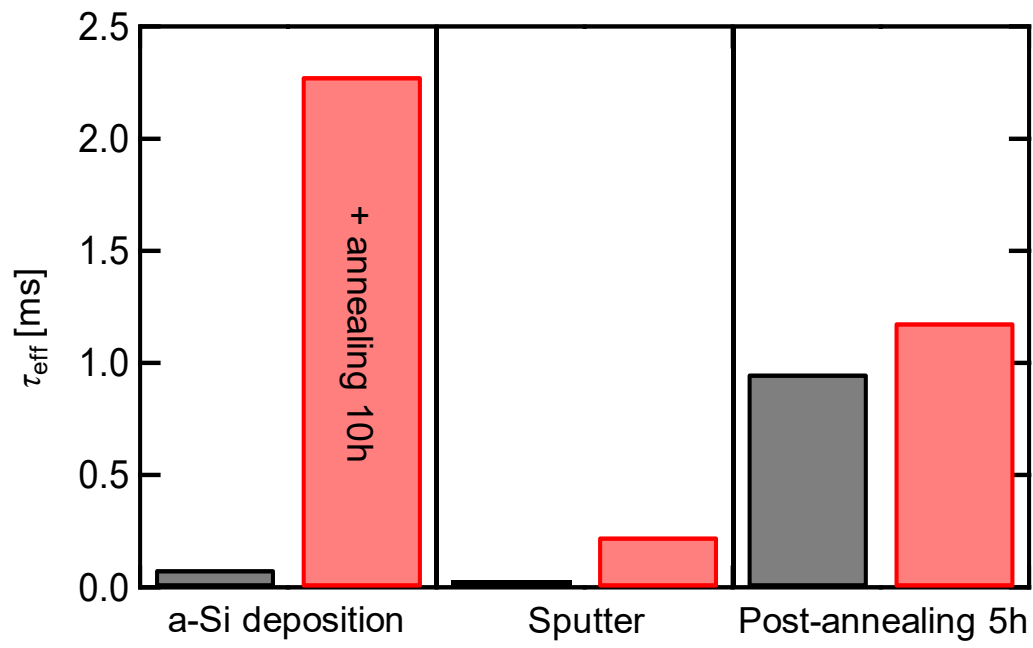


Fig. 3

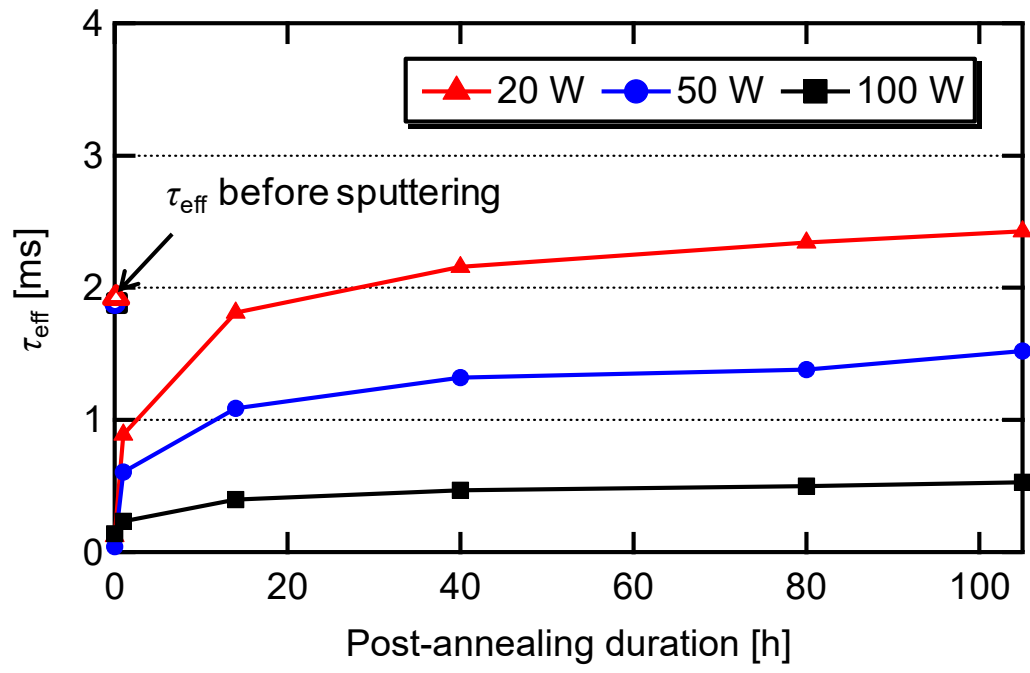


Fig. 4

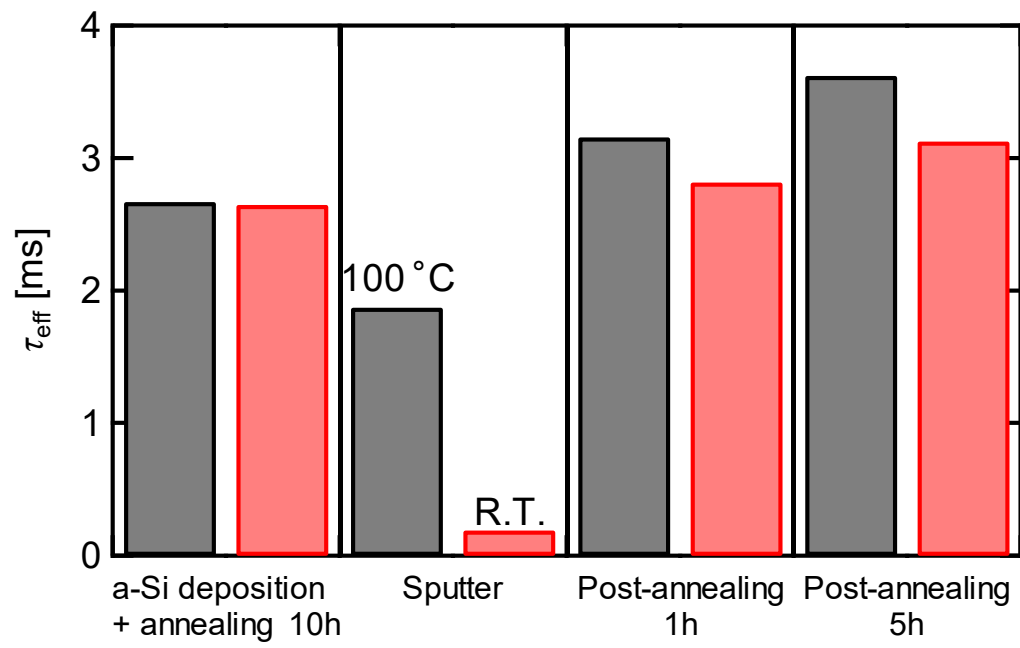


Fig. 5

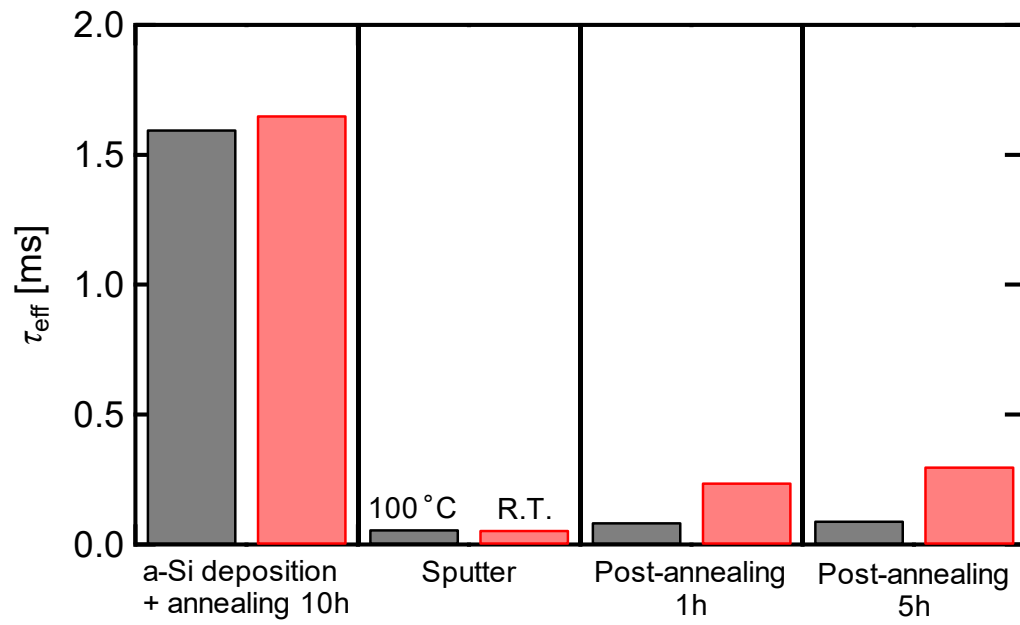


Fig. 6

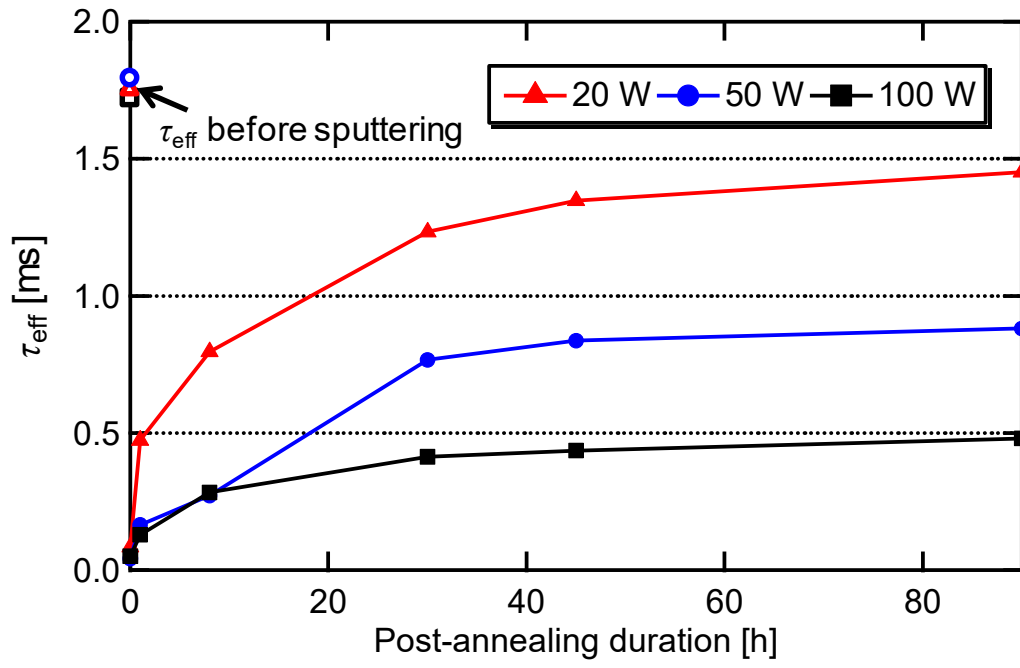


Fig. 7

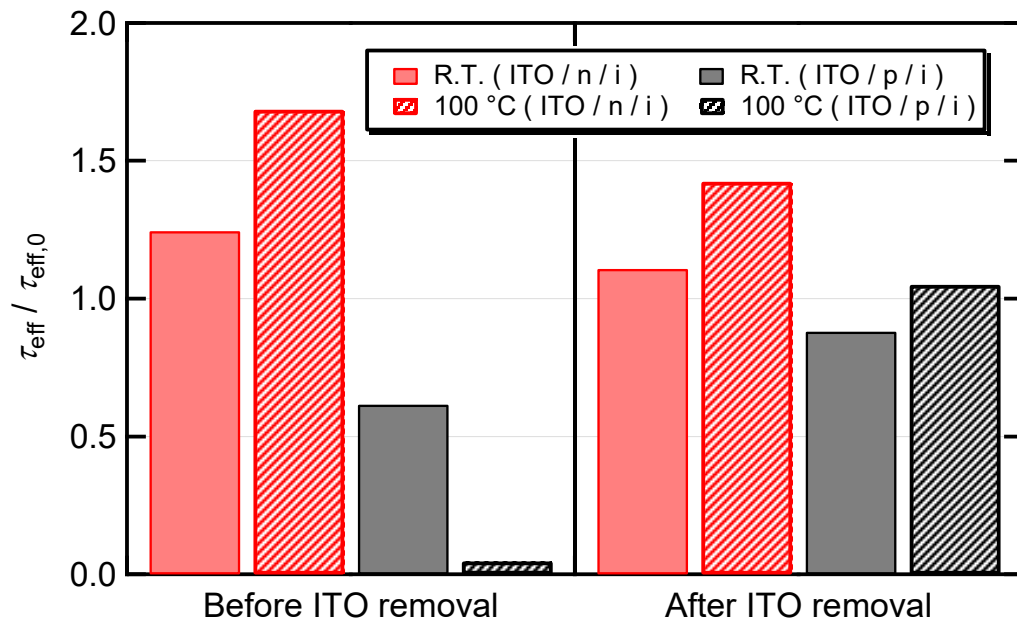


Fig. 8

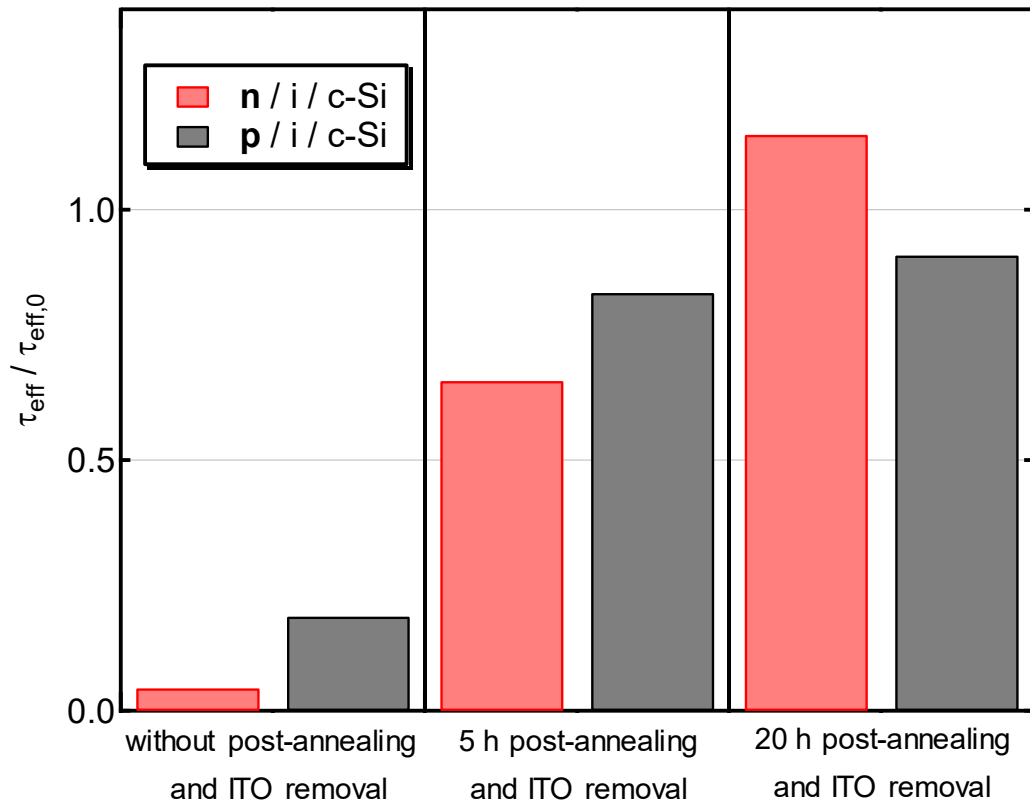


Fig. 9



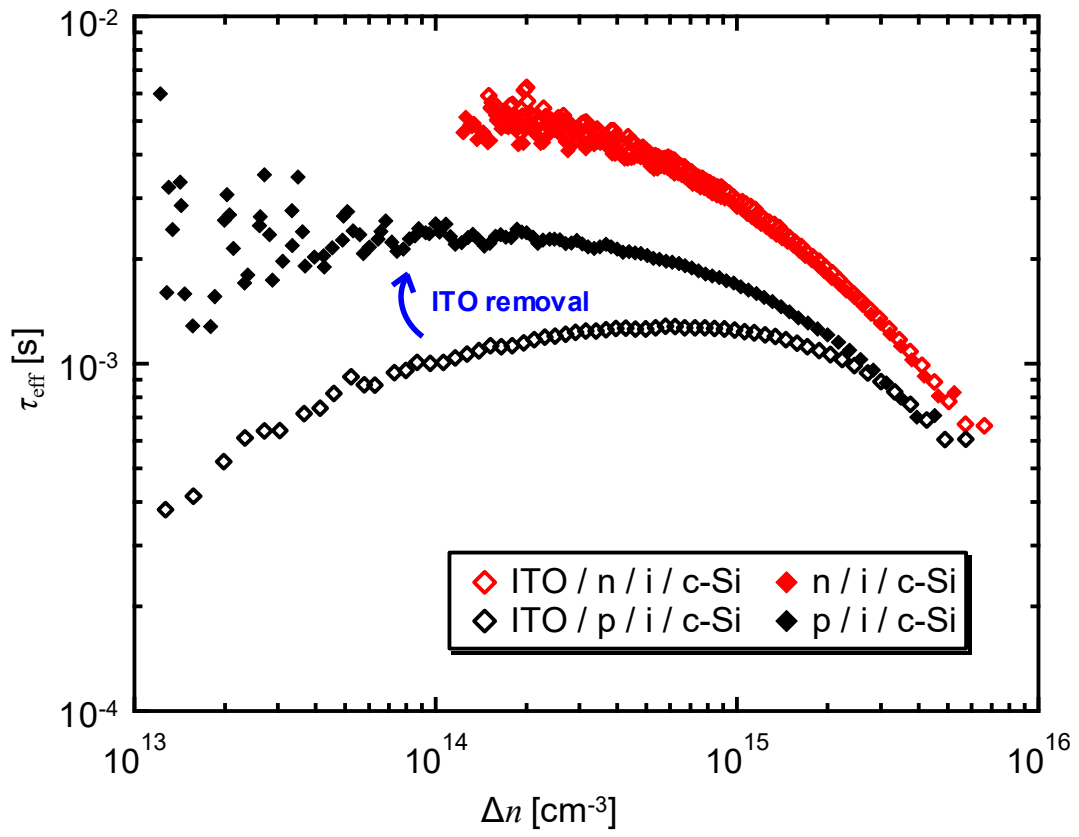


Fig. 10

Cat-CVD	T <sub>sub</sub> [°C]	T <sub>cat</sub> [°C]	Duration [s]	Pressure [Pa]	Gas flow rate [sccm]			
					SiH <sub>4</sub>	H	He:PH <sub>3</sub>	He:B <sub>2</sub> H <sub>6</sub>
<b>i-a-Si</b>	125	1800	45, 100	1	10	-	-	-
<b>n-a-Si</b>	250	1800	35	2	10	-	4.4	-
<b>p-a-Si</b>	250	1800	80	2	10	50	-	16

Sputter	T <sub>sub</sub> [°C]	RF Power [W]	Duration [min]	Pressure [Pa]	Gas flow rate [sccm]
					Ar
<b>ITO</b>	R.T.–150	20–100	100–15	0.5	13.6

Table 1