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論文の内容の要旨

## 1. Research content

### 1.1 Introduction

Indium oxide ($In_2O_3$) and indium tin oxide (ITO) are very mature metal-oxides, which have been in research from many years due to the advantages that they show n-type semiconducting behaviour with high transparency in visible light. Due to these properties, ITO is used as a transparent electrode in thin-film-transistor liquid-crystal display (TFT-LCD), organic solar-cells, electrochromic devices, window coatings, gas sensors, and touch screens.

To fabricate $In_2O_3$ and ITO films, various methods have been used such as sputtering, pulsed laser deposition (PLD), spray pyrolysis, vacuum evaporation, and solution process, etc. Among them, the solution process has advantages over other techniques, such as low-cost (as it does not require costly vacuum system), less time requirement (as no need for vacuum formation). Also, solution process is compatible with printing techniques, ease to coat on substrates with different geometries, simple processing, feasibility of direct patterning, with good source consumption efficiency.

Printed electronics have recently gained attention due to their low environmental impact, fewer fabrication steps, large area fabrication, ease of patterning on organic and inorganic substrates and low cost. Among various printed electronics techniques, inkjet printing is a popular method, but is not appropriate for the miniaturization of advanced electronic devices as the required resolution is sub-micrometers or less, which cannot be realized by inkjet printing. Furthermore, it is hard to achieve precise shape control of the

film via inkjet printing. A novel printing technique known as nano-rheology printing (n-RP), based on direct imprinting of precursor gel films, can fabricate patterns as small as 100 nm with good shape control. n-RP is a resist-free, direct printing method which utilizes the rheological properties of a metal-oxide precursor gel to form patterns in the precursor gel.[1)]

In this work, at first electrical and patterning properties of $In_2O_3$ and ITO were studied by n-RP process. Also, the electrical properties of imprinted $In_2O_3$ and ITO films were also studied and compared with that of non-imprinted films. Finally, bottom gate thin film transistor (TFT) using n-RP, has been fabricated with solution process derived $In_2O_3$ as a channel and source/drain; while solution process derived $HfO_2$ as a gate insulator. Platinum (Pt) is used as gate electrode.

## 2. Research Purpose

The objective of this research is to study the electrical properties of $In_2O_3$ and ITO film prepared by the n-RP process and to fabricate TFT using n-RP process with chemical solution processed $In_2O_3$ as channel and solution processed $HfO_2$ as a high-*k* gate insulator.

### 2.1 Results and Discussion

At first $In_2O_3$ thin films were prepared by solution process using indium acetyacetonate ($In(acac)_3$) as a precursor in propionic acid (PrA). The electrical properties of $In_2O_3$ were studied by varying annealing time and annealing temperature. An optimum condition was obtained at which high mobility and carrier concentration were obtained. It is found that high mobility of around 42.7 $cm^2$ /Vs with a carrier concentration of 9.47 x $10^{18}$ $cm^{-3}$ is obtained when $In_2O_3$ precursor gel film was annealed in $O_2$ at 600 ºC annealing for 1h. Then ITO thin films were prepared using two different precursors of tin (Sn), keeping $In(acac)_3$ in PrA, same. One precursor was tin acetylacetonate ($Sn(acac)_2$) and another was tin chloride ($SnCl_2$). ITO films were also annealed in $O_2$ for 1 h at 600 ºC. ITO concentration was varied from 1 to 10 wt.%. It is found that as the Sn concentration increases, mobility decreases due to the reason that Sn acts as impurity in $In_2O_3$ cubic bixbyite structure. Therefore, more the Sn content, more impurity scattering, hence less mobility. The resistivity as low as 2.6 x $10^{-3}$ Ωcm for our ITO films was obtained for 1 wt.% ITO via $Sn(acac)_2$ with a mobility of 24 $cm^2$/Vs and carrier concentration of 1.0 x $10^{20}$ $cm^{-3}$, when ITO film was annealed in $O_2$ for 1 h at 600 ºC. Figure 1 shows resistivity of ITO films prepared by $SnCl_2$ and $Sn(acac)_2$. Resistivity of $In_2O_3$ films is also shown in Fig. 1, for reference.

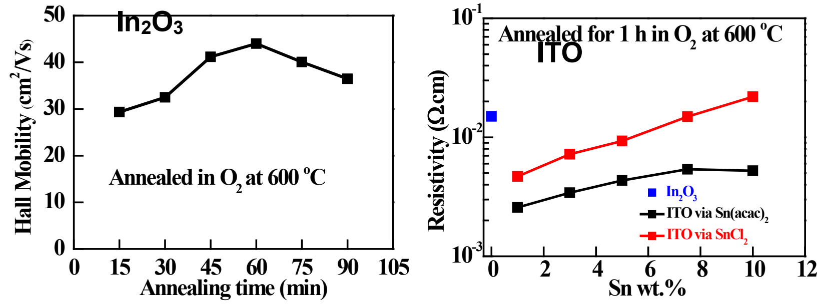


**Fig. 1:** (a) Hall mobility of $In_2O_3$ and (b) resistivity of ITO with respect to Sn wt.%.

Figure 2 shows the patterns of $In_2O_3$ and ITO formed by using n-RP, while Fig. 3 shows the electrical properties of imprinted and non-imprinted $In_2O_3$ and ITO films. Figure 2 shows that with the addition of tin (Sn) to $In_2O_3$ (i.e. ITO) degrades the n-RP properties because the tan δ value of ITO is smaller than that of $In_2O_3$ (tan δ is a measure of viscoelasticity of a material. It is 1 for viscoelastic material, less than1 for solids and greater than 1 for liquids). From Fig. 3, it is seen that, the electrical properties of imprinted ITO films are not altered as much as compared to non-imprinted ITO films, but are greatly affected in the case of imprinted $In_2O_3$ compared to the non-imprinted $In_2O_3$ films. The Hall mobility of imprinted $In_2O_3$ decreases due to the trapped carbon, as confirmed by SIMS measurements, which showed that even after annealing at 600 °C for 1 hour, there was more carbon in the imprinted $In_2O_3$ than non-imprinted $In_2O_3$. An increase in the carrier concentration in imprinted films is due to the increase in oxygen vacancies in $In_2O_3$ after imprinting, as confirmed by XPS studies.

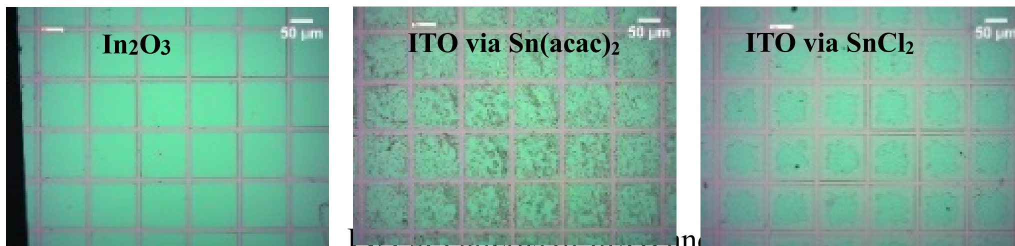


**Fig. 2:** Patterns of $In_2O_3$ and ITO.

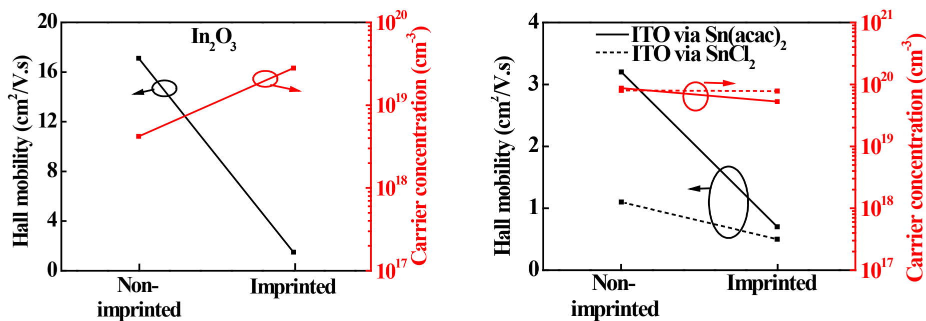


**Fig. 3:** Electrical properties of imprinted and non-imprinted $In_2O_3$ and ITO.

Since the high-*k* gate insulator is required to fabricate TFTs using $In_2O_3$ with relatively

high carrier concentration, $HfO_2$ films were fabricated by the solution process. Polarization-electric field (P-E) and capacitance-voltage (C-V) of the solution processed $HfO_2$, fabricated using hafnium acetylacetonate (Hf(acac)$_4$) in PrA and annealed in $O_2$ at 700 °C for 15 min is shown in Fig 4. It is seen from Fig. 4 that pure $HfO_2$, is linear in nature and shows paraelectricity. The extracted relative dielectric constant ($\varepsilon_r$) from the P-E slope and C-V is 17, while the leakage current density at 1 MV/cm is 1.0 x $10^{-6}$ A/cm$^2$ with breakdown field of 5.8 MV/cm.

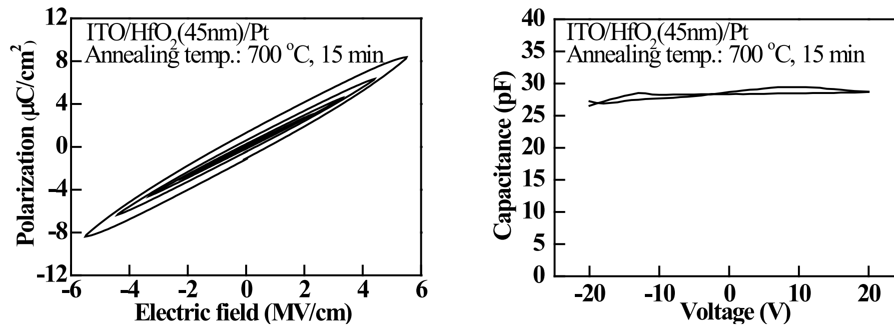


**Fig. 4:** Electrical properties of $HfO_2$ thin films annealed at 700 °C for 15 min in $O_2$.

Figure 5 shows the schematic structure of TFT fabricated by n-RP process. It can be seen that using n-RP, the fabricated TFT has source/drain and channel, all are fabricated by the same material in just one press, simultaneously.

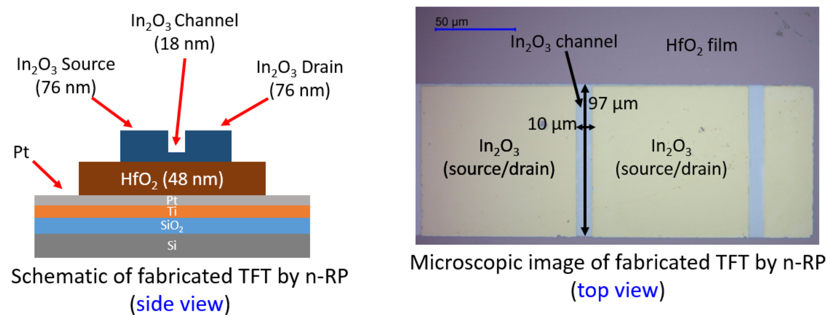


**Fig. 5:** Schematic of TFT fabricated by n-RP process.

Normal n-channel transistor operation was observed. The calculated TFT parameters are, on/off ratio is in the order of ~$10^5$, SS: 2.3 V/dec, mobility: 0.13 cm$^2$/Vs, and threshold voltage: 1.9 V.

**Keywords:** solution process, imprinting, oxide-semiconductors, high-*k* dielectric, thin film transistors

## 論文審査の結果の要旨

薄膜トランジスタ（TFT）は液晶ディスプレイや有機 EL ディスプレイの主要素子であるが、ディスプレイの超高精細化、さらには将来の IoT 社会に向けた多様なセンサ等のニーズの高まりに伴い、微細化した TFT を大面積で安価に製造する技術が求められている。本論文では、比較的移動度の大きい $In_2O_3$ 系酸化物半導体に着目し、溶液プロセスと直接ナノインプリント（ナノレオロジープリンティング : n-RP）を用いた新しい TFT 作製技術の基礎を確立することを目的としている。特にソース/ドレインとチャネルに同一材料を用い、両者を n-RP で一括形成する簡便で独創的な手法を採用している。

本論文では、最初にインジウムアセチルアセトナート（$In(acac)_3$）、塩化スズ（$SnCl_2$）またはスズアセチルアセトナート（$Sn(acac)_2$）をプロピオン酸に溶解して $In_2O_3$ およびインジウムスズ酸化物（ITO）の原料溶液を調製し、$SiO_2$/Si 基板上にスピンコートして乾燥した後に焼成し、薄膜を形成して特性を評価している。$In_2O_3$ 膜では 600℃アニール後に 43cm$^2$/Vs、ITO 膜（Sn1%）では 24 cm$^2$/Vs という大きな移動度が得られている。また Sn 添加量を増加すると移動度が低下すること、Sn 原料として塩化スズを用いた場合よりも $Sn(acac)_2$ を用いた場合に高い移動度が得られることを明らかにしている。次に、n-RP によるパターン形成実験を様々な条件下で実施し、Sn 原料の添加によってパターンの成型特性が劣化することを示すとともに、ゲル膜を剥離後ペレット化して粘弾性測定を行い、$In_2O_3$ の場合には Sn を添加した ITO と比較して、インプリント時の温度においてより「柔らかく」なることを明らかにしている。次に、10mm 角のガラス片をモールドとして用いて比較的大面積のインプリント領域を形成して Hall 測定により電気的特性を評価し、特に $In_2O_3$ のインプリントした領域で移動度の低下とキャリア濃度の上昇を観測している。さらに、$In_2O_3$ のインプリント領域では、600℃のアニール処理後においても多量の残留炭素が存在することを 2 次イオン質量分析（SIMS）により、また膜中の酸素欠損が多いことを X 線光電子分光法（XPS）により示し、インプリント工程による電気的特性の変化の原因を明らかにしている。次に TFT のゲート絶縁膜として高誘電率材料の $HfO_2$ を選択し、溶液プロセスにより薄膜を形成して特性を評価し、700℃アニールした試料において良好な絶縁特性を得ている。最後にこれらの成果を基にして、$HfO_2$ ゲート絶縁膜上に $In_2O_3$ 原料溶液を塗布・乾燥させ、n-RP を用いてソース/ドレインとチャネルを一括形成して TFT 構造を作製した。作製した TFT の電気的特性を評価したところ、良好な飽和特性と $10^5$ 程度と比較的大きなオンオフ比をもつ n チャネルのトランジスタ動作を確認することに成功している。

以上、本論文は、溶液プロセスと直接インプリントの手法を用いた新しい薄膜トランジスタの作製方法を示し、インプリント工程による $In_2O_3$ 系薄膜の電気的特性への影響を明らかにするとともに、TFT を作製してトランジスタ動作を確認することに成功したもので、学術上、応用上双方の観点から価値の高いものである。よって博士（マテリアルサイエンス）の学位論文として十分価値あるものと認めた。