# Performance of Hierarchical Torus Network: HTN

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## 1 Introduction

The demand for even more computing power has never stopped. It is increasing day by day. Areas requiring great computational speed include numerical modeling and simulation of scientific and engineering problems. These include modeling large DNA structures, global weather forecasting, modeling motion of astronomical bodies, fusion energy research, artificial intelligence, and computer vision. In order to solve these grand challenge problems, the goal has been to obtain computer systems capable of computing at the teraflops ($10^{12}$ floating-point operations per second) or petafloaps($10^{15}$ floating-point operations per second) level. Parallel computers with multiple processors are opening the door to these levels of computing performance to meet the increasing demand of computation power.

Although the theoretical foundations for constructing large interconnection networks for massively parallel computer system have existed for a long time, the state of the hardware technology did not allow their cost-effective realization. But, the recent advance in the VLSI technology overcomes this drawback. The recent progress in the VLSI technology achieves VLSI system on stacked silicon planes. On a stacked silicon plane, a part of massively parallel computers is implemented and some of these silicon planes are interconnected. Reducing the peak number of vertical links is also a critical issue for 3D-Wafer Stacked Implementation (3D-WSI). Hierarchical interconnection network minimizes the vertical links for efficient 3D stacked implementation. Hierarchical interconnection networks are suitable for 3D stacked implementation. It is intuitively appealing when a large number of nodes are connected.

When millions of nodes are interconnected together, then the peak number of vertical links of conventional topologies is intolerable. Some hierarchical networks have already been proposed to reduce the peak number of vertical links. But the dynamic communication performance is not good. For efficient 3D-WSI realization, it is essential to design a network which has smaller number of vertical links, while retaining good dynamic communication performance. In this research, we propose a new hierarchical interconnection network, called Hierarchical Torus Network (HTN) for massively parallel computers. HTN possesses better dynamic communication performance with efficient 3D-WSI realization .

## 2 Architecture of the HTN

In this paper, we propose a new hierarchical interconnection network called Hierarchical Torus Network (HTN). It consists of Basic Modules (BM) and the BMs are hierarchically interconnected for higher level networks. The basic module of the HTN is a 3D-torus network of size $(m \times m \times m)$, where $m$ is a positive integer. $m$ could be any value, however, the preferable one is $m = 2^p$, where, $p$ is a positive integer. Successively higher level networks are built by recursively interconnecting next lower level subnetworks in a 2D-torus of size $(n \times n)$, where $n$ is also a positive integer. Both the BM and the interconnection of higher levels have a toroidal interconnection. So, it is called Hierarchical Torus Network (HTN).

The BM has some free ports at the contours of the $xy$-plane. These free ports are used for higher level interconnection. All ports of the interior Processing Elements (PEs) are used up for intra-BM connections. The exterior PEs, however, have either one or two free ports. These free ports and their associated links are used for inter-BM interconnections to form higher level networks. Four links in the North (N), South (S), East (E), and West (W) directions on each contour are interconnected with higher levels. For higher level interconnection, subnet modules with the same address are interconnected by 2D-torus.

## 3 Performance of HTN

An interconnection network should transfer a maximum number of messages in the shortest time with minimum cost and maximum reliability. Clearly, any design of an interconnection network is a trade-off of various parameters. We studied various aspects of HTN in order to set-about it as a better interconnection network.

### 3.1 Static Network Performance

An interconnection network is represented as a graph and also referred to as topology. Evaluation parameters of static network performance to be considered include degree, diameter, cost ($= degree \times diameter$), average distance, bisection bandwidth, connectivity. From the static network performance, it is seen that the HTN possesses several attractive features including fixed diameter, small diameter, reasonable cost, and small average distance. The bisection width of the HTN is higher than TESH and H3D-mesh network, equal to H3D-torus network and smaller than conventional topologies respectively.

### 3.2 3D-WSI Performance

VLSI design issue deals with the efficient layout of a desirable network topology on an integrated circuit. Two frequently used parameters to measure an efficient layout are the layout area and maximum wire length. The recent progress in the VLSI technology achieves 3D computer systems on silicon planes. In the implementation of interconnection network on 3D wafer stacked planes, one of the most important parameter is the peak number of vertical links between adjacent silicon planes. It is shown that the peak number of vertical links in 3D wafer stacked implementation is quite low for HTN as compared to

other similar networks. Thus, HTN permits efficient VLSI/ULSI/WSI realization. The layout area of HTN in 3D wafer stacked implementation is amenable to 3D implementation. The maximum wire length of HTN is smaller than several other networks for parallel computers.

### 3.3 Dynamic Communication Performance

Dynamic communication performance is measured by message latency and network throu -ghput. For the network to have good performance, low latency and high throughput must be achieved. We have been evaluated the dynamic communication performance of HTN as well as several other commonly used networks and hierarchical interconnection networks for parallel computers by dimension order routing under uniform traffic pattern. The comparison of dynamic communication performance reveals that HTN outperforms mesh, torus, TESH, H3D-mesh, and H3D-torus networks.

### 3.4 Redundancy and Yield

Fault tolerant networks are essential to the reliability of massively parallel computer systems. A fault-tolerant network has the ability to route information with the presence of certain faults in the network. In hardware based technique, network is enhanced by additional hardware and providing enough redundancy in the original network design to tolerate a certain number of faults. We have been evaluated the redundancy and yield of HTN by providing redundancy. It is shown that the yield of HTN is satisfactory with 25% redundancy.

### 3.5 Application Mapping

The suitability of an interconnection network for certain application can often be estimated by studying how efficiently common operations such as sorting, broadcasting, and so on, can be performed on the given network. We have discussed some advanced applications, namely bitonic sort, FFT, and finding the maximum value on HTN. It is shown that HTN yields better performance than 2D-torus and 3D-torus networks.

## 4 Conclusions

In this thesis paper, we have proposed a new hierarchical interconnection network, called Hierarchical Torus Network (HTN) for massively parallel computers. We have studied various aspects of HTN in order to set-about it as a better interconnection network. The interconnection philosophy of the HTN, routing of messages, static network performance, 3D-wafer stacked implementation issue, dynamic communication performance, redundancy & yield, and application mapping were discussed in detail. We have compared performance in different aspects between proposed HTN and several other conventional networks & hierarchical interconnection network to show the superiority of HTN over them. Issues for future works include: dynamic communication performance by adaptive routing algorithm for different traffic pattern, fault-tolerance performance, embedding of other frequently used topologies into the HTN, and more on application mapping.