Research on the hardware scheduler in a Real-Time system

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February 13,2003

キーワード: Real-Time、hardware-scheduler、embedded system .

1 Introduction

An enbedded system must ensure realtime which is higyly reliable. therefore scheduling process which chose task and control the timing to execute it, affect the number of task which could be deadline-over.

This paper proposes the small-scale processor which provide various scheduling algorithm. This is added to the exterior of a processor core.The rate of effective execution of a processor is raised.The change of a task is notified to a processor to exact timeing.It aims at reducing the number of tasks used as a deadline miss.

2 Real-Time system

Real-time is not that calculation processing speed is only quick and that reaponce time is short ,but satisfies the defined requirements for time, and operates. When only single processing should be performed in a real-time system, a computer can be concentrated on the processing.but, when there are two or more processings which should be performed and the timeing which should perform processing is given forom the outside, the real-time system must be multitasking. therefore Scheduler which determines which task is performed is important for the computer of the limited throughput which performs real-time multitasking processing efficiently.

3 hardware scheduler

In this paper, a part of scheduler is imprimented as a high efficiency interrption controller. a high efficiency interrption controller run in parallel with main processor.thefore

the overhead by scheduling is cut down. and there is an effect which cuts down the number of tasks used as a deadline-over. a high efficiency interruption controller always supervises a deadline. a high efficiency interruption controller judge whether the task is necessary to contiue execution when the task was deadline-over. and when this controler stop executed task, this controler notifies to a processor about changing task.

because a high efficiency interruption controller is command execution type. Not only specific algorithm, its possible to impliment scheduling algorithm of various kinds.

this contoroler run as a processor only for schedluing. Since this system run as a embeded system, this controler need be made at minimum.so this controler have a minimum of instruction, and does not have multiplier and dividing circuit. by the same reason, this controler have 16-bit register at minimum. this controler have 16-bit memory which shared a part of memory which is used by main processor. this controler have data-chache and instruction-chache for memory access.it reduce the opportunities for memory access, and reduce the opportunities for colision of memory access.

4 Evaluation

4.1 hardware size

high efficiency interruption controller was designed by hardware description language.Evaluation of the amount of hardwares was performed using 0.25 μ ASIC library by design compiler of Synopsys Corp.

4.2 how to si

ソフトリアルタイム，ハードリアルタイムタスクが混在するシステムにおいて，メインプロセッサがタスク処理をおこなう一方で，高機能割り込みコントローラが並列してスケジューリングをおこなうことを仮定し、代表的なスケジューリングアルゴリズムを使用しシミュレーションをおこなった。

4.3 Evalustion of hardware scheduler

代表的なアルゴリズムでハードウェアスケジューラを使用することによって，平均で12.26パーセントデッドラインミスが減少した．ハードリアルタイムタスクを強制終了した場合の平均は，20.62パーセント，ハードリアルタイムタスクを強制終了しない場合の平均は3.9パーセントデッドラインミスが減少した．

5　おわりに

ハードウェアスケジューラの提案をおこない，デッドラインオーバーとなるタスクの削減をおこなった．提案したハードウェア量について評価した．提案したハードウェアを用いたシミュレーションをおこない，様々なアルゴリズムで評価した．