Review

Potential-induced degradation in high-efficiency n-type crystalline-silicon photovoltaic modules: A literature review

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Abstract

n-type crystalline-silicon (c-Si) photovoltaic (PV) cell modules attracts attention because of their potential for achieving high efficiencies. The market share of n-type c-Si PV modules is expected to increase considerably, with wide use in PV systems, including large-scale PV systems, for which the system bias is set as markedly high. Such a high system bias leads to performance losses known as potential-induced degradation (PID). By virtue of many researchers' efforts, the PID behaviors, PID mechanisms, and preventive measures against PID have been well documented in conventional p-type c-Si modules. Researchers recently started to investigate PID in high efficiency c-Si solar cells including n-type c-Si PV modules. Yet, the understanding of PID phenomena remains incomplete. Herein, a literature review of PID in high-efficiency n-type c-Si PV modules is provided as a resource elucidating the current status of related research and remaining unresolved issues. This report mainly presents discussion of PID in several kinds of n-type c-Si PV modules in terms of materials science. PID phenomena are described as divided into some degradation modes. Details present a review of their respective degradation modes, degradation behaviors, proposed mechanisms, and potential measures against degradation. Remaining open issues and anticipated future studies are also summarized.

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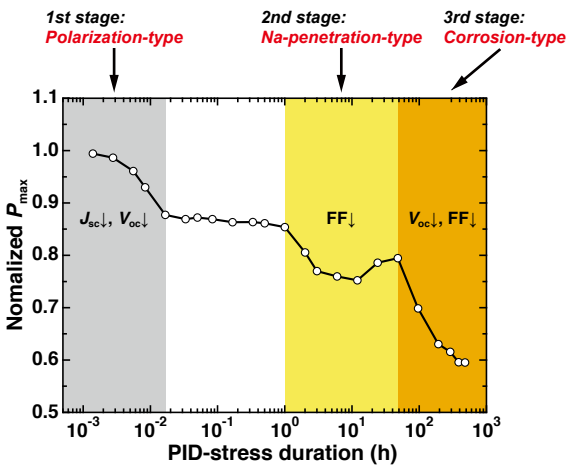

Potential-induced degradation (PID) of photovoltaic (PV) modules has been identified as a central issue in large-scale PV systems. This review surveys PID and related phenomena in several high-efficiency n-type crystalline-silicon (c-Si) PV cell modules. These PV cell modules reportedly undergo three PID types with different mechanisms depending on the cell structure. As described herein, details of these three types of PID, polarization-type PID, Na-penetration-type PID, and corrosion-type PID are discussed. This report also presents remaining unresolved issues and anticipated avenues of future studies.

1. Introduction

Crystalline-silicon (c-Si) photovoltaic (PV) cells fabricated from n-type c-Si wafers, so-called n-type c-Si PV cells, have attracted attention because of their potential to achieve higher efficiencies than those available from p-type cells. These n-type c-Si PV cells are based on high-quality n-type base materials, for which the minority-carrier lifetimes are generally long because of the small impurity capture cross-sections for minority carriers.[1] This phenomenon engenders higher open-circuit voltages (V_{oc}s) and short-circuit current densities (J_{sc}s) and the consequent higher cell efficiencies than those of p-type materials.[2] The silicon heterojunction (SHJ) solar cell, with its 26.7% record efficiency,[3] and the tunnel oxide passivating contact (TOPCon) solar cell, with 25.7% record efficiency,[4] are both categorized as n-type c-Si solar cells. Their performance attests to the high potential for n-type c-Si PV cell capabilities. Additionally, they are known to be adversely affected to only a slight degree by light-induced degradation resulting from the formation of metastable boron–oxygen complexes.[5, 6] By contrast, that type of degradation is frequently observed in conventional p-type c-Si PV cells. Consequently, n-type c-Si PV cells display superior long-term photostability over p-type cells. According to the International Technology Roadmap for Photovoltaic (Eleventh edition), although the current world market share of the n-type c-Si solar cells is approximately 5% of the c-Si-wafer-based solar cell market, that share is expected to increase to around 50% in 2030.[7] The n-type c-Si PV modules are used widely in PV systems of various kinds including residential and large-scale PV systems.

The application of PV cells in large-scale PV systems requires that one understand the behaviors and mechanisms of their potential-induced degradation (PID).[8–14] This PID of PV modules frequently occurs in large-scale PV systems. Conventional PV modules are generally composed of soda-lime silicate glass as cover glass, ethylene–vinyl acetate copolymer (EVA) as an encapsulant, a backsheet, and an aluminum (Al) frame. Typically in large-scale PV systems, many PV modules are connected in series to build up the voltage output, whereas the module frames are grounded for safety reasons. The voltage is typically 1000 V or higher. Therefore, the active circuit of cells in modules has large positive or negative potentials with respect to the grounded frame. These high electric potentials might cause the degradation known as PID. One particularly important feature of PID is that considerable degradation occurs in a short time in the field, such as several months. Degradation of this kind is therefore regarded as a central reliability issue in large-scale PV systems. An earlier comprehensive review[8] presents more detailed information related to PID. Although the first report of PID in c-Si PV modules is that, in n-type interdigitated back-contact (IBC) c-Si PV modules,[15] many researchers have specifically examined PID in conventional p-type c-Si modules for practical reasons since around 2010.[9–14] Efforts of researchers in the field have contributed to remarkable progress in elucidating PID and related phenomena affecting conventional p-type c-Si PV modules; a brief review is presented in Section 2. Understanding PID in p-type c-Si PV modules will help clarify many aspects PID in n-type c-Si PV modules.

Research undertaken to investigate PID in n-type c-Si PV modules has gradually become active since around 2015. Some reports have described PID in

PV modules fabricated from n-type c-Si cells, such as passivated emitter and rear totally diffused (PERT) cells,[16–30] passivated emitter and rear locally diffused (PERL) cells,[31] TOPCon cells,[32] rear-emitter c-Si PERT cells (with the junction not at the front-glass side),[18, 33, 34] IBC cells,[15, 35–39] and Si heterojunction (SHJ) cells.[40–43] According to these many studies, n-type c-Si PV cell modules show PID with different mechanisms from those in p-type cells. This point has also been reported from some comparative studies.[22, 30, 44] Moreover, results demonstrated that PID of several different types can be observed in n-type c-Si PV cell modules. For instance, n-type front-emitter PERT cells are known to exhibit three types of PID: polarization-type PID; PID because of Na penetration, known as Na-penetration-type PID; and corrosion-type PID.[20] These examples are important because they demonstrate that n-type cell modules can undergo PID of several types occurring by different mechanisms. Also, SHJ cells, which have transparent conductive oxide layers as top surfaces, are reported to be adversely affected mainly by corrosion-type PID and to be resistant to other types of PID. This finding implies that PID behaviors differ depending on the surface structure. The main purpose of this study is to review mechanistic aspects of the three types of PID listed above, which occur in n-type c-Si PV modules.

This paper presents a discussion of PID and related phenomena mainly from the perspective of materials science, with no detailed discussion of accelerated PID test methods, system-level preventive measures, or detection methods. However, understanding generally used PID acceleration tests is also important. Typically, module-level PID acceleration tests are used to examine PID susceptibility and to obtain degraded modules quickly. Module tests are conducted by application of a bias to cells (1) from grounded Al frames of modules flooded with water on their cover glass side,[9] (2) from grounded Al frames in damp heat,[11] or (3) from Al plates placed onto their cover glass in a dry environment.[45] As described herein, the third is designated as the “Al-plate method” or “Al-plate PID test.” It must be borne in mind that the Al-plate method is used in a dry environment. When using this method, the influence of moisture ingress can be discounted from the results. The module-level PID tests described above have been regarded as basic methods to investigate PID phenomena. However, after these PID tests, it is difficult to isolate the degraded solar cells and subject them to analyses because the module components adhere strongly to the cells. To overcome this difficulty, Lausch et al. developed a cell-level PID test that has been used to investigate mechanistic aspects of PID.[46–49] Coring procedures developed by Moutinho et al. can also isolate degraded bare cells from tested modules.[50] These cell-level PID and coring procedures are helpful for investigating mechanistic aspects of PID.

This paper is organized into seven sections. Section 2 briefly reviews PID in conventional p-type c-Si PV cell modules. Understanding PID in conventional p-type c-Si PV cell modules is important for elucidating PID in n-type c-Si PV modules. Three-stage degradation in n-type PERT cell modules is introduced in Section 3, presenting good examples of PID occurring by various mechanisms in n-type c-Si PV modules. Section 4 presents specific examination of polarization-type PID. Actually, PID of this kind is known to occur in a short time and at low voltage. Therefore, it is identified as the most important PID mode in n-type c-Si

cell modules. The degradation behavior and proposed mechanisms of the polarization-type PID are discussed. Subsequently, the respective influences of surface structures, the effect of light illumination, and preventive measures are also reviewed. Section 5 presents an examination of Na-penetration-type PID, which is regarded as caused by Na introduction into c-Si layers. It seems apparent that the junction position in solar cells affects degradation behaviors. Section 6 reviews corrosion-type PID. A PID of this type can appear in SHJ cell modules and in modules from conventional n-type cells with front dielectric layers. A negative bias causes cathodic reductions on cell surfaces, engendering unrecoverable degradation. This, too, is an important degradation mode. Section 7 is a summary of this review paper, presenting the outlook for research in this field.

2. PID Phenomena in Conventional p-type c-Si PV Cell Modules

Modules with aluminum back surface field (Al-BSF) c-Si solar cells or passivated emitter and rear cells (PERCs), which are both categorized as p-type c-Si solar cells, are the most commonly installed types of PV modules. Many p-type c-Si PV modules have already been installed in large-scale PV systems. Their PID has been well documented. Although the main subject of this paper is PID in n-type c-Si PV cell modules, we briefly review shunting-type PID, which has been observed in conventional p-type c-Si PV modules in this section because it is useful to elucidate the PID in conventional p-type c-Si PV modules to understand PID in n-type modules. More details are available in a comprehensive review presented by Luo et al.[8] However, some more recent findings of the shunting-type PID in p-type c-Si PV cell modules are presented in the present review. Recently, Sporleder et al.[51–54] have reported corrosive PID at the rear side of bifacial PERCs. This kind of PID is not explained in the discussion of this section.

2.1. Degradation behavior

Conventional p-type c-Si PV cell modules, which have front n^+ emitters passivated with silicon nitride (SiN_x) films, are adversely affected by shunting-type PID, also designated as PID-s in other reports of literature.[8] The PID in p-type c-Si PV modules are observed at the negative potential end of the strings a short time after installation. In 2010, Pingel et al. and coworkers,[9, 10] and Hacke et al.[11] reported accelerating PID test results for conventional p-type c-Si PV modules. Pingel et al. conducted PID tests by application of a bias voltage to cells from the grounded Al frame of modules flooded with water on their cover glass side. The modules exhibited degradation characterized by a marked decrease in the fill factor (FF) and a slight drop in the V_{oc}.[9] These reductions in parameters are caused by a decrease in shunt resistance (R_{sh}). Hacke et al.[11] conducted PID tests by application of a bias voltage to cells from grounded Al frames in a damp heat test chamber. They also reported degradation behavior identical to that reported by Pingel et al. They concluded that reduction in R_{sh} is related to Na migrating from the module cover glass to cells. In cases of PID stress, leakage current occurs between the cells and the frame. The consequent Na-ion migration is considered a primary source of the leakage current.

Some reports describe that short-circuiting of the pn junction caused by

shunting-type PID is sometimes not just a linear shunting behavior. Taubitz et al.[55] reported that the current density–voltage (J–V) curves of a PID-affected module show markedly high n_2 exceeding 10, where n_2 is the ideality factor of the second diode in the two-diode model.[56] Lausch et al.[46] also reported that PID-affected cells exhibit marked increases in n_2 and J_{02} at local spots, where the J_{02} is the saturation current density of the second diode. Such high n_2 and J_{02} imply multiple defect states in the depletion layer of the pn junction interface.[57] Therefore, these results imply that Na penetration engenders markedly enhanced recombination in the depletion layer.

Reportedly, shunting-type PID behavior depends on the surrounding environment. Hoffmann et al.[58] demonstrated that a leakage current from the frame to cells by Na^+ depends strongly on temperature and humidity. Hacke et al.[59] reported that degradation rates increase with temperature and with humidity. Suzuki et al.[60] examined the sequential effects of a salt-mist treatment followed by high system-voltage stress on performance loss. Their results show that salt-mist spraying accelerates the PID of c-Si PV modules. Koentopp et al.[61] showed that preconditioning with UV light increases degradation rates. However, several studies have clarified that illumination during PID stress slows the degradation rate.[62–65] These findings indicate that sunlight plays an important role in shunting-type PID.

Degradation behavior is also affected by module components such as cover glass[45, 66–71] and encapsulant materials.[66, 71–76] Actually, the cover glass might act as a Na source. Reportedly, shunting-type PID is prevented by quartz glass containing no Na impurities.[66] The use of quartz glass reduces voltages across cell components to a remarkable degree because the glass material has high electrical resistance. Therefore, the possibility exists that PID prevention effects are caused not by the absence of Na impurities but by the high electrical resistance of quartz glass. Naumann established that shunting-type PID occurs in bare cells without cover glass.[77] This finding implies that Na from different sources, such as contaminants on cell surfaces, also cause PID. The encapsulant also affects PID because it separates devices from the cover glass and behaves as a resistor. The influences of the cover glass and the encapsulant on PID are explained in greater detail in Section 2.4. As reported by Xiong et al.,[44] the types and materials of cells affect their degradation behavior.

The chemical compositions of SiN_x passivation films affect PID resistance.[9, 10, 71, 72, 78, 79] Moreover, thin SiO_2 layers formed underneath the SiN_x reduce shunting-type PID.[80–82] Surface morphology also affects PID.[83]

2.2. Degradation mechanism

After Naumann and coworkers[12, 13, 84–87] intensively studied mechanisms that give rise to shunting-type PID, they reported specifically that Na accumulates at the SiN_x/Si interface of c-Si solar cells in PID-affected regions.[84] Moreover, Na is detected in the Si bulk region, which reflects that Na is introduced into absorption layers through the SiN_x layers. This fact suggests that, with the assistance of a strong electric field, Na can pass easily even through SiN_x passivation layers, which are known as diffusion barriers for Na.[88] According to findings reported by Wilson et

al.[89] obtained in an electric field of 0.5 MV/cm and 80 °C, the drift time for Na^+ across an 80-nm SiN_x film is approximately 25 min. These experimentally obtained results confirmed the ease of Na penetration under PID stress.

Bauer et al.[85] and Naumann et al.[86], using time-of-flight secondary ion mass spectrometry (SIMS) and electron-beam-induced current (EBIC) measurements, discovered that both PID shunts and Na accumulation occur locally at the same spots. The positions of EBIC signal disappearance were found to correspond to those of Na accumulation. Both were constrained to local spots. These experimentally obtained results directly link the shunts and Na accumulation. Naumann et al.[12, 13] reported an important result explaining the shunting mechanism in PID. Figure 1 portrays a bright-field transmission electron microscope (TEM) image of a stacking fault that terminates at the surface of a PID-affected c-Si PV cell. Figure 1 also shows energy-dispersive X-ray spectroscopy (EDX) mappings of Na, O, and N around the stacking fault. The EDX mapping for Na shows a strong signal along the stacking fault, indicating that, after PID, stacking faults terminating at the front surface are decorated by Na. The solar research group at NREL, USA, reported similar results.[90, 91] Naumann et al.[87] also reported that no stacking fault occurs before PID stressing and defect nuclei such as dislocations for the growth of Na-decorated stacking faults. Ziebarth et al.[92] conducted density functional theory (DFT) calculations of the segregation energy and diffusion barrier energies of Na at a stacking fault. Results demonstrated that the diffusion barrier energy within the stacking fault is reduced considerably when the stacking fault is fully decorated with Na. Park et al.[93] demonstrated from their DFT calculations that the diffusion barrier of Na within a stacking fault without Na decoration is high and reported that Na does not diffuse within the empty stacking fault. These calculations are consistent with the hypothesis[87] stating that Na does not diffuse within an empty stacking fault, but that it is segregated laterally into a {111} plane while forming a stacking fault. Once Na-decorated stacking faults are formed, additional Na atoms are regarded as diffused within the Na-decorated stacking faults.

Based on these facts, the shunting mechanism can be explained.[13, 87] Figure 2 presents a schematic drawing of a cross-section of a PV module that is undergoing PID. The Na^+ in the cover glass or in contaminants in other components, with the assistance of an electric field between the grounded frames and the cells, migrates toward cells and reaches the SiN_x passivation layer surfaces. There, the Na^+ goes through the SiN_x passivation layers and reaches the SiN_x/Si interface. An electric field promotes this process. Some of the Na accumulating in the SiN_x/Si interface is localized to dislocations and is segregated laterally on {111} planes as Na-decorated stacking faults. The Na-decorated stacking faults produce multiple defect levels within the c-Si bandgap. If the local defect concentration in the stacking faults is considerably high, then the orbitals of neighboring defects overlap. This overlapping allows hopping conduction through the defect levels (“Process 1” in Figure 2). Consequently, the Na-decorated stacking faults penetrating the pn junction might behave as two-dimensional electrically conductive layers, which leads to short-circuiting of the pn junction. At low defect concentrations, one can observe recombination via defect levels of different energies located at the same

place in the depletion region ("process 2" in Figure 2).

2.3. Recovery phenomena

Shunting-type PID is recoverable by application of a positive bias to degraded cells with respect to the frame.[10, 11] In fact, even without a positive bias application, PID-affected cells can be regenerated by storage at a high temperature. For example, Lausch et al.[47] observed that a PID-affected cell recovers its performance loss during heating to 250 °C for 2.5 h. During recovery, Na segregated in stacking faults diffuses out of them. This finding implies that PID recovery phenomena are diffusion-driven processes.[12, 13, 47] Masuda et al.[94] showed that PID-affected cells recover almost completely by storage at room temperature for a long time. This phenomenon requires a considerably longer time, such as 460 days.

2.4. Preventive measures

Researchers have proposed numerous approaches as preventive measures against shunting-type PID.

Glass material is well known to have a strong effect on PID. In fact, PID has been reported as preventable by using quartz glass,[11, 66, 67] borosilicate glass,[68] or chemically strengthened glass.[69] Kajisa et al. reported that a lightweight c-Si PV module with an acrylic front cover sheet does not undergo PID.[70] Hara et al. reported that cover glass with a cell-side surface coated with TiO_2 film reduces PID.[45]

Actually, PID is preventable or reducible using high-electric-resistance encapsulants[66, 71–74] or by inserting ionomer or thin polyethylene films between the EVA encapsulant and the cover glass or cells.[75, 76] Because these measures reduce leakage current effectively, it has been inferred that the high-electric-resistance encapsulants and their thin films can suppress Na^+ migration. Naumann et al.[95] alternatively explains that the effect of preventing high-electric-resistance encapsulants is attributable to reduction in voltage across the SiN_x passivation films and the consequently reduced drift of Na^+ in the SiN_x films.

The preventive measures on a module level presented above are effective. However, substituting other materials for conventional module components can greatly increase material costs. To avoid such an increase in costs, cell-level measures should be used. Additionally, it is preferable to have intrinsically PID-free solar cells that are independent of module manufacturers or installers to apply the right (expensive) materials or correct grounding on the systems. Actually, PID has been shown to be preventable by chemical composition modification of the SiN_x passivation layers on the emitter side of c-Si PV cells[9, 10, 71, 72, 78, 79] because the increased conductivity of the SiN_x layer reduces the voltage across the SiN_x layer. Chemical composition modification is realized merely by changing the ratio of silane (SiH_4) gas flow rate to the ammonia (NH_3) gas flow rate during chemical vapor deposition (CVD). Therefore, this approach can suppress PID effectively without increasing material costs. However, changing the chemical composition from conventional, optimized compositions is undesirable because of increased parasitic absorption, which occurs concurrently with increased conductivity. Mishina et al.[96] demonstrated that high PID resistance can be achieved using SiN_x

layers prepared by high-deposition-rate plasma-enhanced CVD (PECVD) with a hollow cathode. These SiN_x layers have conventional refractive indices (RIs). Actually, this PID prevention effect might be caused by high conductivity that is realized from reduced oxygen content because of the high deposition rate. Thin SiO_2 layers formed underneath the SiN_x also reduce the shunting-type PID.[80–81] Du et al.[82] reported that inserting phosphorous silicate glass layers between the front n^+ emitters and the SiN_x ARC layers can markedly reduce the PID of c-Si solar cells without affecting their efficiency.

3. Degradation in n-type PERT Cell Modules: Examples of Three Degradation Mechanisms

This section presents a description of three-stage degradation[20] as an example in which PID stress leads to several kinds of degradation. The PID of n-type PERT cells includes all the degradation mechanisms reviewed in this paper: polarization-type PID, Na-penetration-type PID, and corrosion-type PID. Additionally, based on results of earlier studies, the last part of this section describes which degradation mechanisms can be expected to appear in the respective n-type cell module types.

Figure 3 shows schematic diagrams of cross-sections of representative n-type c-Si solar cells. Generally speaking, n-type PERT cells have an n-type c-Si base substrate, a p^+ front emitter, and an n^+ back surface field, as shown in Figure 3a. Both sides are coated with passivation/antireflection coating layers. In many cases, the emitter is passivated with a SiN_x/SiO_2 stack or a SiN_x/aluminum oxide (AlO_x) stack. The back surface field is passivated with a SiN_x/SiO_2 stack or single-layered SiN_x film. Described in this section is PID in n-type PERT cells with both p^+ emitter and rear surfaces passivated with SiN_x/SiO_2 stacks. Figure 4 presents $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF_0, and $P_{max}/P_{max,0}$ of the n-type PERT cell modules before and after PID tests in which a bias of −1000 V is applied to cells at 85 °C, where subscript 0 represents the initial value and the P_{max} is the maximum output power. For the experiment, the Al-plate method was used. These test results revealed three stages into which the PID in the n-type front-emitter PERT cell modules are divisible.

First-stage degradation is characterized by reductions in $J_{sc}/J_{sc,0}$ and $V_{oc}/V_{oc,0}$.[16, 17, 19, 20] The PID is known to occur in a remarkably short time. For example, this PID starts to occur within several seconds and begins to saturate within a minute in PID tests with −1000 V at 85 °C.[19] This kind of PID is generally called the "polarization effect" or "polarization-type PID" because the degradation is regarded as resulting from charge accumulation at the interface between the passivation layer and the c-Si. Polarization-type PID details are described in Section 4.

After the polarization-type PID, the modules show second-stage degradation, which is characterized by reduction in FF/FF_0.[18, 20] This PID appears after PID stressing for a longer time than that of the polarization-type PID. Such PID has no particular name, but this PID can be regarded as related to Na penetration. Therefore, this PID is designated herein as "Na-penetration-type PID". The degradation behavior of Na-penetration-type PID depends on the pn junction position. This degradation is reviewed specifically in Section 5.

The modules also show third-stage degradation, which is characterized by reductions in $V_{oc}/V_{oc,0}$ and FF/FF_0.[20, 27] During this degradation stage of n-type

PERT cell modules, the PID caused by Na penetration and corrosion-type PID occur simultaneously. They cannot be distinguished clearly. Ohdaira et al.[27] reported that Na precipitation is observed on the cell. They also reported that corrosion of the SiN_x/SiO_2 passivation layer and of the c-Si surface region are observed underneath the Na precipitate. In SHJ PV modules, corrosion-type PID is the main PID mode.[40–43] It must also be emphasized that corrosion-type PID is a Na-related phenomenon. Section 6 specifically addresses corrosion-type PID.

Based on this example, it turns out that n-type PV cell modules can degrade with multiple and different PID mechanisms. Before presenting an explanation of details related to each PID mechanism, Table I presents some degradation mechanisms appearing in several representative n-type cell modules. Table I shows that Na-penetration-type and corrosion-type PID occur only under a negative bias because both are Na-related degradation modes. By contrast, polarization-type PID can result from both polarities, depending on the cell structure.

4. Polarization-type PID

Polarization-type PID, which is attributable to charge accumulation, was first reported in n-type IBC cell modules in 2005.[15] Polarization-type PID has been observed in many n-type Si PV modules fabricated from PERT cells,[16–29] PERL cells,[31] TOPCon cells,[32] and IBC cells,[15, 35, 37, 38] including IBC cells with front-floating emitters.[36] These cells all involve some dielectric passivation layer(s). Although polarization-type PID is not unique to n-type c-Si cells,[97] it has been observed mainly in n-type c-Si cells.

4.1. Degradation behavior

Polarization-type PID has some unique features which differ from those of other types of PID. Figure 5 presents the current–voltage (I–V) characteristics of n-type PERT cell modules before and after PID testing (Al-plate method). The representative cell structure is shown in Figure 3a. As might be apparent from Figure 5, polarization-type PID reduces J_{sc} and V_{oc}.[15–33, 35–38] Furthermore, FF is unchanged in most cases. This lack of change in FF differs greatly from shunting-type PID observed in conventional p-type c-Si PV modules. Analysis of the J–V characteristics before and after PID tests reveals that J_{01} is increased by polarization-type PID,[20] where J_{01} is the saturation current density of the first diode in a two-diode model. An increase in J_{01} generally results from increased diffusion currents of solar cells. In many cases, polarization-type PID does not change other parameters. After polarization-type PID, external quantum efficiency (EQE) is reportedly reduced in a short-wavelength range (mainly at 300–600 nm).[16–20, 22, 23, 31] These results indicate that degradation occurs mainly because of enhancement of the interface recombination at the front surface of c-Si. Nishikawa et al. observed interface recombination enhancements as changes in the effective minority-carrier lifetime (τ_{eff}).[98] As Section 4.2 shows, polarization-type PID is identified as a consequence of undesirable charge accumulation at antireflection and passivation layers.

Polarization-type PID occurs at a low voltage bias or at a low temperature. Hara et al.[16] showed that in the Al-plate method, PID can occur at a very low bias of

−50 V at 85 °C. This feature of polarization-type PID is unique. To date, no report has described that PID occurs by such a low bias condition except for polarization-type PID. This lack of a definitive result implies that cells which are prone to polarization-type PID can degrade not only in large-scale PV systems but also in small-scale systems such as rooftop PV systems or in systems with module-level power electronics. The n-type PERT cell modules degrade also at room temperature (Figure 5).[16] Luo et al. showed that even when a voltage is applied between the rear (n) side of n-type PERT cells and the cover glass surface on the n side, significant degradation occurs at the front (p) side. In this case, the electric field on the p side is weaker. These facts also demonstrate the ease of occurrence of polarization-type PID.

The rate of polarization-type PID is faster than that of other types of PID. Reportedly, in an Al-plate method with negative bias of −1000 V at 85 °C, n-type front-emitter PERT cell modules start to degrade within 5 s. The degradation saturates within 1–2 min,[17, 19] as presented in Figure 6. This rapid degradation and subsequent saturation are behaviors that are unique to polarization-type PID. In actuality, the saturation value is independent of the magnitude of the applied bias (Figure 7).[17, 19]

This PID can occur under both polarities depending on the type of dopant in layers underneath the passivation layers. For instance, cells with passivated p-type layers show polarization-type PID under a negative bias. Cells with passivated n-type layers show polarization-type PID under a positive bias. Actually, standard n-type IBC cells (Figure 3b) show degradation under positive bias.[15, 37–38] By contrast, n-type IBC cells with p-type front-floating emitters show degradation under a negative bias.[36] This feature contrasts with those of shunting-type PID, Na-penetration-type PID, and corrosion-type PID, which reportedly take place only under negative bias conditions.

Polarization-type PID has been reported to be recovered easily by application of opposite bias to the bias causing degradation.[15–20, 98] For example, n-type front-emitter PERT cells that have been degraded under a negative bias are recoverable by application of a positive bias. Luo et al. reported that polarization-type PID in n-type PERL cells with SiN_x/AlO_x passivation stacks can be recovered quickly by illumination.[31] This point is also presented in Section 4.4.

4.2. Proposed mechanisms

Polarization-type PID is identified as a consequence of charge accumulation in (front) antireflection/passivation layers. Swanson et al.[15] proposed that accumulated charges resulting from leakage currents flowing between the frame and cells attract minority carriers to the interface between the passivation film and the c-Si. Thereby, interface recombination of minority carriers via interface defect states is enhanced. Other researchers have reported experimentally obtained results that support the mechanism.[16, 17, 19, 22] Bae et al.[22] confirmed experimentally that the positive charge density in the front SiN_x/SiO_2 is increased by application of a negative bias. The proposed mechanism is now widely accepted.

Some reports of the literature have proposed K centers in SiN_x as the origin of accumulated charge.[17, 19] These K centers, which are dangling bonds of Si atoms

backbonded to three nitrogen atoms in SiN_x layers,[99–101] have three charge states: neutral, positively charged, and negatively charged. These K centers, according to their three charge states, are designated respectively as K^0, K^+, and K^-. The charge state is known to be manipulated by an externally applied bias.[102, 103] Typical SiN_x layers fabricated by PECVD for c-Si solar cells have K centers with areal density of approximately 10^{12} cm^{-2}.[102, 103] It has been proposed that K centers are sources of additional charges in SiN_x layers in polarization-type PID.[17, 19] Hereinafter, this model is designated as the "K-center model." Figure 8 presents a schematic diagram of the K-center model for polarization-type PID in an n-type front-emitter PERT cell module. The figure portrays cross-sectional pictures near the front surface of the n-type front-emitter PERT cell in the module undergoing polarization-type PID. The c-Si top surface is the p-type emitter. Before biasing, K centers are present in the front SiN_x passivation layers (Figure 8a). During the negative bias application, positive charges are created or are transferred onto the SiN_x surface. As a result, positive charges accumulate on the surface (Figure 8b). These positive charges extract electrons from K^0 and K^- centers and leave the K^+ centers in the SiN_x (Figure 8c). These K^+ centers shift the net charge of the SiN_x toward positive. Thereby, minority carriers, holes, are attracted to the SiN_x/c-Si interface. Interface recombination via interface defect states is enhanced there.

The model presented above is also applicable to SiN_x-passivated n-type surfaces, such as those n-type IBC solar cells (Figure 3b), because K centers can also be charged negatively. For passivated n-type surfaces, the terms "negative bias," "positive charges," "K^+ centers," "electrons," and "holes" can be replaced respectively with "positive bias," "negative charges," "K^- centers," "holes," and "electrons" because PID occurs on p-type and on n-type surfaces under opposite biases.

The K-center model explains the experimentally obtained results well. The positive charge density is limited by the K-center density, which explains the saturation behavior (Figure 6) and the applied bias dependence (Figure 7). Saturation is assumed to occur when all the K centers are positively charged. From Al-plate PID tests, it has been shown that a sufficient number of positive charges for complete charging of all K centers is supplied within a very short time, such as 1–2 min at −1000 V and 85 °C. This finding is consistent with remarkable rapid degradation.[17, 19] The K-center density was confirmed to be similar to the density of positive charges after the saturation of degradation.[19]

4.3. Influences of surface structure

Polarization-type PID results from charge accumulation in surface dielectric layers. Therefore, the PID degradation behavior is sensitive to surface structures, including passivation and antireflection stacks and the doping concentration of the passivated surface. This section presents a description of how the surface structure affects the polarization-type PID. Some findings are useful to formulate degradation countermeasures and to elucidate some effects related to illumination during PID stress. The influences of illumination are addressed in the following section, with prescribed preventive measures explained in section 4.5.

Surface passivation films affect the degradation behavior. For n-type PERT cells

with SiN_x/SiO_2 passivation stacks, SiO_2 films are proposed to play an important role in the charge accumulation process.[17, 19] The SiO_2 films were expected to help SiN_x films retain their additional charges injected by an applied bias.[17, 19] This hypothesis was confirmed in n-type PERT cells[21] and also in p-type conventional c-Si cells.[97] These facts demonstrate that the respective properties of thin films on SiN_x films and c-Si surfaces are crucially important in polarization-type PID. Therefore, the possibility exists that passivation films of other kinds, such as SiN_x/AlO_x passivation stacks, which are widely applied to p-type c-Si surfaces, are also involved in PID degradation behavior.

Luo et al. showed that polarization-type PID in n-type c-Si cells with front p^+ emitter passivated with SiN_x/AlO_x is recoverable by illumination.[32] Additionally, polarization-type PID on the SiN_x/AlO_x-passivated rear of p-type PERC solar cells reportedly does not occur under illumination; even when PID occurs during PID tests in the dark, the degradation is recoverable by illumination used after the degradation. This result is not a phenomenon occurring in n-type c-Si cells. This example is important for elucidating illumination effects on polarization-type PID behavior. However, n-type PERT cells with SiN_x/SiO_2 passivation stacks are reportedly insensitive to illumination.[24] These studies demonstrate that effects of illumination on polarization-type PID depend strongly on the surface passivation structure. This strong dependence is reviewed in greater detail in Section 4.4.

Janssen et al.[26] demonstrated that stacked SiN_x films composed of 60-nm-thick SiN_x with RI of 2.0 and 20-nm-thick SiN_x with RI of 2.4, on the c-Si p-type emitter surface, minimize polarization-type PID. This minimization is regarded as occurring as a result of the dissipation of accumulated charges by carrier transport between the high-RI interlayers and emitters to validate the PID-preventive measure proposed by Janssen et al. Yamaguchi et al.[29] implied that it is necessary to use sufficiently thin SiO_2 films between the high RI SiNx film and the emitter because carrier transport between the high-RI interlayers and the emitters is prevented by thick SiO_2. These are of practical importance to develop preventive measures against polarization-type PID. Related details are explained in Section 4.5. Yamaguchi et al.[29] also shows that high emitter-surface doping concentrations moderately reduce PID effects. This reduction further implies that solar cells with low surface-doping concentrations can be expected to be sensitive to polarization-type PID. Solar cells with selective emitters and IBC solar cells with no front-surface doped layers are expected to be sensitive to polarization-type PID. An additional nitridation step applied before SiN_x layer deposition can reduce the PID effect effectively when used together with a high emitter-surface doping concentration.[29] However, the nitridation step alone provides no marked effect on polarization-type PID.[29]

Hara et al.[104] confirmed that SHJ PV cells with front transparent conductive oxide layers show no polarization-type PID. Luo et al.[32] showed that the TOPCon structure composed of SiN_x/n^+-doped polycrystalline Si (poly-Si) layer/SiO_2 (Figure 3c) exhibits no polarization-type PID. The front sides of these TOPCon solar cells were passivated with SiN_x/AlO_x, showing polarization-type PID.

4.4. Influence of illumination

In the actual field, the exposure to high potential, and thus PID, occurs only under (natural) illumination. Therefore, it is crucially important to elucidate the effects of illumination on degradation behavior. A few reports of some earlier studies have described some important hints on illumination effects to date. These findings are summarized in this section.

Luo et al.[24] reported that PID in n-PERT cells with SiN_x/SiO_2 passivation stacks is insensitive to illumination, as presented in Figure 9. In this PID test, transparent conductive gel was substituted for a metal plate. Yamaguchi et al.[105] also reported that the polarization-type PID behavior remains unchanged irrespective of the presence or absence of illumination. Luo et al.[32] demonstrated that polarization-type PID in n-type cells with a front p^+ emitter passivated with SiN_x/AlO_x is recoverable by natural illumination (Figure 10). As shown in Figure 10, degraded modules with a normalized P_{mpp}, i.e. $P_{max}/P_{max,0}$, of approximately 80% were regenerated almost completely by 5-h exposure to sunlight. Additionally, polarization-type PID on the SiN_x/AlO_x rear side of p-type PERCs is also reported not to occur under illumination with a low intensity of 0.01 sun. This is not a phenomenon occurring in n-type c-Si cells, but it is an important example elucidating the effects of illumination on polarization-type PID behavior. These findings demonstrate that effects of illumination on polarization-type PID depend on the passivation structure.

The root causes of the illumination effect on polarization-type PID must be discussed next. Luo et al. speculated that solar cell sensitivity to polarization-type PID is related to the passivation/antireflection structure. We derive a plausible hypothesis from results of studies of the effect of illumination on shunting-type PID[62–65] and from cell-level preventive measures against polarization-type PID.[26, 29] In shunting-type PID, the delay of PID in the presence of illumination is explained as follows. Illumination increases the conductivity of the front SiN_x layers. This increased conductivity consequently reduces the voltage across the SiN_x layers and thereby reduces the drift of Na^+ ions, which results in the delay of the shunting-type PID. On the other hand, polarization-type PID can be prevented effectively using high-RI SiN_x layers[26] together with sufficiently thin thermal or chemical SiO_2 films. It is noteworthy that the SiO_2 films must be sufficiently thin because the SiO_2 is expected to permit tunneling to dissipate the accumulated charges by charge transfer between the high-RI SiN_x layers and the emitters. In other words, the electric insulation property must be sufficiently low. By combining these findings, the hypothesis of the effect of illumination of polarization-type PID is proposed as explained below. Under PID stress, additional charges are accumulated in the solar cell SiN_x layer. When the cell is illuminated, the SiN_x layer conductivity increases. If the electrical resistance of the (SiO_x or AlO_x) layer underneath the SiN_x layer is sufficiently low, then the accumulated charges will dissipate via carrier transport between the SiN_x layer and the c-Si. In this case, the cell shows no degradation under illumination. Alternatively, the degradation is recovered by illumination. However, if the resistance is high, then the accumulated charges are retained. Also, (stable) polarization-type PID is observed.

The hypothesis presented above can explain the reported illumination

sensitivity of polarization-type PID. The polarization-type PID of many n-type PERT cells with SiN_x/SiO_2 stacks are insensitive to illumination because these have thick SiO_2 passivation films (approximately 10 nm). By contrast, the PID of cells with SiN_x/AlO_x stacks are sensitive to illumination because AlO_x films have considerably lower insulation properties than thick SiO_2 films. From this hypothesis, it is expected that cells with very thin SiO_2 with thickness of 1 nm show no polarization-type PID under illumination, and that the degradation is recoverable by illumination. The hypothesis must be verified by additional experimentation.

4.5. Preventive measures

Developing preventive measures against polarization-type PID is important. This section presents a review of the proposed module-level and cell-level preventive measures. System-level measures might also be effective for preventing polarization-type PID. Nevertheless, these system-level preventive measures are not addressed herein.

Many module-level measures have been proposed to prevent shunting-type PID in conventional p-type c-Si PV cell modules. These measures are based on alternative glass or encapsulants. Some researchers have attempted to apply these measures to n-type c-Si modules to prevent polarization-type PID. Moreover, some different results have been reported for systems including other cells than p-type c-Si cells. Chemically strengthened glass reduces shunting-type PID effectively.[69] Hara et al.[16] applied chemically strengthened glass to modules with n-type PERT cells. However, in that case, polarization-type PID effects were not reduced at all. Luo et al.[23] reported that PID-resistant EVA and polyolefin encapsulants, both typically having higher resistance or a lower water vapor transmission rate, are slow but do not prevent polarization-type PID. These measures developed for conventional p-type c-Si cell modules are ineffective for modules with n-type c-Si PV cells. Ionomer encapsulants[16] and Na-free glass[23] were confirmed as effective for preventing shunting-type and polarization-type PID. However, these module-level measures are undesirable in terms of cost. Eventually, cell-level measures are necessary to avoid an increase in the module cost.

As described briefly earlier, Janssen et al.[26] proposed a preventive measure that provides an excellent anti-PID property and cost-effectiveness. They showed that stacked SiN_x films composed of a 60-nm-thick SiN_x top layer with RI of 2.0 and a 20-nm-thick SiN_x bottom layer with RI of 2.4 minimize the polarization-type PID, as shown in Figure 11. This minimization results from the dissipation of accumulated charges by carrier transport between the high-RI interlayers and the emitters.[29] This measure not only offers an excellent anti-PID property. It also does not increase the production cost because the measure can be achieved merely by modifying the ratio of silane to ammonia. Additionally, this measure sometimes even improves the initial cell performance because of better antireflection and passivation properties. This measure should be used together with very thin SiO_2 passivation films.[29] When SiN_x films are used for passivation of p-type surfaces in industrial cells, SiO_2 passivation films underneath the SiN_x are used in many cases. If the SiO_2 films are thick and prevent carrier transport between the high-RI interlayers and the emitters, then the measure is regarded as invalid. Therefore, the

SiO_2 should be sufficiently thin. To realize such very thin SiO_2 films with excellent passivation properties, one can use the nitric acid oxidation of the Si technique.[106] If AlO_x films are applied underneath the high-RI SiN_x interlayers, then the allowed thickness might be greater because of the lower insulation property of AlO_x.

Another possible cell-level measure was proposed for n-type PERT cells.[29] This measure is achieved by a combination of etching of the surface boron depletion layer and additional nitridation step before SiN_x deposition. The former engenders a high surface doping concentration, which makes the surface more insensitive to an electric field resulting from accumulated charges in the SiN_x layer. Additionally, etching of the surface boron depletion layer might improve the initial cell performance slightly because of the reduced surface recombination.[29] The additional nitridation step is a plasma treatment process that causes atomically distorted interfaces.[107, 108] Atomic-scale Si-rich thin layers are known to be formed in the immediate vicinity of the distorted interface, which might cause a higher electric conductivity. This combination can be shown to reduce polarization-type PID effectively.[29] However, a shortcoming exists by which cell production costs are expected to be increased by these additional cell processing steps. Therefore, the cost-effectiveness of this measure is inferior to that of measures based on high-RI interlayers.

5. Na-penetration-type PID

Conventional p-type c-Si PV cell modules exhibit shunting-type PID, which results from Na penetration. Furthermore, in n-type c-Si cells of some kinds, researchers have observed PID that can be regarded as resulting from Na penetration. No particular name exists for such PID. As described in this review, such degradation is designated as Na-penetration-type PID as a matter of convenience. The cause of PID is Na introduced from PV module components through the passivation layers and/or unpassivated edges of solar cells. Therefore, such PID occurs only under negative bias. As already described in Section 3, n-type PERT cells show Na-penetration-type PID. Moreover, rear-emitter and IBC n-type c-Si cells and SHJ cells have been reported to be adversely affected by this type of PID. Unlike the case of polarization-type PID, power losses by Na-penetration-type PID depend on the cell structures. More concretely, the degradation behavior depends on whether the PID-affected side is on the pn-junction side or not.

In this section, Na-penetration-type PID behaviors in each type of cell are described separately. Actually, Na-penetration-type PID has not been investigated sufficiently to date, but this PID degradation mechanism resembles that of shunting-type PID. Therefore, many findings can be obtained analogously by comparing Na-penetration-type PID to shunting-type PID.

5.1. Front-emitter n-type PERT cell

Komatsu et al.[20] reported that, after the first degradation, which corresponds to polarization-type PID, n-type PERT cells (Figure 3a) undergo Na-penetration-type PID. They assumed that the degradation results from Na penetration into the c-Si substrate. Actually, in dynamic SIMS (D-SIMS) measurements of PID-affected cells, Na was detected in the c-Si substrate region.[27] This Na is also apparent in a

D-SIMS profile for Na in Figure 12. In fact, Na^+ ions are known to be introduced into the c-Si substrate from the cell surface through SiN_x passivation layers by PID stress.[84, 89]

The Na-penetration-type PID in n-type front-emitter PERT cells is characterized mainly by reduction in the FF. This reduction is similar to nonlinear shunting behavior. In Figure 4, the second-stage degradation corresponds to the Na-penetration-type PID. The degradation is accompanied by a markedly increased J_{02} and $n_2 > 2$, in the two-diode model. Such a high n_2 implies a strongly enhanced recombination in the depletion region of the pn junction via multiple defect states.[57] The front-emitter n-type PERT cells have the pn junction on the PID-affected side. Therefore, the Na atom density at the pn junction interface can be high. The Na impurities are known as a "lifetime killer". These Na atoms at the pn junction interface are assumed to produce defect states and to enhance the depletion-region recombination.[109] This enhancement might cause the reported nonlinear shunting, which might be related to formation of the Na-decorated stacking faults observed in PID-affected conventional p-type c-Si PV cell modules. However, no detailed analysis of that point has been undertaken to date. Whether Na-decorated stacking faults are formed or not should be investigated.

This PID is recovered almost completely by application of a reverse, positive bias.[20] By comparison with PID in conventional p-type c-Si PV cell modules, the Na-penetration-type PID in n-type PERT cells is expected to be recoverable by storage at an elevated temperature or by being stored at room temperature for a long time. However, Na-penetration-type PID recovery has not yet been investigated sufficiently.

Measures for preventing this PID have not been studied sufficiently. However, because the degradation mechanisms are similar for shunting-type PID in p-type c-Si PV cell modules, many module-level and cell-level preventive measures for the p-type c-Si PV cell modules described in Section 2.4 are probably also effective. An earlier study indicated that n-type PERT cell modules with an ionomer encapsulant undergo no degradation, even after PID tests with −1000 V at 85 °C for two weeks.[16] This finding implies that the Na-penetration-type PID is preventable using the ionomer encapsulant.

5.2. IBC and rear-emitter n-type c-Si cell modules

IBC n-type c-Si cells[35, 39] and rear-emitter n-type c-Si PV cells[33] also reportedly undergo Na-penetration-type PID. The former is shown in Figure 3b, and the latter is designated as a flipped structure of n-type PERT cells shown in Figure 3a. Unlike the front-emitter PERT cells, these cells exhibit Na-penetration-type PID characterized mainly by reductions in J_{sc} and V_{oc} because neither cell type has any pn junction on the affected front side. The Na atoms introduced into the front surface region of these cells are not near the pn junction. They merely behave as recombination centers. Nishikawa et al.[98] confirmed that n-type substrates passivated with SiN_x films show decreased τ_{eff} after negative-bias application. The EQE in a short-wavelength range is confirmed to be reduced after PID.[33, 39] Additionally, the J_{01}s of IBC n-type c-Si cells and rear-emitter n-type c-Si PV cells are confirmed to be increased after Na-penetration-type PID.[33, 39] This increase

also indicates increased diffusion current via defect states originating from Na introduced in the surface region of the c-Si wafer. One model has been proposed based on the formation of Na-decorated stacking faults.[34] Figure 13 shows a model in which bulk recombination in the surface region of c-Si is enhanced by Na-decorated stacking faults formed by PID stress. However, no detailed analysis has yet been performed.

The resistance of these cells to Na-penetration-type PID is also expected to be improved by the same preventive measures as those used for shunting-type PID because the mechanism of this PID resembles that of shunting-type PID.

Na-penetration-type PID in IBC n-type c-Si cell modules is reportedly reduced under illumination.[39] Figure 14 shows effects of illumination on Na-penetration-type PID occurring in n-type IBC c-Si PV cell modules. The result reveals that the illumination delays Na-penetration-type PID in n-type c-Si solar cells. The origin of this effect is explained to be increased conductivity of the front SiN_x passivation layers. The increased conductivity causes a reduction in voltage applied across the SiN_x passivation layers. This reduced voltage in turn reduces the drift of Na^+ in the SiN_x layers, leading to reduced degradation. This proposed mechanism is similar to that of shunting-type PID under illumination.

5.3. SHJ cell modules

PV Modules fabricated from SHJ cells (Figure 3d) also show Na-penetration-type PID.[41, 43] However, Na-penetration-type PID might not be the main PID mode in SHJ cells because they require a long time and high voltage to generate Na-penetration-type PID in SHJ PV cells. In this case, Na should be introduced into the surface region of the c-Si wafer. However, SHJ cells have transparent conductive oxide (TCO) layers, e.g. In_2O_3-based, on both sides. Actually, Na cannot pass easily through these TCO layers. One way might be that Na drifts through pores in damaged TCO layers after corrosion-type PID. As described in Section 6.2, the main PID mode in SHJ cells is corrosion-type PID. Because Na-penetration-type PID in SHJ cells is an example illustrating that the emitter position impacts the behavior, we briefly introduce the results in this section. The information presented herein was obtained from acceleration tests on SHJ cell modules encapsulated with module materials for more conventional p-type and n-type solar cells, such as tempered cover glass and EVA encapsulant layers. Excellent stability of commercial SHJ cell modules has been demonstrated.[44, 104, 110, 111]

Front-emitter SHJ PV cell modules show Na-penetration-type PID, which is characterized by a reduction in the FF.[43] This degradation behavior resembles that of front-emitter n-type PERT cells. However, rear-emitter SHJ cells show Na-penetration-type PID, which is characterized by reduced V_{oc} and J_{sc}.[41, 43] This behavior resembles that of IBC and rear-emitter n-type cells. Considered together, these results demonstrate that the emitter position affects the Na-penetration-type PID behavior.

The SHJ PV cell modules only exhibit Na-penetration-type PID under severe PID conditions (Al-plate method) involving very high voltage of −2000 V over several tens of days.[41] Actual PV systems are typically limited both by technology and by regulations to 1000 or 1500 V. For that reason, Na-penetration-type PID is

not regarded as easily occurring in actual PV systems. However, Masuda et al.[42] demonstrated that the PID in SHJ cell modules is accelerated considerably by moisture ingress. That SHJ cells with damaged TCO layers are more susceptible to Na-penetration-type PID is also possible. Moisture ingress should be prevented by using encapsulants and backsheets with sufficiently low moisture permeability to ensure high reliability of SHJ cell modules. The use of ionomer encapsulants affords excellent stability against Na-penetration-type PID.[40, 41]

6. Corrosion-type PID

Corrosion-type PID has been observed in p-type c-Si cell modules and in thin-film PV modules. Hacke et al.[11] reported that the dissolution of SiN_x antireflection/passivation films and the degradation of metallization are caused PID stress. Sporleder et al.[51–54] investigated corrosion-type PID on the rear side of p-type bifacial PERC solar cells. The corrosion of TCO layers and related degradation in thin-film PV modules under bias application are well-known phenomena.[112–115] These reported findings demonstrate that cathodic corrosion under a negative-bias application can adversely affect PV cells.

Also in n-type c-Si-based solar cells, negative biases engender cathodic corrosion of cell materials. Reportedly n-type PERT cells[27] and SHJ cells[40, 41] undergo corrosion-type PID under a negative bias. Here, we summarized these reported results and findings.

6.1. n-type PERT cell modules

After Al-plate PID tests in which a negative bias of −1000 V was applied for 20 days, n-type front-emitter PERT cells (Figure 3a) showed significant reduction in the V_{oc} and FF.[20] Ohdaira et al.[27] analyzed such degraded cells using secondary electron microscopy (SEM) and EDX. Results of these analyses are presented in Figure 15. These findings demonstrate that micrometer-sized Na precipitates are formed on solar cells. They erode the c-Si substrate as well as the passivation/antireflection layer. The Na-based precipitates destroy surface passivation and the pn junction, which reduces V_{oc} and FF considerably. This PID is only barely recovered by application of a positive bias. If rear-emitter and IBC cells would also be shown to exhibit corrosion-type PID, then the degradation could probably be characterized by reductions in J_{sc} and V_{oc}.

The mechanism of the formation of the Na-based precipitates remains unclear. The formation might be related to some sort of chemical reduction reaction. An earlier study[27] applied PID tests at relative humidity of <2%. The study required a long time to cause degradation. However, the degradation can be accelerated greatly under the presence of moisture. Much additional work must be conducted to verify this point.

6.2. SHJ PV modules

According to some reports,[44, 104, 110, 111] commercial SHJ PV cell (Figure 3d) modules have excellent tolerance against PID. Therefore, PID in SHJ cell modules is not identified as a severe reliability issue at present. However, this does not mean that research investigating PID in SHJ cell modules is unnecessary. SHJ cell

modules with traditional module encapsulation materials are adversely affected by corrosion-type PID,[40, 41] which implies that the noteworthy high PID tolerance of commercial SHJ cell modules is attributable to the use of anti-PID encapsulation materials. Continued investigation of PID in SHJ PV modules has contributed to the development of low-cost cell-level preventive measures. Such measures might enable us to achieve highly reliable SHJ cell modules with low-cost module encapsulation materials. This section specifically describes the current status of research on corrosion-type PID in SHJ PV cell modules.

Modules fabricated from SHJ PV cells with tungsten-doped In_2O_3 (IWO) films on both sides show reduction in J_{sc} under negative bias application.[40, 41] Figure 16 presents the 1-sun and dark *J–V* characteristics of the SHJ PV modules before and after Al-plate PID exposure in which a negative bias of −1000 V was applied at 85°C in a dry environment. Although J_{sc} decreases gradually with exposure time, the dark *J–V* characteristics remain unchanged, revealing that the J_{sc} loss is not caused by recombination losses but by an increase in optical losses. This degradation can not be recovered by application of a positive bias, as in the case of n-type PERT cells described above.

By X-ray absorption fine structure spectrometry, results showed that the increase in optical losses is attributable to absorption in the front IWO layers caused by the precipitation of metallic In.[41] Figure 17 shows In K-edge and W L_3-edge X-ray absorption near-edge structure (XANES) spectra obtained from the front IWO film of a degraded SHJ PV cell. The XANES spectra were analyzed by fitting the XANES spectra using the data extracted from a pristine IWO film and from the standard In and W samples. From the In K-edge spectrum, In_2O_3 is confirmed to be reduced considerably to metallic In by PID stress. However, the chemical state of the W atoms is unaffected by PID stress. The same findings were derived from the analysis of X-ray absorption fine structure spectra.[41] These results indicate that In_2O_3 in In_2O_3-based TCO is chemically reduced. Metallic In is precipitated within the TCO. The metallic In precipitates absorb some of the incident light and thereby reduce J_{sc}. These In precipitates are formed in chemical reduction reactions. Additionally, numerous Na impurities exist on the degraded cell surface.[41] The mechanism of the chemical reduction of In_2O_3 TCO is now under discussion. Based on the findings presented above, a mechanism is proposed as[40, 41]

$$Na^+ + e^- \rightarrow Na, \quad (1)$$

$$H_2O + Na \rightarrow NaOH + H, \quad (2)$$

$$In_2O_3 + 6H \rightarrow 2In + 3H_2O. \quad (3)$$

As, based on this mechanism, H_2O participates in the chemical reaction (2), moisture has a strong effect on this corrosion-type PID. Masuda et al.[42] reported that moisture accelerates the corrosion-type PID in SHJ PV modules to a marked degree. The above corrosion-type PID is expected to occur in cells of other types that involve In_2O_3 TCO layers, for example, carrier-selective contact cells.

The corrosion-type PID can be prevented completely using ionomer encapsulant.[40, 41] However, this measure is undesirable because alternative module encapsulation materials are expensive in many cases. Therefore cell-level low-cost preventive measures should be developed to reduce the module production cost. The findings presented above are expected to be useful for developing such

preventive measures.

Here, possible cell-level measures to prevent the corrosion-type PID in SHJ cell modules are discussed. One is the application of SiO_x barrier films to prevent moisture and Na ingress. Based on the proposed mechanism, moisture and Na are the triggers of corrosion. Therefore, moisture-barrier and Na-barrier SiO_x films might reduce the PID effectively. Such SiO_x barrier films improve cells' resistances to damp-heat and PID stress by reducing the ingress of both moisture and Na into the layer below the barrier films.[116] Another approach is the use of alternative TCO materials. The development of highly stable and low-cost TCO materials with sufficiently high conductivity persists as a challenging issue.

7. Conclusions and Outlook

PV modules fabricated from high-efficiency n-type c-Si cells attract attention because of their potential for achieving higher efficiencies than those of p-type cells. The share of n-type c-Si cells is expected to increase continuously. Research investigating their reliability and degradation becomes increasingly important. As an important degradation mode, PID in n-type c-Si PV modules has been investigated actively in recent several years. As described in this paper, we have reviewed important findings obtained from assessment of PID in n-type c-Si PV cell modules.

Depending on their cell structures, n-type c-Si PV modules can be affected by PID of three kinds: polarization-type PID, Na-penetration-type PID, and corrosion-type PID. Some n-type PERT cells are known to show all three PID modes. Particularly, polarization-type PID is identified as a severe degradation mode because large degradation appears quickly, even under mild conditions. Therefore, we explained polarization-type PID comprehensively.

Actually, n-type Si PV cells of many types, such as PERT cells, PERL cells, TOPCon cells, and IBC cells, show polarization-type PID. These solar cells all involve dielectric SiN_x antireflection/passivation layers. Polarization-type PID occurs very easily under mild PID conditions, which implies that degradation occurs not only in large-scale PV systems but also in low-voltage systems such as systems with power optimizers or micro-inverters. Polarization-type PID results from charge accumulation in the SiN_x layers. Polarization-type PID can be fully recovered simply by application of a reverse bias. For a proposed mechanism called the K-center model, the charge accumulation process is explained as charge trapping or detrapping at K centers by an electric field. Polarization-type PID in cells passivated with SiN_x/SiO_2 is not sensitive to illumination. However, PID in cells with SiN_x/AlO_x stacks have been reported as reduced by illumination. The PID is preventable by application of a fairly thin high-RI SiN_x interlayer between the emitter and the bulk SiNx layer. This measure not only produces an excellent anti-PID property; it also does not increase production costs. Nevertheless, attention must be devoted to properties of films underneath the high-RI SiN_x interlayer to validate the preventive measures. Some module-level preventive measures have also been described.

Reports have described Na-penetration-type PID occurring in front-emitter and rear-emitter PERT cells, IBC cells, and SHJ cells. The behavior of this degradation

differs depending on whether the pn junction is located on the PID-affected side or not. When the pn junction is absent on the PID-affected side, the degradation is characterized by reductions in J_{sc} and V_{oc}. However, the FF is markedly lower when the pn junction is on the Na-penetration-type PID-affected side. Influence of the pn junction position was shown clearly in bifacial SHJ cells. In IBC cells, the Na-penetration-type PID is delayed by illumination. Additionally, we addressed the possibility that typical module-level preventive measures are effective for this degradation type.

Also, corrosion-type PID in modules with n-type PERT cells have been reviewed herein. In these n-type PERT cells, Na-based precipitates are formed on the cell surface, which damages the SiN_x antireflection/passivation layers and which erodes the c-Si surface region. This destructive degradation cannot be recovered by a reverse-bias application. Modules with SHJ PV cells show corrosion-type PID that is characterized by reduction of J_{sc} under a negative-bias application. This degradation, which is unrecoverable, results from increased absorption of the IWO layers caused by the chemical reduction of In_2O_3 in the IWO layers. Corrosion-type PID in SHJ PV modules was shown to be accelerated considerably under the presence of moisture. This degradation can be prevented easily using high-electric-resistance encapsulants such as ionomer. However, this measure increases the material cost.

Many open questions and other issues remain in PID in n-type c-Si cell modules. We propose the following open research questions that must be answered in the next few years:

(1) For polarization-type PID, further verification experiments for the K-center model should be conducted. Additionally, the mechanism of the dependence of the passivation structure on the illumination must be clarified. The influence of illumination is one of the most important open questions to be investigated.

(2) For Na-penetration-type PID, open questions remain about details of degradation mechanisms, the influence of illumination, and the influence of humidity. Cell-level, low-cost preventive measures against Na-penetration-type PID should be developed. One must confirm that the cell-level measure developed for shunting-type PID that are based on the high-RI SiN_x antireflection/passivation films can also be effective against Na-penetration-type PID in n-type cells.

(3) For corrosion-type PID, details of degradation mechanisms are under discussion. Effects of illumination, temperature, and humidity on degradation are still understood only incompletely. To prevent increased module material costs, cell-level low-cost measures must be developed to prevent corrosion-type PID.

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Figure captions

Figure 1. On the left is a bright-field TEM image of a Na-decorated stacking fault formed by PID stress. Small images on the right represent EDX mappings acquired in scanning TEM mode at the stacking fault near the interface between Si and SiN_x. A Na-EDX map of the lower part of the stacking fault is shown in the inset on the left. Reproduced with permission.[13] Copyright 2013, Elsevier B.V.

Figure 2. Schematic drawing of a cross-section of a conventional p-type c-Si cell undergoing shunting-type PID. Current flows across a Na-decorated stacking fault are shown at high-level concentration (process 1, black) and at a low local level concentration (process 2, gray). Reproduced with permission.[13] Copyright 2013, Elsevier B.V.

Figure 3. Schematic diagrams of cross-sections of representative (a) n-type front-emitter PERT, (b) n-type IBC cells, (c) n-type bifacial TOPCon cells, and (d) n-type rear-emitter SHJ cells (not to scale). In Panel (d), a-Si is an abbreviation for amorphous Si.

Figure 4. $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF_0, and $P_{max}/P_{max,0}$ of the n-type front-emitter PERT cell modules before and after PID tests where a negative bias of −1000 V is applied to cells at 85 °C in a dry environment. The Al-plate method was used as a PID acceleration test. Data points represent the mean values of three identical modules. Error bars correspond to the standard deviation of the mean. Data extracted from reference. [20]

Figure 5. *I–V* curves of n-type front-emitter PERT cell modules before and after an Al-plate PID test for 2 h: before, −1000 V at 25 °C, −50 V at 85 °C, and −1000 V at 85 °C. Data extracted from reference.[16]

Figure 6. Dependences of $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF_0, and $P_{max}/P_{max,0}$ of n-type front-emitter PERT cell modules on the duration of PID stress. The Al-plate method was used in this experiment. The bias and temperature in the PID tests were set respectively to −1000 V and 85 °C. Data points represent the mean values of three identical modules, and the error bars correspond to the standard deviation of the mean. The solid lines represent visual guides. Reproduced with permission.[19] Copyright 2018, The Japan Society of Applied Physics.

Figure 7. Applied-bias dependence of $P_{max}/P_{max,0}$ of n-type front-emitter PERT cell modules in PID tests at 85 °C. The data points represent the mean values of three identical modules. Error bars correspond to the standard deviation of the mean.

Solid and dashed lines represent visual guides. Reproduced with permission.[19] Copyright 2018, The Japan Society of Applied Physics.

Figure 8. Schematic diagram of the proposed model for polarization-type PID in n-type front-emitter PERT cell modules. Panels (a), (b), and (c) show cross-sections of a module near the EVA/cell interface. (a) Before stressing, K centers exist in the front SiN_x film. (b) During application of a negative bias, positive charges accumulate on the surface of the front SiN_x film. (c) Positive charges subsequently extract electrons from K^0 and K^- centers, leaving K^+ centers. Reproduced with permission.[19] Copyright 2018, The Japan Society of Applied Physics.

Figure 9. Normalized P_{max}, short-circuit current I_{sc}, V_{oc}, and FF of modules fabricated from n-type front-emitter PERT cells with SiN_x/SiO_2 passivation stacks after 24-h PID testing at three different irradiance levels (0, 250, and 800 W/m^2). Two samples were tested at each irradiance level. The dashed line in blue is a guide for the eye. Reproduced with permission.[24] Copyright 2018, IEEE.

Figure 10. Normalized performance of TOPCon cells with front-side SiN_x/AlO_x passivation films after PID stress (−1000 V), after 5-h outdoor sunlight exposure and after 10-day indoor dark storage at room temperature. All parameters are normalized to their initial values. The uncertainty represents one standard deviation. Reproduced with permission.[32] Copyright 2019, Elsevier B.V.

Figure 11. Time evolution of $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF_0, and $P_{max}/P_{max,0}$ for n-type PERT modules tested until 100-h PID-stress exposure (−1000 V, 60 °C, 85% relative humidity). Cell I-a has a uniform SiN_x film with an RI of 2.0, and cell I-b has the Si-rich SiN_x interlayer with an RI of 2.4. Data extracted from reference. [26]

Figure 12. D-SIMS depth profiles for Na in n-type front-emitter PERT cells before and after 12-h and 480-h PID tests in which a negative bias of −1000 V was applied 85 °C and the profiles after recovery tests for the same duration as the PID tests. Reproduced with permission.[27] Copyright 2019, The Japan Society of Applied Physics.

Figure 13. Schematic diagrams of (a) a cross-section near the front surface of a rear-emitter n-type PERT c-Si cell with a Na-decorated stacking fault and (b) an expected band structure in the c-Si region affected by the Na-decorated stacking fault. Reproduced with permission.[34] Copyright 2016, IEEE.

Figure 14. $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF_0, and $P_{max}/P_{max,0}$ of the IBC PV cell modules as a function of the duration of the PID test performed in the dark and under one-sun illumination. Reproduced with permission.[39] Copyright 2021, The Japan Society of Applied Physics.

Figure 15. Cross-sectional SEM and EDX images of the n-type front-emitter PERT cell after the PID test in which a negative bias of −1000 V was applied at 85 °C for 480 h. Reproduced with permission.[27] Copyright 2019, The Japan Society of Applied Physics.

Figure 16. Respective (a) one-sun-illuminated and (b) dark *J–V* curves of SHJ PV modules before and after PID tests in which a negative bias of −1000 V was applied for 9, 18, and 32 days at 85 °C. The inset figure presents the dependence of the $J_{sc}/J_{sc,0}$ value on the PID test duration. Reproduced with permission.[41] Copyright 2018, John Wiley & Sons, Ltd.

Figure 17. (a) In K-edge and (b) W L_3-edge XANES spectra obtained from the front IWO film of an SHJ PV cell after a PID test. The experimentally obtained data are denoted by open circles. The solid lines were obtained by fitting the XANES spectra using data extracted from the pristine IWO film and from the standard In and W samples. The lines designated with "Pristine IWO" and with "In" respectively show the pristine IWO and metallic In components of the fitting curve. In panel (b), the best fit was obtained when the W component was zero. Therefore, the line for the W component is not shown. The fitting result indicates the formation of an additional metallic In component that accounts for approximately 24% of the total amount of In atoms. Reproduced with permission.[41] Copyright 2018, John Wiley & Sons, Ltd.

Table I. Summary of degradation mechanisms appearing in several representative n-type cell modules

Mechanism	Negative bias	Positive bias
Polarization-type PID	PERT (front)[16–26, 28, 29], PERL (front)[31], TOPCon (front)[32]	Bifacial PERT (rear)[33], IBC[15, 36–37]
Na-penetration-type PID	PERT (front)[18, 20], PERT (rear)[18, 33], IBC[34, 38]	—
Corrosion-type PID	PERT (front)[27], SHJ (front)[42], SHJ (rear)[39–42]	—

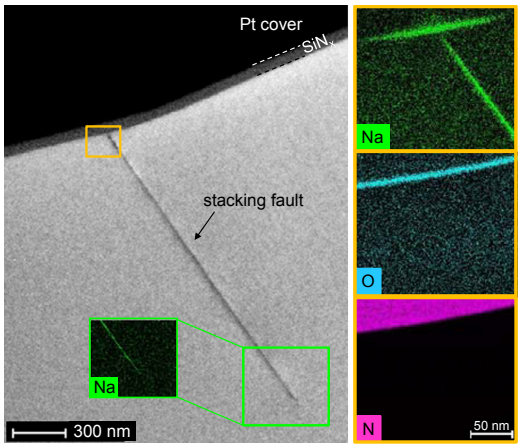


Figure 1

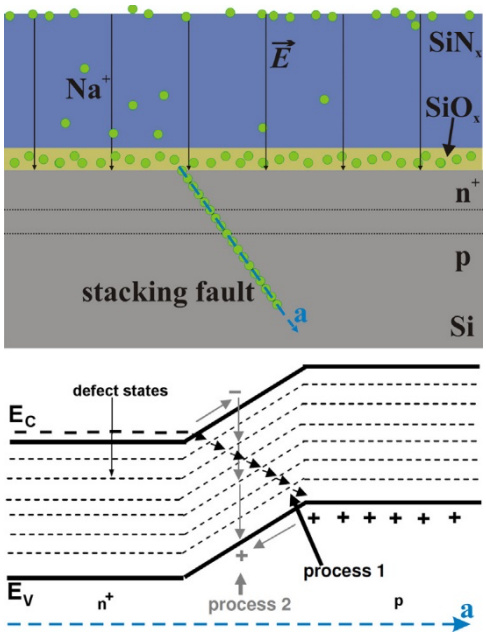

Na+
E
SiNx
SiOx
n+
p
stacking fault
a
Si
defect states
EC
EV
n+
process 2
process 1
p
a

Figure 2

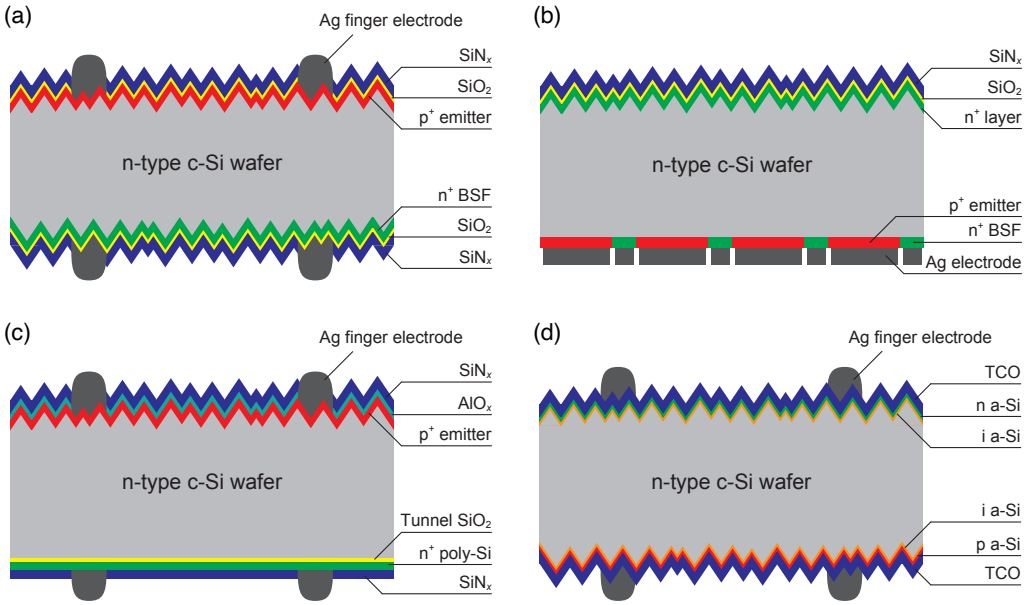

(a)
Ag finger electrode
SiNx
SiO2
p+ emitter
n-type c-Si wafer
n+ BSF
SiO2
SiNx
(b)
SiNx
SiO2
n+ layer
n-type c-Si wafer
p+ emitter
n+ BSF
Ag electrode
(c)
Ag finger electrode
SiNx
AlOx
p+ emitter
n-type c-Si wafer
Tunnel SiO2
n+ poly-Si
SiNx
(d)
Ag finger electrode
TCO
n a-Si
i a-Si
n-type c-Si wafer
i a-Si
p a-Si
TCO

Figure 3

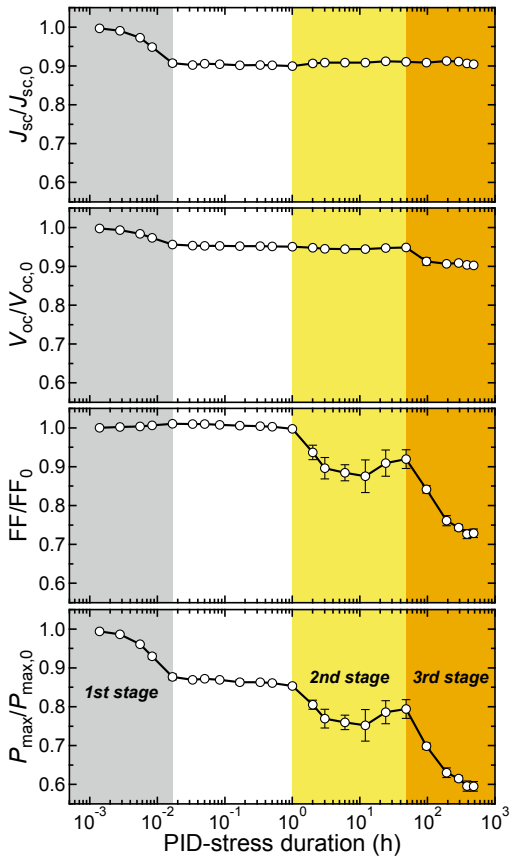

$J_{sc}/J_{sc,0}$
$V_{oc}/V_{oc,0}$
FF/FF$_0$
$P_{max}/P_{max,0}$
1st stage
2nd stage
3rd stage
PID-stress duration (h)

Figure 4

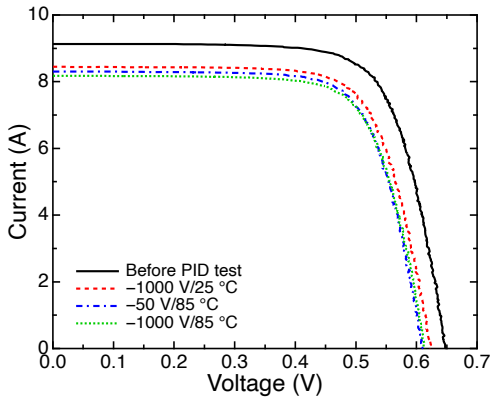

Current (A)
Voltage (V)
Before PID test
−1000 V/25 °C
−50 V/85 °C
−1000 V/85 °C
0
2
4
6
8
10
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7

Figure 5

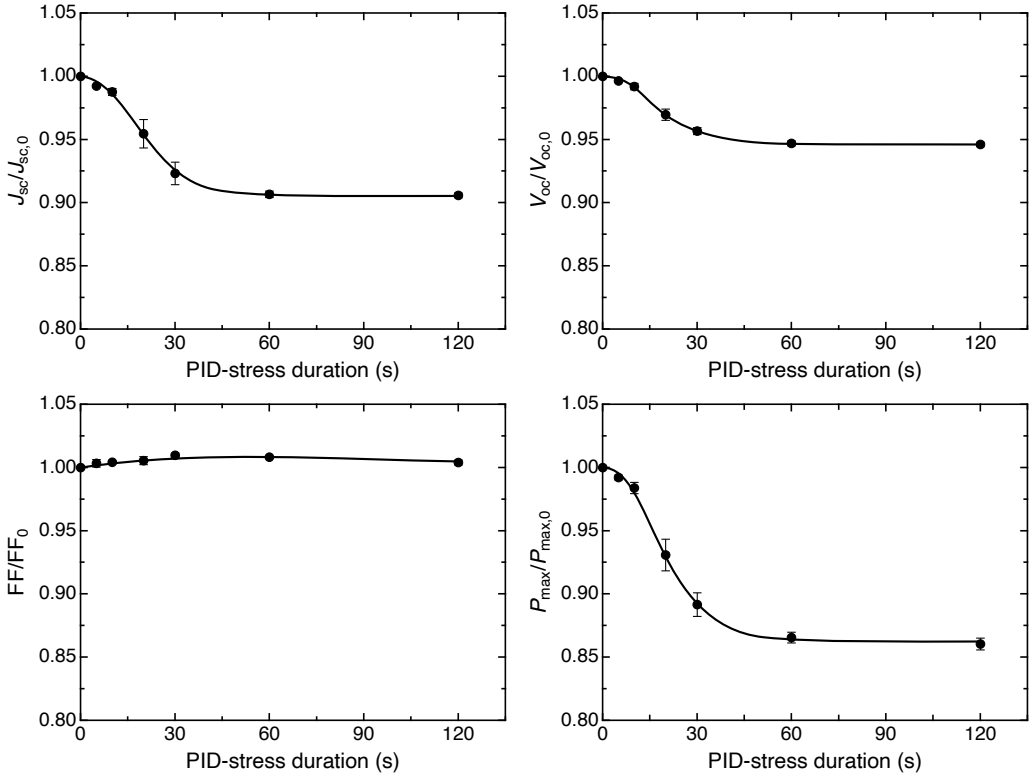

1.05
1.00
0.95
0.90
0.85
0.80
0
30
60
90
120
PID-stress duration (s)
$J_{sc}/J_{sc,0}$
$V_{oc}/V_{oc,0}$
FF/FF_0
$P_{max}/P_{max,0}$

Figure 6

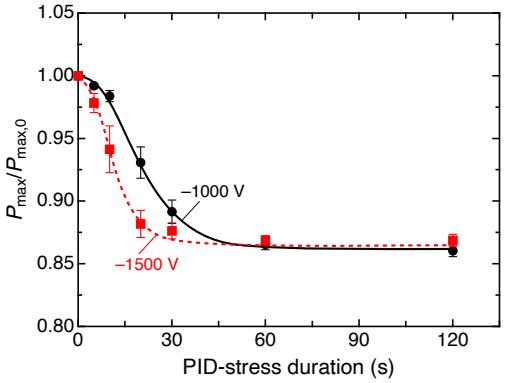

1.05
1.00
0.95
0.90
0.85
0.80
$P_{max}/P_{max,0}$
0
30
60
90
120
PID-stress duration (s)
−1000 V
−1500 V

Figure 7

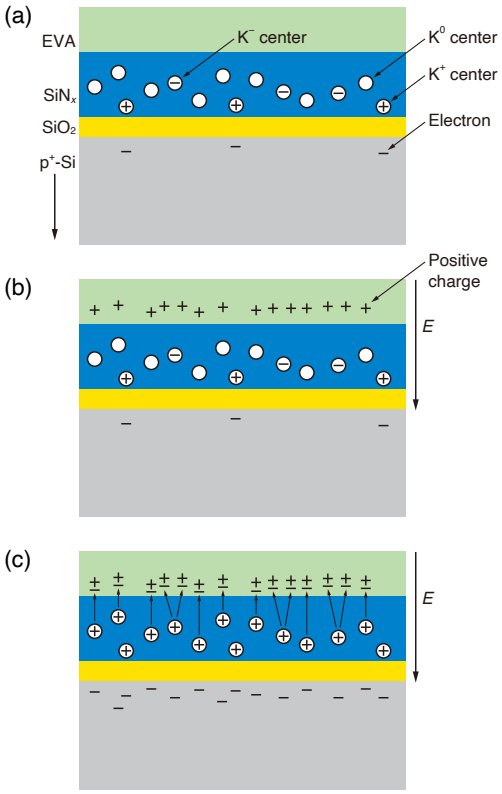

(a)
EVA
SiNx
SiO2
p+-Si
K− center
K0 center
K+ center
Electron
(b)
Positive charge
E
(c)
E

Figure 8

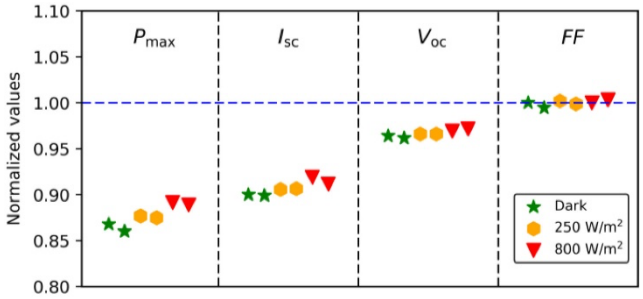

1.10
1.05
1.00
0.95
0.90
0.85
0.80
Normalized values
P_{max}
I_{sc}
V_{oc}
FF
Dark
250 W/m^2
800 W/m^2

Figure 9

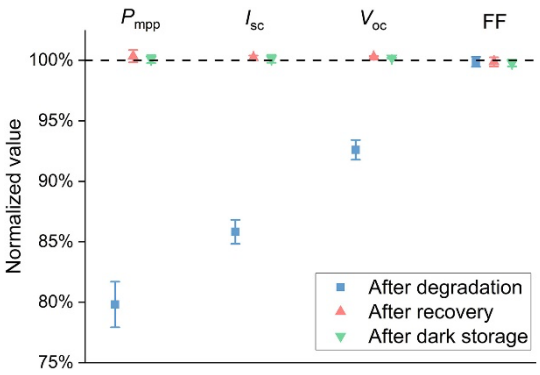

P_{mpp}
I_{sc}
V_{oc}
FF
100%
95%
90%
85%
80%
75%
Normalized value
After degradation
After recovery
After dark storage

Figure 10

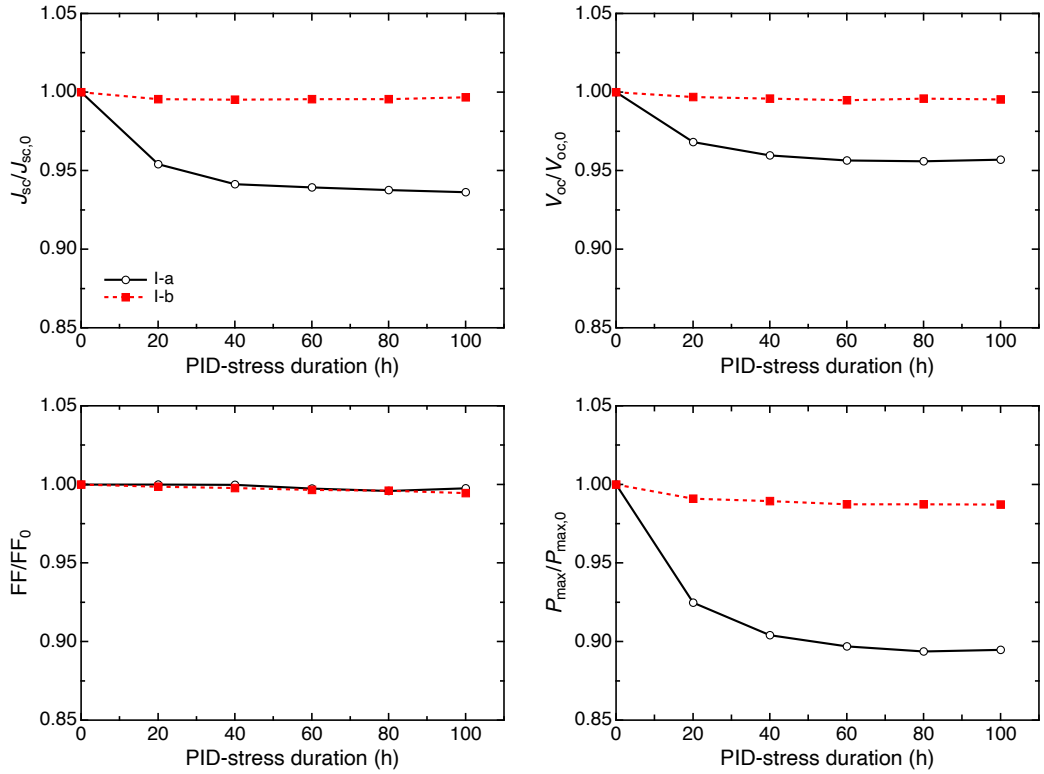

1.05
1.00
0.95
0.90
0.85
0
20
40
60
80
100
PID-stress duration (h)
$J_{sc}/J_{sc,0}$
I-a
I-b
$V_{oc}/V_{oc,0}$
FF/FF$_0$
$P_{max}/P_{max,0}$

Figure 11

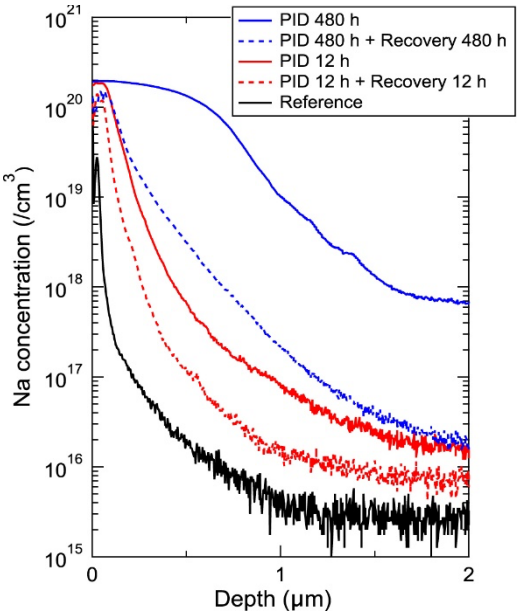

PID 480 h
PID 480 h + Recovery 480 h
PID 12 h
PID 12 h + Recovery 12 h
Reference
Na concentration (/cm3)
Depth (μm)
10^21
10^20
10^19
10^18
10^17
10^16
10^15
0
1
2

Figure 12

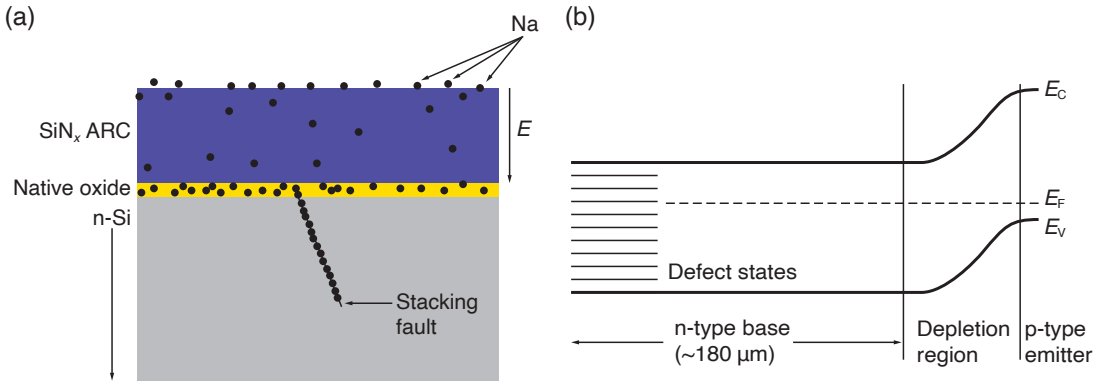

(a)
Na
SiNx ARC
E
Native oxide
n-Si
Stacking
fault
(b)
EC
EF
EV
Defect states
n-type base
(~180 µm)
Depletion
region
p-type
emitter

Figure 13

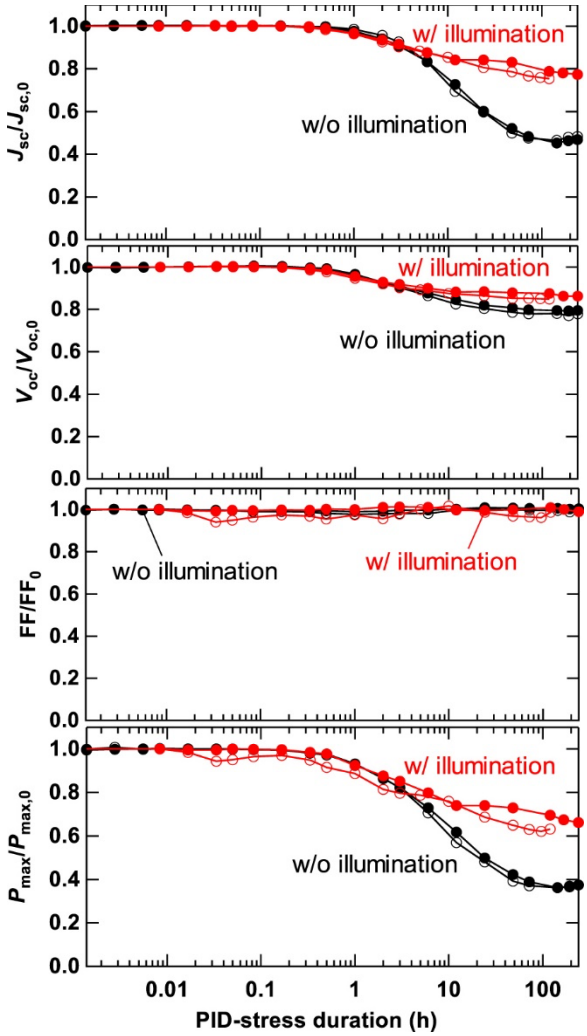

w/ illumination
w/o illumination
$J_{sc}/J_{sc,0}$
$V_{oc}/V_{oc,0}$
FF/FF_0
$P_{max}/P_{max,0}$
0.0
0.2
0.4
0.6
0.8
1.0
0.01
0.1
1
10
100
PID-stress duration (h)

Figure 14

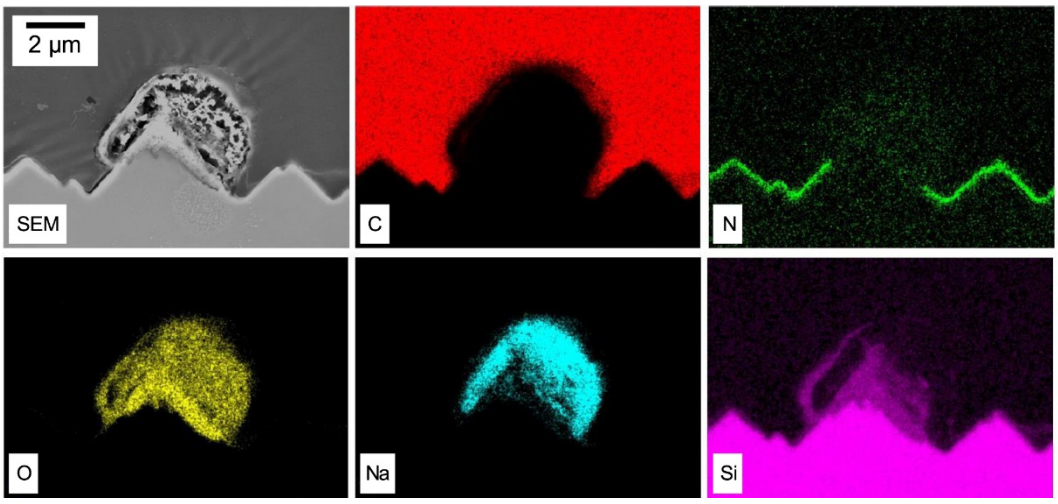


Figure 15

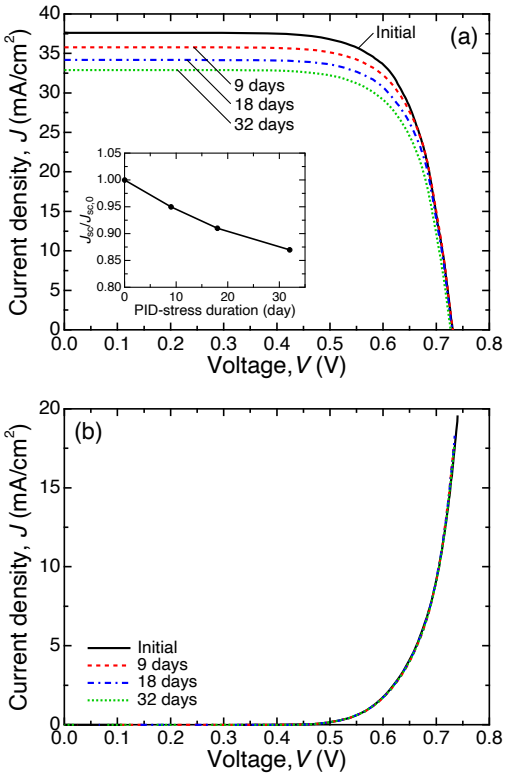

(a)
Initial
9 days
18 days
32 days
Current density, J (mA/cm2)
Voltage, V (V)
Jsc/Jsc,0
PID-stress duration (day)
(b)
Initial
9 days
18 days
32 days
Current density, J (mA/cm2)
Voltage, V (V)

Figure 16

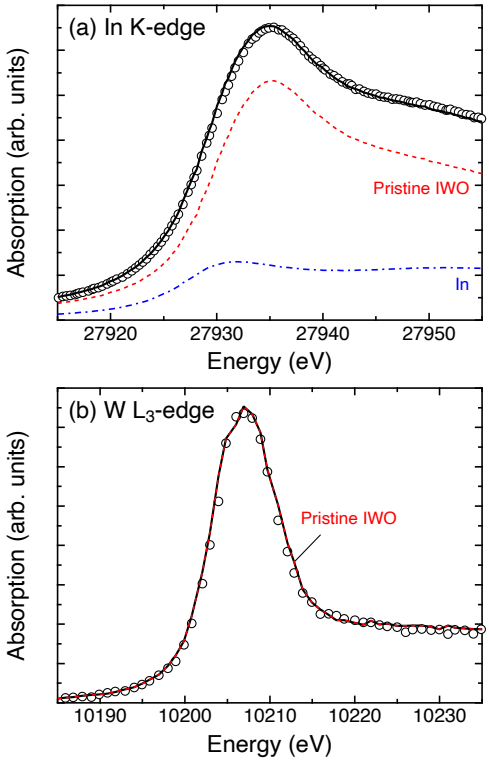
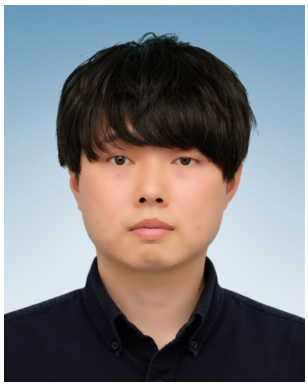

(a) In K-edge
Absorption (arb. units)
Pristine IWO
In
27920
27930
27940
27950
Energy (eV)
(b) W L3-edge
Absorption (arb. units)
Pristine IWO
10190
10200
10210
10220
10230
Energy (eV)

Figure 17

Biographies



Dr. Seira Yamaguchi received his Ph.D. degree in Materials Science from the Japan Advanced Institute of Science and Technology, Japan, in 2019. He joined Toyota Technological Institute as a postdoctoral researcher in 2019 and joined Niigata University as a Project Assistant Professor in 2020. His research work mainly covered the investigation of potential-induced degradation (PID) in n-type crystalline silicon solar cells, the development of PID acceleration test methods, and the fabrication of high-quality passivating contact materials. He is now an Assistant Professor at the University of Tsukuba. His current research interests include the characterization of carbon fiber reinforced plastics, perovskite solar cells, and organic semiconductor devices by operando electron spin resonance spectroscopy.

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Prof. Atsushi Masuda received his Ph.D. degree in Engineering from Kanazawa University, Japan, in 1996. In 1996 he joined the Japan Advanced Institute of Science and Technology, in 2005 he joined the National Institute of Advanced Industrial Science and Technology, and in 2020 he joined Niigata University. He is currently a Professor, Graduate School of Science and Technology, Niigata University. His main research fields are photovoltaics and thin-film electronic materials. He is the author and the co-author of over 250 technical papers and conference papers. He is a senior member of the Japan Society of Applied Physics.

Prof. Keisuke Ohdaira received his Ph.D. from the University of Tokyo in 2004. He then moved to Tohoku University and worked as a post-doctoral researcher (2004–2005). He became an Assistant Professor (2005–2011) in the Japan Advanced Institute of Science and Technology (JAIST), and promoted to an Associate Professor (2012–2018) and to a Professor (2018–) in JAIST. He received the best paper award of the 27th International Photovoltaic Science and Engineering Conference (PVSEC-27) in 2017. His current research topics are related to the application of catalytic chemical vapor deposition (Cat-CVD) for high-efficiency Si wafer-based solar cells and perovskite/silicon tandem cells, thin-film solar cells using polycrystalline silicon films formed by flash lamp annealing, and potential-induced degradation of crystalline silicon photovoltaic modules.