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Description	

Second-stage potential-induced degradation of n-type front-emitter crystalline silicon photovoltaic modules and its recovery

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We investigate the second-stage potential-induced degradation (PID) of n-type front-emitter (n-FE) crystalline silicon (c-Si) photovoltaic (PV) modules. The PID of n-FE c-Si PV modules is known to occur in three stages under negative bias stress. The second-stage PID is characterized by a reduction in fill factor (FF), due to the invasion of sodium (Na) into the depletion region of a p^+n junction and resulting increase in recombination current. The second-stage PID shows a curious independence on a negative bias voltage for the PID stress. This may indicate that the Na inducing the FF reduction comes not from the cover glass but originally exists on and/or near the cell surface. The FF reduction is recovered quite rapidly, within a few seconds, by applying a positive bias to the degraded cell. The recovered n-FE c-Si PV modules show more rapid degradation if they receive the negative bias stress again, which can be explained by Na remaining in the p^+ emitter.

Keywords: potential-induced degradation, photovoltaic module, n-type front-emitter solar cell, sodium

1. Introduction

The construction of large-scale photovoltaic (PV) power plants is ongoing due to increasing energy demand and concern in climate change. The usage of PV modules with higher efficiencies is desired for more generation and lower cost of electricity. PV modules with crystalline silicon (c-Si) solar cells have dominated the present share of the PV market because of their matured fabrication technology and high conversion efficiency.¹⁾ In particular, n-type c-Si PV cells have been expected as a next-generation standard for the PV modules²⁾ since they can have higher conversion efficiency than conventional p-type ones and higher stability against light soaking due to the absence of the problem of boron–oxygen complex formation.^{3,4)}

In the large-scale PV power plants, potential-induced degradation (PID) is one of the most serious issues in the long-term reliability of PV modules.⁵⁾ PID is a performance degradation of PV modules triggered by a voltage difference between a grounded aluminum frame and cells. The PID of conventional p-type c-Si PV modules has been investigated in detail and the mechanisms of the PID has been considerably clarified.^{5–12)} On the other hand, detailed studies on the PID for the n-type c-Si PV modules are insufficient and need to be investigated furthermore.^{13–19)}

We have thus far investigated the PID of n-type c-Si PV modules²⁰⁾ with cells such as rear-emitter,²¹⁾ front-emitter (FE),^{22–31)} interdigitated back-contact,³²⁾ and Si heterojunction structures.^{33–37)} Of those, n-type FE (n-FE) c-Si PV modules have been investigated in the most detail. We have clarified that the PID of n-FE c-Si PV modules occurs in three stages, under a negative bias stress, with different behaviors and mechanisms.²⁴⁾ The first-stage PID is generally referred to as polarization-type PID (PID-p). This type of PID occurs due to the accumulation of fixed charges in the surface dielectric film such as Si nitride (SiN_x).¹⁸⁾ In the n-FE c-Si PV modules, positive fixed charges are accumulated in the surface SiN_x by extracting electrons from K centers by a negative bias stress.^{22,23,30)} This accelerates the recombination of minority carriers, electrons, on the surface of the p^+ emitter, resulting in simultaneous reductions in short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}). The second-stage PID of n-FE c-Si PV modules is characterized by a reduction in fill factor (FF) alone.²⁴⁾ We have clarified that based on the change in the J – V characteristics of the modules by the PID stress, the reduction in FF is not mainly due to the formation of shunting path but due to

the enhancement of recombination current, unlike in the case of conventional p-type c-Si PV modules.¹¹⁾ Sodium (Na) ions may invade the depletion layer of the p⁺-n junction of an n-FE cell and act as recombination centers. The third-stage PID is characterized by serious further reductions in FF and V_{oc} . This occurs through the formation of Na-based dome-like structures on the surface of n-FE cells, by which the surface SiN_x is catastrophically destroyed.²⁵⁾ The three types of PID phenomena occur after different negative bias applications: ~1 min for the first-stage PID, ~1 h for the second-stage PID, and ~50 h for the third-stage PID in our indoor PID test at 85 °C under a negative bias of -1000 V.²⁴⁾ We have also clarified that the first-stage and second-stage PID can be recovered by applying a positive bias to the cell, whereas the third PID cannot be recovered significantly.²⁴⁾ Among the three types of PID, the second-stage PID and its recovery have not been fully clarified. In this study, we investigate the second-stage PID of n-FE c-Si PV modules and its recovery in more detail by systematically changing applied voltage and PID-stress duration.

2. Experimental procedures

We used homojunction bifacial c-Si PV cells with a size of 156×156 mm². The cells had SiN_x/SiO₂ passivation stacks on the p⁺ emitter side. We first cut the cells into 20×20 mm²-sized small pieces and then laminated using conventional module materials such as cover glass, ethylene-vinyl acetate copolymer (EVA) sheet, and backsheet consisting of 38-μm-thick polyvinyl fluoride (PVF)/250-μm-thick polyethylene terephthalate/38-μm-thick PVF. The p⁺ emitter side of the cells faced illumination so that the module becomes the n-FE structure. The details of the module fabrication have been reported elsewhere.²¹⁾

We performed PID tests for the n-FE c-Si PV modules using Al-plate method.³⁸⁾ Negative bias voltages of -50, -200, -600, and -1000 V were applied to the short-circuited electrodes of the n-FE c-Si cells with respect to a grounded Al plate placed on the cover glass of the modules. A conductive rubber sheet was inserted between the Al plate and the cover glass of the modules for better electrical connection between them. Some of the modules underwent positive bias application at a voltage of +1000 V for the recovery test after the PID test. The bias voltage was applied using an insulation tester (TOS7210S, KIKUSUI). The PID and recovery tests were performed in a dry chamber

under air atmosphere at 85 °C with no intentional humidity stress (estimated relative humidity <2%RH).

The n-FE c-Si PV modules before and after the PID and recovery tests were characterized by measuring current-density–voltage (J – V) characteristics in the dark and one-sun light illumination and external quantum efficiency (EQE) spectra.

3. Results

Figure 1 shows the J – V characteristics of n-FE c-Si PV modules before and after the PID test at a voltage of –1000 V for various durations. J_{sc} and V_{oc} decrease simultaneously in the first 120 s. This is typical behavior of the first-stage PID, PID-p, in n-FE c-Si PV modules, due to the accumulation of positive charges in SiN_x and resulting acceleration of surface recombination.^{22,23,30)} The modules then show different type of PID characterized by a reduction in FF alone after the PID test for 12 h. Note that the degradation of FF is not by the formation of shunting paths but by the increase in recombination current, current through the carrier recombination in the depletion layer of a p^+ – n junction, as confirmed in the negative bias region of Fig. 1. A longer PID test for 480 h results in further reductions in V_{oc} and FF. This degradation, the third-stage PID, is due to the formation of Na-based domes on the surface of n-FE cells.²⁵⁾

Figure 2 shows the J_{sc} , V_{oc} , FF and P_{max} , normalized by their initial values, of n-FE c-Si PV modules as a function of the duration of PID test at various negative-bias stresses. The first-stage PID, J_{sc} and V_{oc} reductions by PID-p, is seen after the PID test for $\sim 10^{-2}$ – 10^{-1} h. Note that the first-stage PID progresses faster at a larger negative voltage, while the saturated J_{sc} and V_{oc} values are independent of the applied voltage. These phenomena can be explained from the origin of the positive charges in SiN_x . Electrons of K^0 and K^- centers in SiN_x are extracted by the negative bias stress and K^+ centers left behind act as the positive charges. The faster PID-p at higher voltage may be due to more rapid electron extraction. The voltage-independent saturated J_{sc} and V_{oc} values originate from the existence of the upper limit of positive charges, in which all the K center are converted to K^+ centers.^{22,23,30)} The third-stage PID, V_{oc} and FF reductions due to the formation of Na-based domes, is seen after the PID test at voltages of –1000 and –600 V for $\sim 10^2$ h. The duration needed for the emergence of the third-stage PID and its degree depend on applied voltage, and the degradations are not clearly seen in the case of PID tests at voltages of

–200 and –50 V. The formation of the Na-based domes requires a quantity of Na ions, and the Na ions may come from the cover glass of the modules. The voltage dependence of the third PID is reasonable because more Na ions may reach the cells at higher voltage, while the domes may not be formed if the amount of Na is insufficient in the case of lower voltage. In contrast to the first-stage and the third-stage PID, the second-stage PID, characterized by FF reduction in a PID-stress duration of 10^0 – 10^1 h, seems to be independent of the applied voltage, except in the case of –50 V. As mentioned earlier, the FF reduction is due to the invasion of Na into the depletion region of a p^+ – n junction and resulting increase in a recombination current. One can see in Fig. 2 that the decreased FF reversely increases with increasing PID-stress duration and the increase in FF occurs earlier under higher negative bias stress. This may be because Na in the depletion region of a p^+ – n junction is drawn off to the surface Na-based domes.

Figure 3 shows the J_{sc} , V_{oc} , and FF, normalized by their initial values, of the n-FE c-Si PV module as a function of the duration of positive bias application at +1000 V after the PID test at a voltage of –1000 V for 12 h. J_{sc} and V_{oc} , degraded during the first-stage PID test, are recovered to the initial values within $\sim 10^{-2}$ h. This duration is similar to that for the degradation to their saturated values and is far from the total PID-stress duration of 12 h. This feature is reasonable since the origin of the positive charges in SiN_x is K^+ centers and there is an upper limit of the positive charges. We have already confirmed the duration needed for the recovery of the first-stage PID is independent of the prior total PID stress duration.²³⁾ On the other hand, FF, which is degraded for the 12-h PID stress, is recovered to the initial value much more rapidly by applying a positive bias only for 5 s. This indicates the existence of a curious mechanism of the disappearance of Na in the depletion region of a p^+ – n junction.

Figure 4 shows the dark J – V characteristics of the n-FE c-Si PV module before and after the PID test for 12 h at a voltage of –1000 V and after the successive recovery test for 12 h at a voltage of +1000 V. We see drastic changes of the J – V characteristics by the PID test, which are consistent with the degradations of J_{sc} , V_{oc} , and FF by the first-stage and the second-stage PID. The successive 12-h recovery test leads to the improvement in the dark J – V characteristics, but the initial J – V curve cannot be completely reproduced. Figure 5 shows the FF, normalized by its initial value, of the n-FE c-Si PV module after the 12-h PID test and the successive 12-h recovery test as a function of the second PID

test duration. Although the duration needed for the saturation of FF reduction is ~ 12 h in the first PID test, FF decreases more quickly and reaches the saturated value for 10^{-2} – 10^{-3} h in the second PID test.

We also investigated the recovery of the performance of an n-FE c-Si PV module only by heating. Figure 6 shows the J_{sc} , V_{oc} , FF, and P_{max} , normalized by their initial values, of the n-FE c-Si PV module after the 12-h PID test as a function of the duration of heating at 85 °C. J_{sc} and V_{oc} are recovered close to the initial values by heating for 1–10 h. The recovery of FF occurs more rapidly than those of J_{sc} and V_{oc} and the recovery is completed for ~ 30 s. The duration needed for the recovery by heating alone is larger than that in the recovery test with positive bias application as shown in Fig. 3, which indicates that the recovery of the performance is realized not only by heating but also by the bias application. Here we have also confirmed that the first-stage PID, PID-p, can also be recovered by heating alone.

4. Discussion

As demonstrated in the previous section, the FF reduction of n-FE c-Si PV modules by negative bias stress can be recovered by a following positive bias application. However, the behavior of FF recovery is different from that of the recovery of J_{sc} and V_{oc} . The durations needed for the reduction and recovery are almost the same in the case of the first-stage PID, J_{sc} and V_{oc} reductions, as shown in Figs. 2 and 3. This can be understood based on the mechanism of the first-stage PID. The first-stage PID occurs by the accumulation of positive charges in SiN_x by the formation of K^+ centers, and J_{sc} and V_{oc} are thus recovered by a reduction in the number of K^+ centers. The K^+ centers are formed by the extraction of electrons from K^0 and K^- centers and are annihilated by the addition of electrons, both of which take place through the flow of a leakage current. Thus, the increase and decrease in the K^+ centers, that is, degradation and recovery, occur in the equivalent duration. On the contrary, FF reduction in the first PID test requires 12 h but FF is recovered only for 5 s. This may indicate that the degradation state causing the FF reduction is unstable. The FF reduction occurs by the invasion of Na into the depletion region of the $\text{p}^+\text{-n}$ junction. We have previously performed secondary ion mass spectrometry measurement and experimentally confirmed that the 12-h PID stress, which induces the second-stage PID, increases the concentration of Na in the n-FE cells.²⁵⁾

Based on the reported very low diffusion coefficient values of Na in c-Si,³⁹⁾ it is unlikely that Na diffuses through Si crystal. The formation of Na-decorated stacking faults has been observed in p-type c-Si cells after the PID stress,^{9,10,40)} and the Na invasion into the depletion region may occur also in n-FE cells through the same mechanism. Ohno et al. have demonstrated that the Na-decorated stacking faults in undoped or n-type Si are much less stable than those in p-type Si.⁴¹⁾ The Na atoms in the stacking faults existing in the depletion region of the p⁺-n junction can thus be removed more easily than those in p⁺ region during the recovery process. We speculate that Na ions may be partly or completely diffused out from the stacking faults in the depletion region, whereas Na-decorated stacking faults may remain in the p⁺ region. This can explain the curious facts that the dark $J-V$ characteristics cannot be fully recovered to the initial state even after a sufficiently long positive bias application. It is known that the stacking faults formed by the PID stress continue to exist even after the release of Na from them.⁴²⁾ The remaining stacking faults themselves may also partly contribute to the imperfect recovery of the dark $J-V$ characteristics. The remaining Na-decorated stacking faults in the p⁺ region can also explain the faster emergence of the FF reduction in the second PID test. The diffusion barrier for Na in Na-decorated stacking faults is known to be ~ 0.3 eV, which is much lower than that of empty stacking faults (~ 2.0 eV) and of Si bulk (~ 1.3 eV).⁴⁰⁾ Na can thus quickly invade into the depletion region through the Na-decorated stacking faults during the second PID test.

We next discuss the voltage independence of the second-stage PID. If the Na atoms causing the second-stage PID come from cover glass, the duration needed for the drift through EVA encapsulant must depend on the applied voltage and the emergence of FF reduction must depend on the applied voltage. The Na causing the second-stage PID may originally exist on or near the surface of the cell. On the contrary, the third-stage PID, the formation of Na-based domes,²⁵⁾ shows clear voltage dependence, as shown in Fig. 2, and the Na source for the third-stage PID may be the cover glass. This is reasonable since more Na atoms are needed for the formation of Na-based domes.

Finally, we discuss the second-stage PID, FF reduction, of n-FE c-Si PV modules in actual outdoor operation. Since we have observed the FF reduction of n-FE c-Si PV modules operated in outdoor condition,³¹⁾ possible measures for the suppression of the second-stage PID should be considered. Positive-bias application and/or heating can

recover the FF of n-FE c-Si PV modules, as shown in Figs. 3 and 6. These are, however, not the best ways for the mitigation of the second-stage PID since, once the degradation occurs, the re-degradation of FF takes place more rapidly, as shown in Fig. 5. The usage of n-FE c-Si PV cells and/or encapsulant containing less Na may mitigate the second-stage PID. In addition, drifting Na ions away from the cell surface by positive bias application prior to the outdoor installation of the modules may lead to the delay of the FF reduction. More effective suppression of the second-stage PID may be realized by repeating the positive bias application during their outdoor usage before the formation of Na-decorated stacking faults in the p^+ emitter.

5. Conclusion

The second-stage PID of n-FE c-Si PV modules has been investigated in detail. We have observed that the second-stage PID is independent of the applied negative voltage, except for the case of an extremely low voltage. Na atoms causing the FF reduction may thus exist on and/or near the surface of the cells. The recovery of FF by positive-bias application occurs quickly, within a duration much smaller than the duration needed for the FF reduction. We also observed that dark J - V characteristics cannot be completely recovered to the initial state. These phenomena may be explained by the mechanism of the invasion of Na into c-Si. Na-decorated stacking faults may be formed during the invasion process and they may remain in the p^+ region even after the recovery process.

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Figure captions

Fig. 1 J - V characteristics of n-FE c-Si PV modules receiving a PID test at a voltage of -1000 V.

Fig. 2 J_{sc} , V_{oc} , FF, and P_{max} , normalized by their initial values, of n-FE c-Si PV modules as a function of the duration of the PID test at various voltages.

Fig. 3 J_{sc} , V_{oc} , and FF, normalized by their initial values, of the n-FE c-Si PV module as a function of the duration of positive bias application at $+1000$ V after the PID test at a voltage of -1000 V for 12 h.

Fig. 4 Dark J - V characteristics of the n-FE c-Si PV module before and after the PID test for 12 h at a voltage of -1000 V and after the successive recovery test for 12 h at a voltage of $+1000$ V.

Fig. 5 FF, normalized by its initial value, of the n-FE c-Si PV module after the 12-h PID test and the successive 12-h recovery test as a function of the second PID test duration.

Fig. 6 J_{sc} , V_{oc} , FF, and P_{max} , normalized by their initial values, of the n-FE c-Si PV module after the 12-h PID test as a function of the duration of heating at 85 °C.

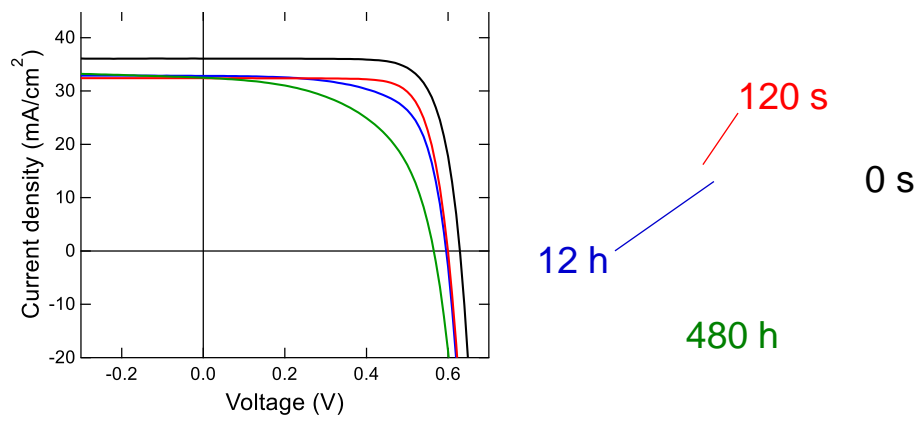


Figure 1 K. Ohdaira et al.

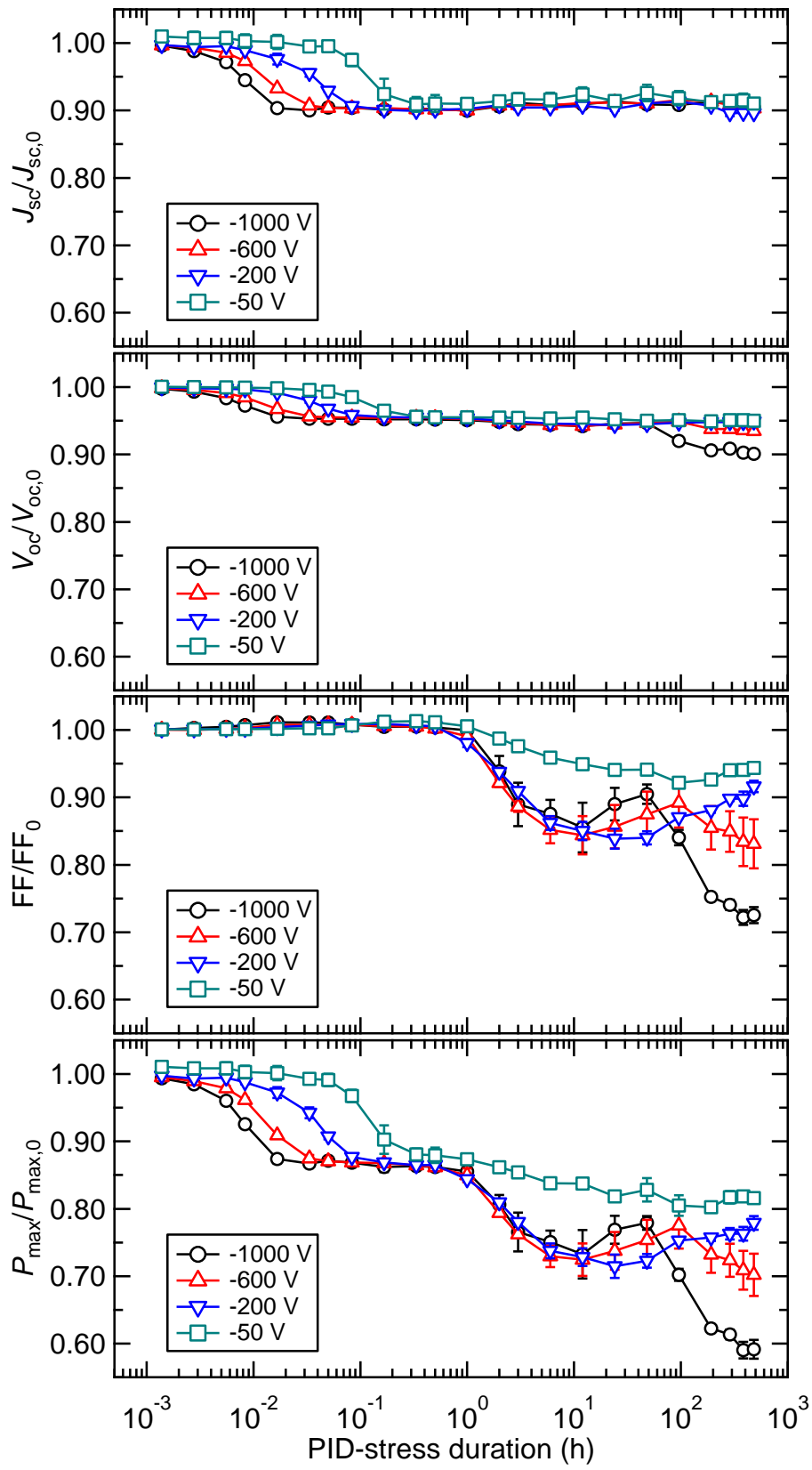


Figure 2 K. Ohdaira et al.

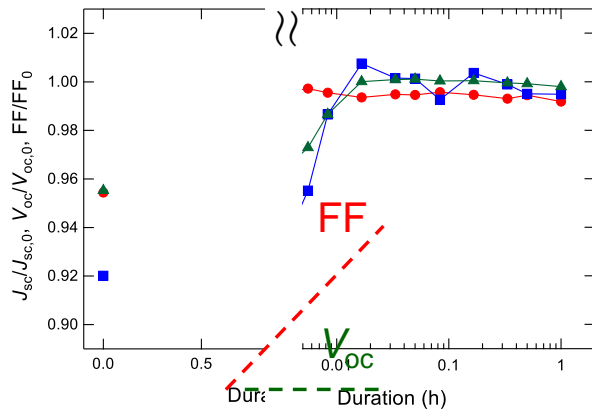


Figure 3 K. Ohdaira et al.

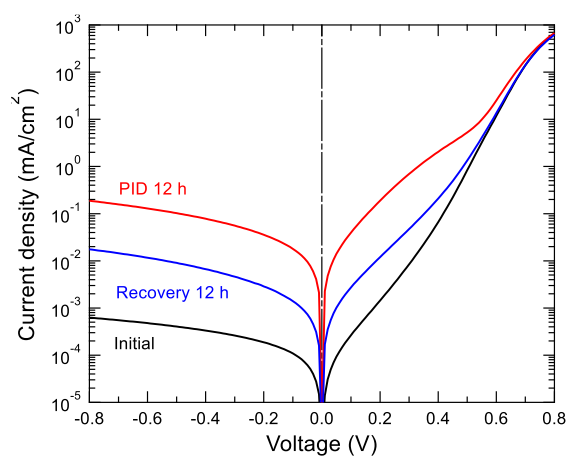


Figure 4 K. Ohdaira et al.

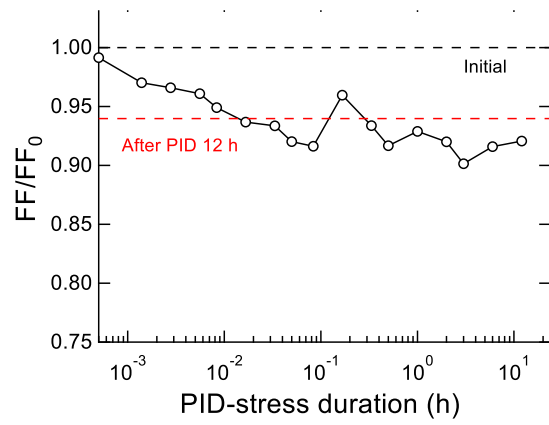


Figure 5 K. Ohdaira et al.

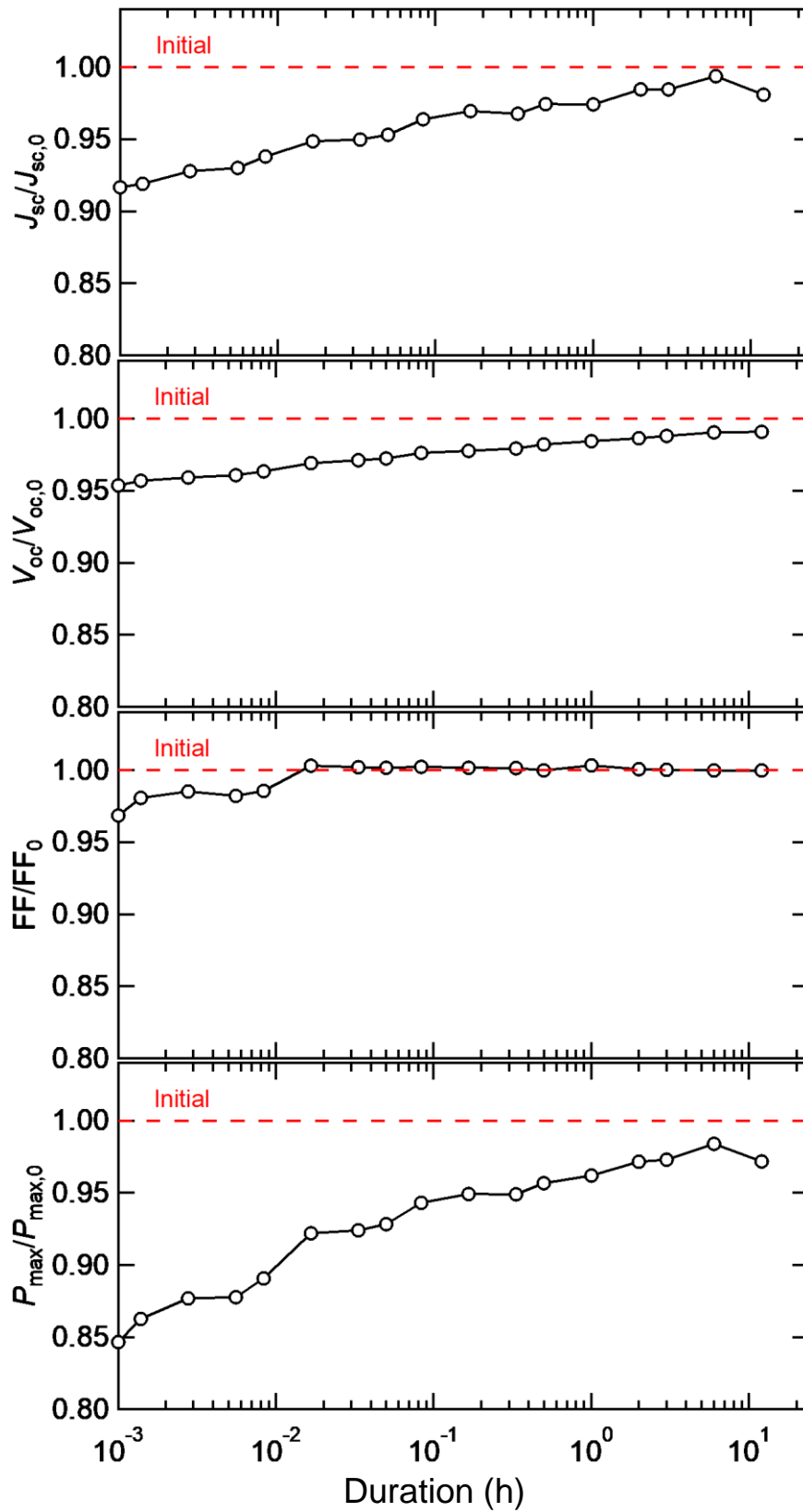


Figure 6 K. Ohdaira et al.