Reconfigurable Cache for Real-Time Data Applications

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1 Introduction

The processor is making to high performance has been achieved by improving, a super-scalar of the operation frequency, and using the instruction level parallelism, for example, VLIW in the background of the advancement of the integration of the transistor in recent years. On the other hand it is not improved as for perfprmance of the memory access. Therefore,the execution performance being limited by the memory access is problem.

In this research, to use the cache memory effectively, the composition of the cache memory is dynamically changed. That is, to correspond to different demands according to the application used, it changes it into the cache memory composition of the exclusive use corresponding to the application. To give not only the exclusive use but also generality, a usual cache access can be done to the accesses excepting for a specific application.

The following three functions are achieved by the reconfigurable cache memory.

1. Partition Based on Priority of Real-Time Task
2. FIFO Buffer Receiving Large-Scale Data
3. Prefetch Buffer Receiving Prefetched Block

2 Three Functions by Reconfigurable Cache Memory

2.1 Partition Based on Priority of Real-Time Task

It is effective to use the processor of the MultiThreading to do efficient execution though processing separately for two or more tasks is done when a real- time application is executed. However, the cache miss increases in the processor of the MultiThreading so that two or more tasks may compete and use one cache, and there is a possibility that the execution performance decreases. In the reconfigurable cache used by this research, the partition that limits the cache area of each task to delete the influence between tasks and allocates it is divided.

2.2 FIFO Buffer Receiving Large-Scale Data

As for reconfigurable cache, the FIFO partition is prepared, and the stride data transfered by DMA transfer about SDT etc. is received for the application that needs a large-scale stream data like the media processing. When reconfigurable cache as FIFO partition, the partition is divided by a unit that is more detailed than the way-cache, the function as the data cache is not disturbed, and the execution performance is improved.

2.3 Prefetch Buffer Receiving Prefetched Block

There is a problem of cache-index conflict. Before Prefetch data is actually used, it is replaced by the competition with other data in usual cache. Frequently accessed data is replaced by Prefetch data in usual cache. It solves it by using reconfigurable cache that one partition as Prefetch buffer in this research.

3 Simulation Environment

In this research the simulator uses the integer instruction group of SPARC Architecture Version 8 as an instruction set. The data cache of the simulator uses 4 way-set-assosiative cache. 4KB of the area of 1 way-cache. The block size of 32 byte, the cash size by 16KB.

4 Evaluation and Consideration

The sort program and the matrix calculation program are used to evaluate the partition based on the priority of real-time task. Livermore Kernel is used to evaluate the FIFO partition and Prefetch partition.

5 Related Work

The relation research on Reconfigurable cache memory and Prefetch buffer are described.

6 Conclusion

Units that are more detailed than way-cache because of expanding tag and comparator when reconfigurable cache uses. The partition division is enabled that it is an offer of the partition of the proper size to various applications.

When two or more tasks are executed like a real-time application, through put can be improved by using the processor of the MultiThreading. In the evaluation, it was shown that the execution of the task of high priority was able to be improved execution by securing the cache area where the task of high priority was able to be used by reconfigurable cache.

When reconfigurable cache as the SDT,it was shown to improve the execution performance of the application by decreasing the competition between data cache and FIFO partition enough area for the SDT.

In the data prefetch mechanism, the competition between prefetch data and other data was solved giving reconfigurable cache as prefetch partition, and the cache miss was deleted greatly.

It has a mutually different because of compare SDT and Prefetch functions that are the functions to do data prefetch from the memory to cache advantage and fault. It was shown to use these two functions properly according to the usage, to solve for a fault each other, and to improve the execution performance by having both functions in this research.