Research on High Speed Detection of Audio Watermark by Hardware

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1 Introduction

This paper proposes high speed digital watermark detection method by parallelized hardware on a FPGA. The digital audio watermarks are a technique to embed author information into digital audio. Author information mean author name or author ID etc. These are inaudible signals. Recently, illegal copies and illegal distributions are serious problem, and watermarking is useful method to defend illegal copies. In order to prevent illegal distribution, high speed and parallel watermarks detection is required. However, detection speed is too slow for real time watermark detection.

This paper proposes a method that the watermark detection algorithm is implemented on hardware for high speed and parallel detection. First, a suitable algorithm for the hardware is examined for high speed and parallel detection. Second approach for high speed and parallel detection is proposed the efficiency improvement technique and the parallel technique. A prototype circuit on a FPGA for high speed and parallel digital watermark detection is implemented. Finally, the performance of the prototype hardware is evaluated and the system to prevent the illegal distribution is proposed.

2 Digital Audio Watermarking Algorithm

Digital audio watermarking is the technique to embed author information into digital audio. This is inaudible to human ear. There are two typical schemes for audio watermarking. One of them uses a frequency domain and another uses a time domain. These schemes need the original audio or the watermark when detecting the watermark. This paper proposes the method that the digital audio watermark detection algorithm is implemented on the hardware for high speed and parallel detection. But, all watermark algorithms are not suitable for implementing on the hardware. Because of that the hardware has various restrictions. Therefore, a suitable algorithm for hardware is examined and suitable algorithm implements on the hardware. The hardware should not use the floating point arithmetic and multiplications and divisions calculation abundantly, and the hardware dose not have a lot of memories. This paper uses the audio watermark algorithm that uses the watermark when detecting it and uses the time domain. By preliminary experiment, this algorithm is able to be detected with software in 11.87 seconds, when it detects 50 watermarks.

3 Hardware

The audio watermark algorithm is implemented on the FPGA for high speed and parallel detection. In order to shorten the development period, this paper uses the RC2000 and Handle-C. RC2000 is FPGA board that has an xc2v8000 FPGA chip. Handle-C is a C-like language of circuit description. There are two policies for development of the hardware circuit. One policy is to make a high speed and small circuit without multiplication and division calculations. Another policy is to make a parallel circuit for parallel detection. Two problems occurred when the circuit was implemented on the FPGA. One problem is the lack of the memory capacity for storing many watermarks. So, this paper proposes theirs solution. This paper uses the external memory on the RC2000 for the solution of the lack of the memory capacity. The board can accommodate 192 watermark detection circuit, if we could use unlimited logical circuit. Another problem is the delay by the division calculation that can not be reduced. This paper

proposes the technique of watermark detection that does not use division at all for the solution of the delay of division. The prototype hardware circuit that is able to detect 25 and 50 watermarks at same time is implemented on the RC2000 by using solutions for problems.

4 Performance evaluation

The performance of the prototype circuit is evaluated. This paper measures and compares the detection time with the prototype circuit and the software. Time for 50 watermarks detection is 0.5s by the prototype circuit with 30MHz clock. Although time for 50 watermarks detection time by the software is 11.87s. So the prototype circuit is 23 time faster than the software. The software detection time increases in proportion to the number of watermarks. On the other hand, the prototype circuit detection time is not in proportion to the number of watermarks. So, the prototype circuit is useful for a lot of watermarks detection. This paper evaluates the critical path and the amount of circuit. By the result of the critical path evaluation, the maximum clock speed of the prototype circuit is 40MHz. The 82 watermarks detection circuit is able to implement on the RC2000 by the evaluation of the amount of circuit.

5 Illegal distribution monitoring system

An illegal distribution monitoring system is proposed. This system is monitoring the illegal audio file distribution in the internet. This system detects watermarks from an audio file that is transferred in the network. If the watermark is detected from the audio file, its transfer is stopped. This system uses the watermark detection hardware that is the prototype circuit for high speed and parallel watermark detection. This paper shows that this system does not become the bottleneck of network and this is useful by the devising of management.

6 Conclusion

This paper proposes high speed digital audio watermark detection by parallelized hardware on a FPGA. A suitable audio watermark detection algorithm in the time domain for hardware was shown. This algorithm was implemented on a FPGA and achieved high speed and parallel detection. The detection time by this prototype circuit is 23 times faster than the software. This prototype circuit is able to execute with 40MHz clock speed, and can detente up to 82 watermarks. Finally, this paper shows a concept of an illegal distribution deterrent system using the prototype circuit.