Research of high speed and low power consumption Netowork Processor that apply VLIW architecture

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1 Introduction

As the number of network users increases, further speed-up of network data transfer is required. One of the bottle neck to speed up data transfer is the routing process at packet forwarding.

Moreover, the most high speed routers comprised in the core of the network are constituted of general-purpose processors and ASIC chips. However, it takes a great amount of cost and time to develop ASIC chips with high performance.

In such a background, the Intel Corp. developed an network processor that is software controlled and specialized for network equipments. This network processor is expected that low cost routers with sophisticated and flexible features can be developed in a short time by using its capability of software implementation and performance improvement with ease of process parallelization.

Packet forwarding is a major part of processing in the network processor, for which the VLIW architecture is appropriate. The VLIW processor can execute in parallel data transfer(load/store), conditional branch, and arithmetic logical operations.

This paper proposes an instruction set of a VLIW architecture which can execute operations in parallel specialized for looking up the routing address table. The VLIW instruction achieves high performance, and reduces power consumptions because of circuit simplification of the VLIW architecture.

2 Network Routing

The IXA (Internet eXchange processor Architecture) of the Intel Corp. is a typical semiconductor architecture of the network processor which is specialized for network equipments.

The major operations of the network processor are spent on packet forwarding process, receiving packets, looking up the routing table, and sending packets. The routing table looked up by the router is dynamically changed. Since a looking up operation is performed for every packet, it occurs several thousands to millions times per second. Therefore, this processing is a bottleneck of the entire network.

The function of routing operation is mainly to analyze IP address stored in a input packet header, and to lead to a target exit port. The routing table is conceptually a table storing pairs of a destination IP address and an exit port number. It is inefficient to retrieve the table, because it takes time proportional to the table size.

Therefore, a representation called Patricia tree is used. It has branches, left and right, corresponding to 0/1 of IP address binary repressions, and stores a pair of a target IP address and an exit port number in a leaf of the Patricia tree.

The advantage of the Patricia tree is to find fast an exit port because it judge only on/off of each bit when matching an IP address. Moreover, the another advantage is to maintain an efficient retrieval tree by restructuring the tree if the routing information changes dynamically.

3 VLIW Instruction set

The loop frequency increase by depth deep as for the search for the Patricia tree, and the next packet must stand by while working previous packet.

There are a lot of uselessness.Then, VLIW Instruction set was designed so that parallel execution was possible. 5 units of ld*1,ldd*1,st*1,alu*1 and bra*1 in total are used at the instruction usually. The instruction set that uses this resource is assumed to be an VLIW A instruction set. The unit frequently used is added, and the instruction set that uses 7 units of ld*2 ldd*1 st*1 alu*2 and bra*1 in total is assumed to be VLIW B instruction set.

4 Estimate

Whether the resource can be effectively used by all means and about speed-up to the Patricia tree search by using the instruction set of the technique for proposing is evaluated.

The number of packets treatable at the same time depends on a usual cycle of processing and the use rate of each unit. A total cycle of this search operation is 51 cycles, and ld instruction is used by 15 cycles among those.

The processing cycle that hangs around one packet compared with usually becomes 54.3% for the VLIW A instruction set. However, because only time and the same usual can be used, waiting for the unit happens frequently, and the resource is decreased after a peak of 31.1% of level 1.

The processing cycle that hangs around one packet compared with usually becomes 33.0% for the VLIW B instruction set. In addition, it usually rises to the bottom by 35.4% in level 1 at the use rate of the unit compared with same usual.

5 Conclusion

In VLIW B Instruction set, both sides of the speed-up of effective use and the tree search of the resource were able to be achieved by adding the unit with high use frequency.