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Description	

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**Low-frequency noise in AlTiO/AlGaN/GaN
metal-insulator-semiconductor field-effect transistors with
non-gate-recessed or partially-gate-recessed structures**

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(Dated: July 14, 2023)

Abstract

We have systematically investigated low-frequency noise (LFN) in AlTiO/AlGaN/GaN metal-insulator-semiconductor field-effect transistors (MIS-FETs) with non-gate-recessed or partially-gate-recessed structures, where gate insulators using AlTiO, an alloy of Al₂O₃ and TiO₂, are obtained by atomic layer deposition. For drain current LFN, we find pure $1/f$ spectra for the well-above-threshold regime, and superposition of $1/f$ and Lorentzian spectra near the threshold voltage. The Hooge parameters are evaluated from the $1/f$ contribution and found to be independent of the AlTiO thickness. However, the remaining AlGaN thickness strongly affects the Hooge parameter near the threshold voltage; in the low channel electron concentration regime of the partially-gate-recessed FETs, a smaller remaining AlGaN thickness gives a larger Hooge parameter proportional to the inverse of the electron concentration, indicating that channel electron number fluctuation dominates the Hooge parameter. We consider that the channel electron number fluctuation is caused by electron traps introduced by the recess etching process in the remaining AlGaN. On the other hand, the Lorentzian spectra give specific time constants almost independent of the AlTiO thickness and the remaining AlGaN thickness, corresponding to trap depths of 0.6-0.8 eV. This can be attributed to traps in AlTiO near the AlTiO/AlGaN interface.

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I. INTRODUCTION

For high-speed and high-power applications, GaN-based metal-insulator-semiconductor field-effect transistors (MIS-FETs) have been extensively investigated using various gate insulators, such as high-dielectric-constant (high- k) oxides Al_2O_3 [1], HfO_2 [2, 3], TiO_2 [4], AlSiO [5, 6], AlTiO [7–12], high- k oxynitrides TaON [13], AlON [14], and high- k nitrides BN [15, 16], AlN [17–21]. In particular, $\text{Al}_x\text{Ti}_y\text{O}$ (AlTiO), an alloy of Al_2O_3 and TiO_2 , is an important insulator, because it can be applied to dielectric constant engineering, energy gap engineering, and interface charge engineering [11]. Previously, we reported normally-off operations in partially-gate-recessed $\text{AlTiO}/\text{AlGaN}/\text{GaN}$ MIS-FETs using gate insulators AlTiO with a rather thick remaining AlGaN thickness [12]. However, for gate-recessed AlGaN/GaN MIS-FETs, in addition to the problem of device instability [22, 23], low-frequency noise (LFN) will be enhanced [24–28], influenced by the insulator itself and the insulator/etched-semiconductor interface. Although several studies have shown that enhancement in LFN is ascribed to the channel mobility degradation/fluctuation in the partially-gate-recessed [24] and the fully-gate-recessed AlGaN/GaN MIS-FETs [25–28], the underlying physics is not clear. Moreover, in addition to $1/f$ LFN spectra [21, 29–34], Lorentzian LFN spectra are sometimes observed [7, 35–41], which are strongly related to the insulator materials and the device fabrication processes. Thus, LFN characterization is an important diagnosis for gate-recessed AlGaN/GaN MIS-FETs.

In this study, we systematically investigated LFN in $\text{AlTiO}/\text{AlGaN}/\text{GaN}$ MIS-FETs with non-gate-recessed or partially-gate-recessed structures, using an $\text{Al}_x\text{Ti}_y\text{O}$ ($x/(x+y) = 0.73$, energy gap $E_g \sim 6$ eV, dielectric constant $k \sim 14$) gate insulator obtained by atomic layer deposition (ALD) [7, 9, 11, 12]. For drain current LFN, we find pure $1/f$ spectra for the well-above-threshold regime, and superposition of $1/f$ and Lorentzian spectra near the threshold voltage. The Hooge parameters are evaluated from the $1/f$ contribution and found to be independent of the AlTiO thickness. However, the remaining AlGaN thickness strongly affects the Hooge parameter near the threshold voltage; in the low channel electron concentration regime of the partially-gate-recessed FETs, a smaller remaining AlGaN thickness gives a larger Hooge parameter. We consider that this is owing to electron traps introduced by the recess etching process in the remaining AlGaN . On the other hand, the Lorentzian spectra give specific time constants almost independent of the AlTiO thickness and the remaining

AlGa_N thickness, corresponding to trap depths of 0.6-0.8 eV. Since the gate leakage currents are dominated by Poole-Frenkel mechanism due to traps with the similar depth in AlTiO, we consider that the Lorentzian spectra are attributed to traps in AlTiO near the AlTiO/AlGa_N interface.

II. DEVICE FABRICATION AND CHARACTERISTICS

The fabrication of the non-gate-recessed and partially-gate-recessed AlTiO/AlGa_N/Ga_N MIS devices, MIS-FETs and MIS-capacitors, started from an Al_{0.24}Ga_{0.76}N (20 nm)/Ga_N(3 μ m) heterostructure on sapphire(0001), followed by Ti/Al/Ti/Au Ohmic electrode formation. For gate recess process, the AlGa_N layer was etched by using electron cyclotron resonance nitrogen plasma, with the radio frequency power of 100 W, the acceleration voltage of 100 V, and the ion beam current density of 0.3 mA/cm². The etching rate was $\simeq 1.2$ nm/minute and the etching depths were $\simeq 9$ nm and $\simeq 15$ nm (i.e., the remaining AlGa_N thickness $d_{\text{AlGaN}} \simeq 11$ nm and $\simeq 5$ nm, respectively), as measured by atomic force microscopy. After etched-AlGa_N surface cleaning by acetone, methanol, oxygen plasma ashing, and a TMAH-diluted solution to remove oxide and oxygen-related molecules, Al_xTi_yO ($x/(x+y) = 0.73$, $E_g \sim 6$ eV, $k \sim 14$) gate insulators with several thicknesses ($d_{\text{AlTiO}} = 26, 18$, and 11 nm) were formed by ALD at 130 $^{\circ}\text{C}$ using TMA (trimethylaluminum), TDMAT (tetrakis-dimethylamino titanium), and water [7, 9, 11, 12], followed by post-deposition annealing at 350 $^{\circ}\text{C}$ in H₂-mixed Ar. After necessary device isolation by B⁺ ion implantation, Ni/Au gate electrodes were formed. Finally, post-gate annealing at 400 $^{\circ}\text{C}$ in N₂ completed the device fabrication. Figure 1(a) and (b) show the device dimension of the non-recessed and partially-recessed MIS-FETs, respectively. In the latter, the recessed gate of length $L_{\text{RG}} = 2$ μm is overlapped by the total gate of length $L_{\text{G}} = 2.5$ μm . The source-drain distance is 5 μm , and the gate width is $W = 50$ μm . Figure 1(c) and (d) show the device dimension of the non-recessed and partially-recessed MIS-capacitors, respectively, where the recessed area $S_{\text{RG}} = 70^2$ μm^2 is overlapped by the total gate area $S_{\text{G}} = 75^2$ μm^2 , which is surrounded by the Ohmic electrodes.

Basic characteristics were obtained for each device. Figure 2(a) and (b) are output and transfer characteristics for a non-recessed FET ($d_{\text{AlGaN}} = 20$ nm, $d_{\text{AlTiO}} = 26$ nm), respectively, where I_{D} is the drain current, I_{G} is the gate current, and g_{m} is the transconductance,

which are normalized by the gate width W and shown on the vertical axes. Fig. 2(c) and (d) are for a partially-recessed FET ($d_{\text{AlGa}} \simeq 11$ nm, $d_{\text{AlTiO}} = 26$ nm). Figure 3(a) and (b) show capacitance-voltage (C - V) characteristics at 1 MHz of a non-recessed capacitor ($d_{\text{AlGa}} = 20$ nm, $d_{\text{AlTiO}} = 26$ nm) and a partially-recessed capacitor ($d_{\text{AlGa}} \simeq 11$ nm, $d_{\text{AlTiO}} = 26$ nm), respectively. The total electron number N under the gate is calculated by integration of C as a function of V_G , which is plotted in the same figure. The threshold voltage V_{th} can be determined by the N - V_G relation. For the non-recessed capacitors, V_{th} is determined by simple linear fitting with $qN \simeq C(V_G - V_{\text{th}})$ (q : the electron charge) for $V_G > V_{\text{th}}$ as in Fig. 3(a). On the other hand, since the recessed capacitors have the recessed area with the threshold voltage V_{th} and the non-recessed area with the threshold voltage $V_{\text{th0}} < V_{\text{th}}$, we obtain two lines $qN \simeq C_{\text{nr}}(V_G - V_{\text{th0}})$ for $V_{\text{th0}} < V_G < V_{\text{th}}$ and $qN \simeq C_{\text{nr}}(V_G - V_{\text{th0}}) + C_{\text{r}}(V_G - V_{\text{th}})$ for $V_G > V_{\text{th}}$ as in Fig. 3(b). Thus, the recessed device threshold voltage V_{th} is determined by the intersection point of the two lines [12].

III. LOW-FREQUENCY NOISE CHARACTERIZATION

The LFN measurement system consists of a shielded chamber for probe station, a battery-driven low-noise preamplifier (LNA, Stanford SR570), a dynamic signal analyzer (Agilent 35670A), and an RC passive low-pass filter (LPF). For measuring LFN in the MIS-FETs, the source is grounded, the drain is applied with a DC bias voltage and a DC offset current by the battery-driven LNA, and the gate is connected to a parameter analyzer through the LPF with a cut-off frequency ~ 0.05 Hz to eliminate the noise from the parameter analyzer [7, 21, 42]. The schematic of the LFN measurement setup is shown in Fig. 4. We measured LFN for each AlTiO/AlGa/GaN MIS-FET in the linear regime for a frequency range $f = 0.1$ - 10^3 Hz. In Fig. 5, we show examples of the measurement results of the drain current noise power spectral density (PSD) normalized by the drain current square, S_{I_D}/I_D^2 . In the well-above-threshold regime $V_G - V_{\text{th}} \gtrsim 3$ V, pure $1/f$ LFN spectra [43]

$$\frac{S_{I_D}}{I_D^2} = \frac{A}{f} \quad (1)$$

are observed, where A is a prefactor. On the other hand, near the threshold voltage, we find superposition of $1/f$ and Lorentzian spectra given by

$$\frac{S_{I_D}}{I_D^2} = \frac{A}{f} + \frac{B}{1 + (2\pi\tau f)^2}, \quad (2)$$

where B is a prefactor and τ is a time constant for the Lorentzian spectra. Since A and B respectively characterize the intensity of $1/f$ and Lorentzian noise, it is important to extract them from the measured spectra. We carried out fitting of S_{I_D}/I_D^2 using Eq. (2), which includes Eq. (1) as a special case of $B = 0$. Figure 6 shows examples of the fitting, where a current PSD in the well-above threshold regime is fitted by Eq. (2) with $B \simeq 0$, whereas a current PSD near the threshold voltage is well-fitted by Eq. (2) with $B \neq 0$.

From the fittings, we obtain A for all the spectra. In order to analyze A , we should consider the contributions from each region of the FETs. The on-resistance R_{on} for the non-recessed FETs is given by

$$R_{\text{on}} = 2R_c + R_{\text{ac}} + R_{\text{nr}} = R_{\text{ext}} + R_{\text{nr}}, \quad (3)$$

where R_c is the Ohmic contact resistance, R_{ac} is the resistance of the access region (total length $L_{\text{ac}} = 2.5 \mu\text{m}$), R_{nr} is the resistance of the non-recessed gated region (length $L_G = 2.5 \mu\text{m}$). For the partially-recessed FETs, the on-resistance is given by

$$R_{\text{on}} = 2R_c + R_{\text{ac}} + \tilde{R}_{\text{nr}} + R_r = R_{\text{ext}} + \tilde{R}_{\text{nr}} + R_r, \quad (4)$$

where $\tilde{R}_{\text{nr}}$ is the resistance of the non-recessed gated region (total length $L_G - L_{\text{RG}} = 0.5 \mu\text{m}$) and R_r is the resistance of the partially-recessed gated region (length $L_{\text{RG}} = 2 \mu\text{m}$). As a result, we obtain

$$\begin{aligned} A &= A_{\text{ext}} \frac{R_{\text{ext}}^2}{R_{\text{on}}^2} + A_{\text{nr}} \frac{R_{\text{nr}}^2}{R_{\text{on}}^2} & (\text{non-recessed FET}) \\ A &= A_{\text{ext}} \frac{R_{\text{ext}}^2}{R_{\text{on}}^2} + \tilde{A}_{\text{nr}} \frac{\tilde{R}_{\text{nr}}^2}{R_{\text{on}}^2} + A_r \frac{R_r^2}{R_{\text{on}}^2} & (\text{partially-recessed FET}). \end{aligned} \quad (5)$$

A_{ext} is the factor for the PSD generated by the external region, the Ohmic contact resistance and the access region, which is independent of V_G . A_{nr} is the factor for the non-recessed gated region depending on V_G for the non-recessed FETs. $\tilde{A}_{\text{nr}}$ and A_r are the factors for the non-recessed gated and the recessed gated regions for the partially-recessed FETs, respectively, which also depend on V_G . In order to determine the external factor A_{ext} , we measured LFN in the ungated non-recessed two-terminal devices, whose structure is shown in the inset of Fig. 7(a). Figure 7(b) shows $A_{\text{ext}} = S_I f / I^2$ as a function of the access length L , where A_{ext} can be fitted with a decreasing function of L as in the previous report [21], because

$$A_{\text{ext}} = 2A_c \frac{R_c^2}{R_{\text{ext}}^2} + A_{\text{ac}} \frac{R_{\text{ac}}^2}{R_{\text{ext}}^2} = \frac{2A_c R_c^2 + A_{\text{ac}} R_{\text{ac}}^2}{(2R_c + R_{\text{ac}})^2} \quad (6)$$

holds and the L dependence comes from $R_{ac} \propto L$ and $A_{ac} \propto 1/L$ (inversely proportional to the system size). For our FETs, since the access length is $L_{ac} = 2.5 \mu\text{m}$, we obtain $A_{\text{ext}} \simeq 4 \times 10^{-11}$, from which we can determine A_{nr} depending on V_G for the non-recessed FETs. Additionally, the length of non-recessed gated region in the partially-recessed FETs is $L_G - L_{\text{RG}} = 0.5 \mu\text{m}$, which is one-fifth of the length of non-recessed gated region in the non-recessed FETs ($L_G = 2.5 \mu\text{m}$). Hence, we obtain $\tilde{R}_{\text{nr}} = R_{\text{nr}}/5$ and $\tilde{A}_{\text{nr}} = 5A_{\text{nr}}$. As a result, we can extract A_r . In Fig. 8, A_{nr} and A_r are plotted as functions of $V_G - V_{\text{th}}$. We find that A_{nr} and A_r increase for low $V_G - V_{\text{th}}$, and approach constants at higher $V_G - V_{\text{th}}$.

The effective Hooge parameters α_H in the intrinsic region can be evaluated by [43]

$$\begin{aligned} \alpha_H &= A_{\text{nr}}N = A_{\text{nr}}n_sL_GW & (\text{non-recessed FET}) \\ \alpha_H &= A_rN = A_rn_sL_{\text{RG}}W & (\text{partially-recessed FET}), \end{aligned} \quad (7)$$

where n_s is the sheet electron concentration in the intrinsic region, which can be calculated from the electron number obtained by the C - V characteristics. Figure 9(a) and (b) plot α_H as functions of $V_G - V_{\text{th}}$ for the non-recessed FETs and the partially-recessed FETs. We find that α_H is independent of the AlTiO thickness but strongly dependent of the remaining AlGaIn layer; a smaller d_{AlGaIn} gives a larger α_H , although α_H seems to approach the same constant at high $V_G - V_{\text{th}}$. We evaluate α_H as a function of n_s for each FET in Fig. 10. We find that for $n_s \lesssim 2 \times 10^{12} \text{ cm}^{-2}$, $\alpha_H \propto n_s^{-1}$ for the partially-recessed FETs, whereas α_H is weakly dependent on n_s for the non-recessed FETs. The behavior of $\alpha_H \propto n_s^{-1}$ was observed for example in Schottky FETs [44], and can be attributed to the electron number fluctuation caused by electron traps. The trap density D_0 can be estimated by the relation [21, 43, 45]

$$\alpha_H \simeq \frac{k_B T D_0}{n_s \ln(f_h/f_l)}, \quad (8)$$

where f_l and f_h are the lower and higher limits of the $1/f$ spectrum, respectively. Thus, we obtain $D_0 \sim 3 \times 10^{11}$ and $\sim 5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ for the partially-recessed FETs with $d_{\text{AlGaIn}} \simeq 5$ and $\simeq 11 \text{ nm}$, respectively. We consider that the recess etching process may introduce electron traps in the AlGaIn layer, the longer the etching process is carried out, the smaller the remaining AlGaIn thickness is, and the higher the trap density becomes. This might also explain the weak dependence of α_H on n_s for the non-recessed FETs, since the trap density is too low to have a pronounced effect as observed in the partially-recessed FETs. On the other hand, at high n_s , we observe a strong, universal increase in α_H for all

the FETs, which can be attributed to the fluctuation in the intrinsic gate voltage through the extrinsic source resistance [21].

In general, Lorentzian LFN strongly depends on the gate insulator quality, such as traps [7, 21]. In the present case, from the fittings, we obtain the prefactor B and the time constant τ in Eq. (2) for all the FETs as shown in Fig. 11, where B and τ are plotted as functions of $V_G - V_{th}$. It seems that B is almost independent of the AlTiO thickness and the remaining AlGaIn thickness. Furthermore, B rapidly decreases with increase in $V_G - V_{th}$ and becomes negligible in the well-above threshold regime. The extracted specific time constant, $\tau \sim 0.5$ s, seems to be almost independent of $V_G - V_{th}$, the AlTiO thickness, and the remaining AlGaIn thickness. The time constant τ corresponds to a trap level depth E_a via

$$\tau = \frac{1}{\sigma_e N_c v_{th}} e^{E_a/k_B T}, \quad (9)$$

where σ_e is the electron capture cross-section, N_c is the effective density of states in the conduction band, v_{th} is the electron thermal velocity, and k_B is the Boltzmann constant. We assume $\sigma_e = 10^{-16}$ - 10^{-14} cm² for the traps in AlTiO; this is reasonable since ALD Al₂O₃ shows similar σ_e [46], while much smaller σ_e was observed in SiN [47]. An electron effective mass should be between $m^* = 0.3m_e$ for Al₂O₃ [48] and $m^* = 30m_e$ for TiO₂ [49]. Thus, the trap depth can be estimated to be $E_a \simeq 0.6$ - 0.8 eV. The fact that B and τ are almost independent of the remaining AlGaIn thickness and the AlTiO thickness suggests that the Lorentzian spectra are attributed to traps in AlTiO near the AlTiO/AlGaIn interface.

IV. COMPARISON WITH POOLE-FRENKEL CURRENTS

Since the Poole-Frenkel analysis is effective to examine the traps in AlTiO, we investigated gate leakage currents of the MIS capacitors. Figure 12(a) and (b) show the gate leakage current density J as a function of V_G at reverse bias at $T = 300$ - 400 K for a non-recessed capacitor ($d_{AlGaIn} = 20$ nm, $d_{AlTiO} = 26$ nm) and a partially-recessed capacitor, ($d_{AlGaIn} \simeq 11$ nm, $d_{AlTiO} = 26$ nm), respectively. Leakage dominated by the Poole-Frenkel mechanism is given by [50]

$$\frac{J}{F} = D e^{-\beta \phi} e^{\beta \sqrt{q^3 F / (\pi \kappa \epsilon_0)}}, \quad (10)$$

where F is the electric field in the AlTiO insulators, $\beta = 1/k_B T$, D is a constant, ϕ is the trap level depth in the AlTiO, κ is related to the dielectric constant, and ϵ_0 is the vacuum

permittivity. The electric field can be evaluated by [7]

$$F = \frac{\Delta\sigma_{\text{ins}} - qn_s}{k_{\text{AlTiO}}\epsilon_0}, \quad (11)$$

where $\Delta\sigma_{\text{ins}} = \sigma_{\text{ins}} - \sigma_{\text{GaN}}$ is the difference between the fixed charge density σ_{ins} at AlTiO/AlGaN interface and the GaN polarization charge density σ_{GaN} , and k_{AlTiO} is the insulator dielectric constant. Based on measurements of MIS capacitors with several insulator thicknesses and 1D Poisson-Schrödinger calculation [9, 11, 12], we find that $\Delta\sigma_{\text{ins}} \simeq 4 \times 10^{12}$ and $2 \times 10^{12} \text{ cm}^2$ for the non-recessed and partially-recessed capacitors, respectively. Figure 13(a) and (b) show $J/F\sqrt{F}$ relations for the non-recessed and partially-recessed capacitors, respectively, exhibiting the leakage dominated by the Poole-Frenkel mechanism according to Eq. (10) in the high field regime. From the fittings, we obtain $D \exp(-\beta\phi)$ as a function of $1/T$, which is plotted in Fig. 13(c). The trap level depth in the AlTiO insulator is extracted to be $\phi \simeq 0.6 \text{ eV}$, which is independent of the remaining AlGaN thickness as expected, and similar to the one obtained from the Lorentzian spectra. This suggests that the traps in the AlTiO insulator are responsible for the Lorentzian LFN and the Poole-Frenkel mechanism. It should be noted that the Poole-Frenkel mechanism is caused by the whole of the bulk traps in the AlTiO insulator. On the other hand, since the Lorentzian noise is not influenced by the AlTiO thickness and the electric field or the gate voltage, we consider that the traps in AlTiO contributing the Lorentzian noise are those near the AlTiO/AlGaN interface, where the trap density might be high.

V. CONCLUSION

We investigated LFN in AlTiO/AlGaN/GaN MIS-FETs with non-gate-recessed or partially-gate-recessed structures. From drain current LFN characterization, we find pure $1/f$ spectra for the well-above-threshold regime, and superposition of $1/f$ and Lorentzian spectra near the threshold voltage. The Hooge parameters are evaluated from the $1/f$ contribution and found to be independent of the AlTiO thickness, but strongly dependent of the remaining AlGaN thickness near the threshold voltage. The Hooge parameters are proportional to the inverse of the channel electron concentration at low concentrations, dominated by the channel electron number fluctuation, which can be attributed to electron traps introduced by the recess etching process in the remaining AlGaN. On the other hand, the

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Lorentzian spectra are almost independent of the AlTiO thickness and the remaining Al-GaN thickness. Comparing with the gate leakage currents dominated by the Poole-Frenkel mechanism due to traps in AlTiO, we consider that the Lorentzian spectra are attributed to traps in AlTiO near the AlTiO/AlGaN interface.

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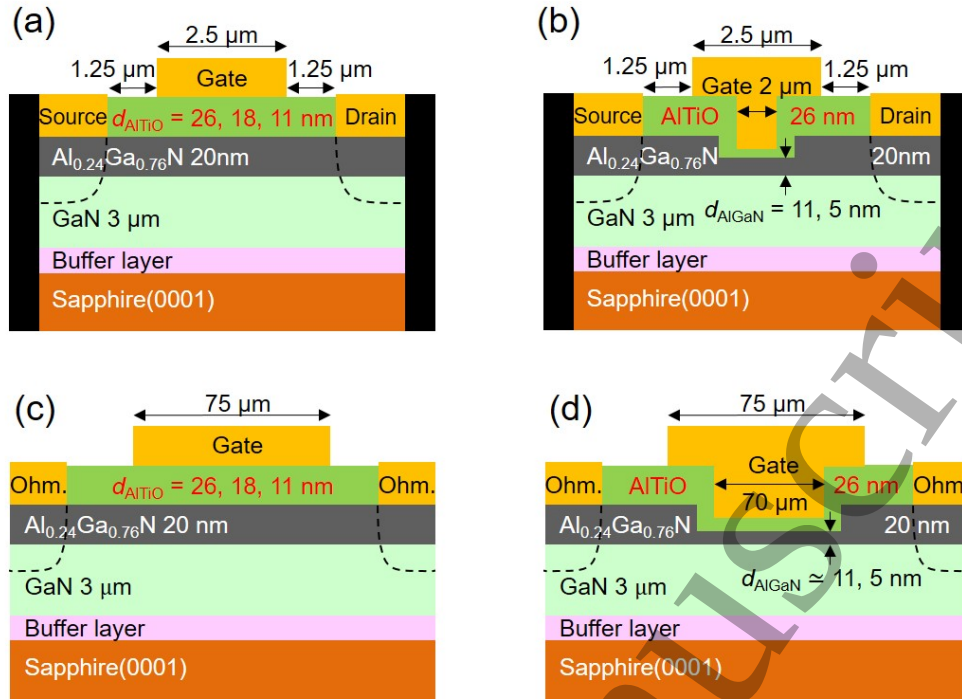


FIG. 1: The dimension of (a) non-recessed and (b) partially-recessed AlTiO/AlGaN/GaN MIS-FETs, and (c) non-recessed and (d) partially-recessed AlTiO/AlGaN/GaN MIS capacitors. The non-recessed devices have the remaining AlGaN thickness of $d_{\text{AlGaN}} = 20$ nm, and AlTiO thicknesses of $d_{\text{AlTiO}} = 26, 18$, and 11 nm. The partially-recessed devices have remaining AlGaN thicknesses of $d_{\text{AlGaN}} \approx 11$ and 5 nm, and an AlTiO thickness of $d_{\text{AlTiO}} = 26$ nm.

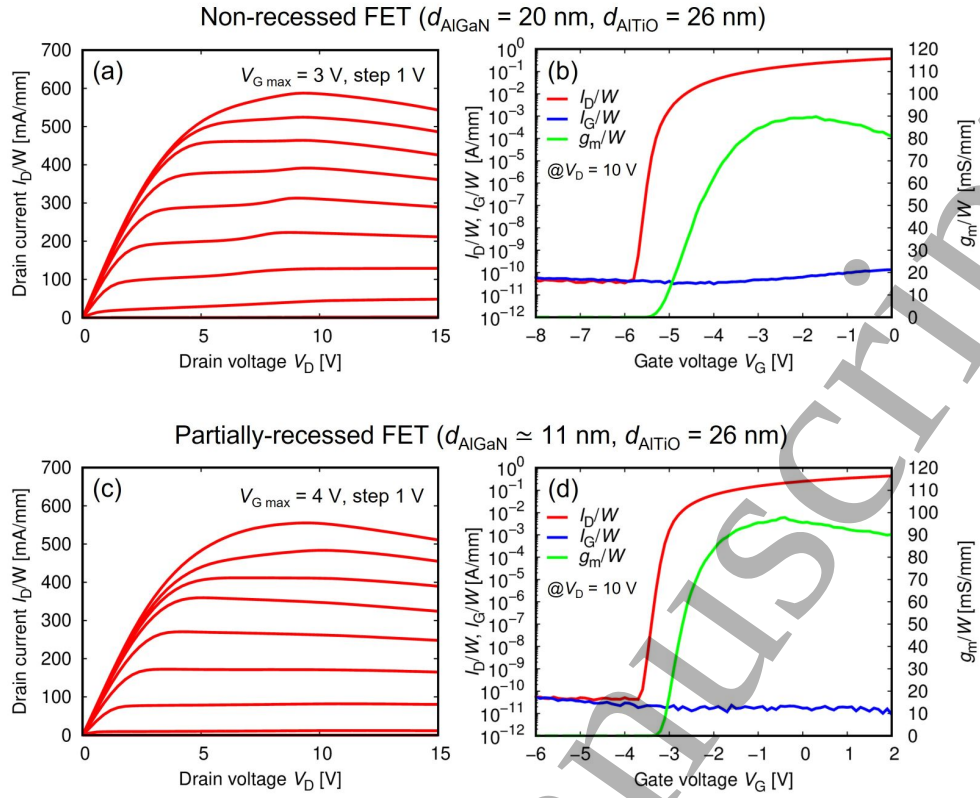


FIG. 2: Device characteristics of FETs with the gate length $L_G = 2.5 \mu\text{m}$ and the gate width $W = 50 \mu\text{m}$. (a) Output and (b) transfer characteristics for a non-recessed FET ($d_{\text{AlGaN}} = 20 \text{ nm}$, $d_{\text{AlTiO}} = 26 \text{ nm}$). (c) Output and (d) transfer characteristics for a partially-recessed FET ($d_{\text{AlGaN}} \approx 11 \text{ nm}$, $d_{\text{AlTiO}} = 26 \text{ nm}$). I_D is the drain current, I_G is the gate current, and g_m is the transconductance, which are normalized by W and shown on the vertical axes.

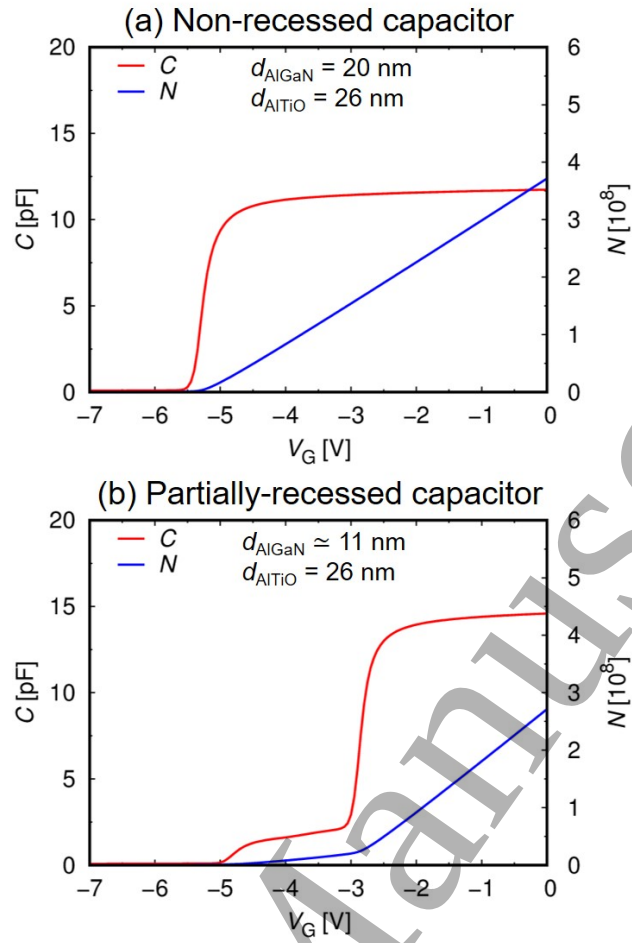


FIG. 3: The C - V characteristics of (a) a non-recessed capacitor ($d_{\text{AlGaN}} = 20$ nm, $d_{\text{AlTiO}} = 26$ nm) and (b) a partially-recessed capacitor ($d_{\text{AlGaN}} \approx 11$ nm, $d_{\text{AlTiO}} = 26$ nm). The carrier number N is calculated by integrating C as a function of V_G .

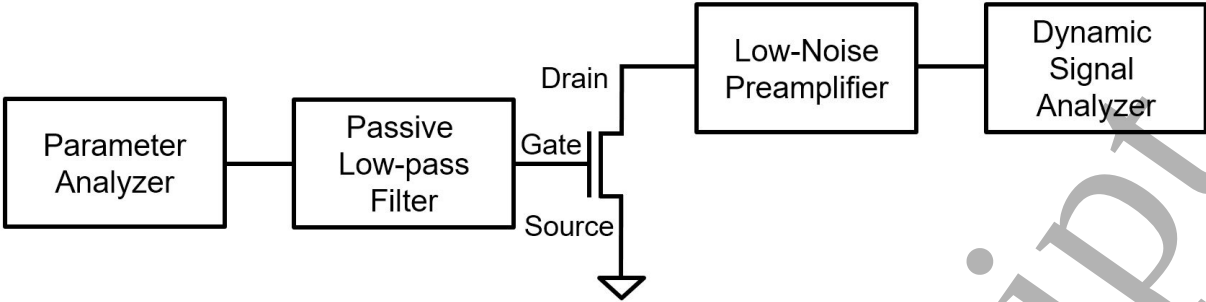


FIG. 4: The schematic of the LFN measurement setup. A low-noise preamplifier (Stanford SR570), a dynamic signal analyzer (Agilent 35670A), and an RC passive low-pass filter (cut-off frequency ~ 0.05 Hz) are used. The FET gate is connected to a parameter analyzer through the low-pass filter to eliminate the noise from the parameter analyzer.

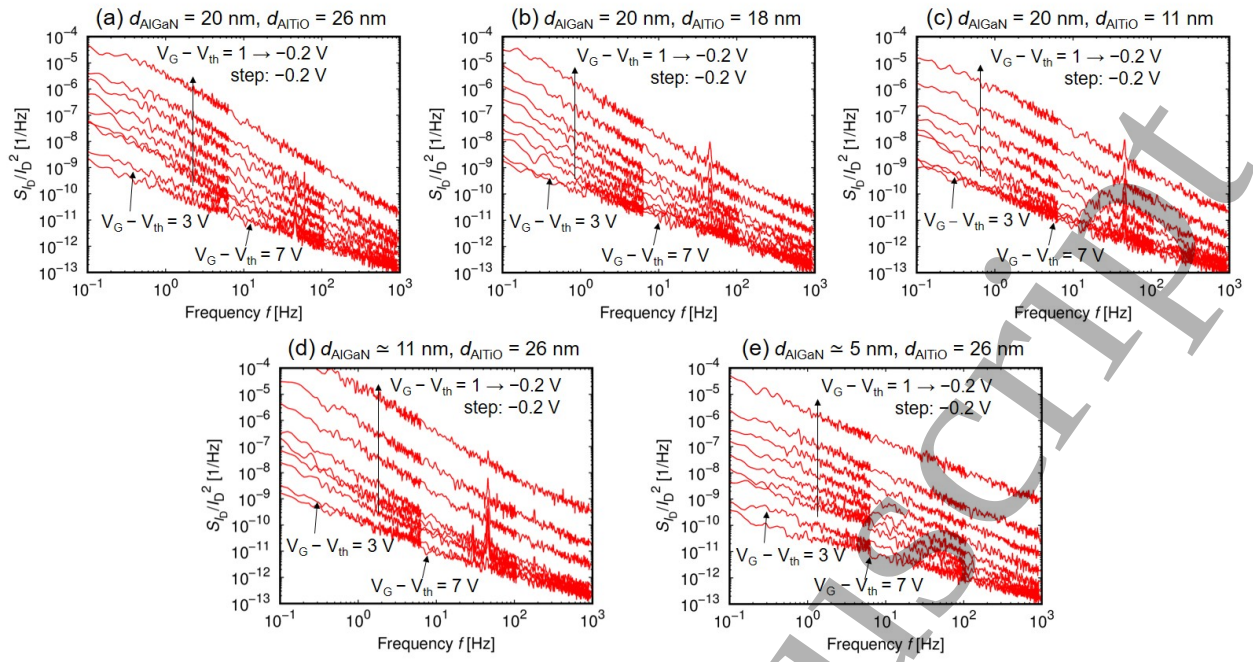


FIG. 5: Examples of LFN spectra normalized by the drain current square, S_{I_D}/I_D^2 , for the non-recessed FETs (a), (b), and (c), and the partially-recessed FETs (d) and (e).

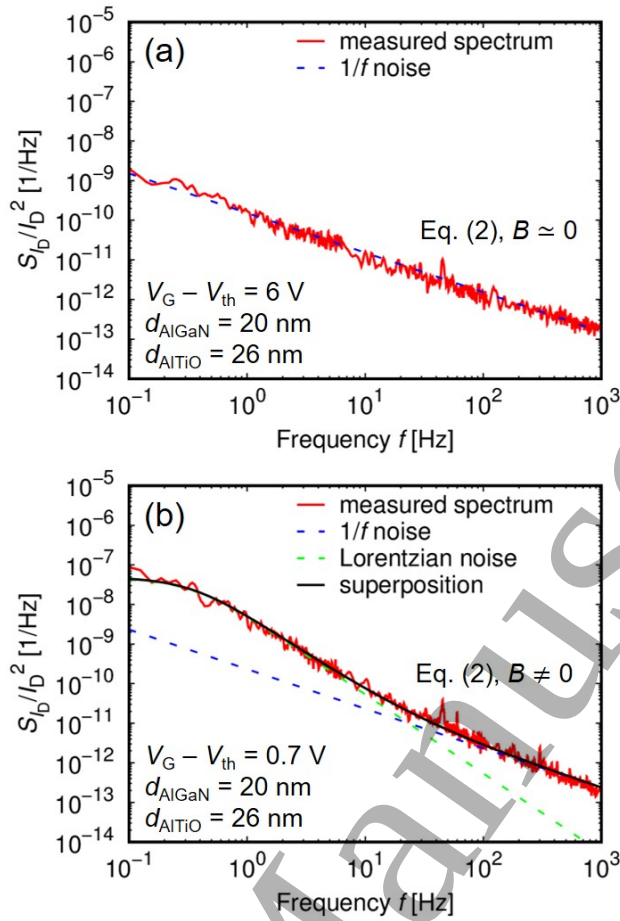


FIG. 6: Examples of fitting of current PSD (a) in the well-above threshold voltage regime using Eq. (2) with $B \simeq 0$, and (b) near the threshold voltage using Eq. (2) with $B \neq 0$.

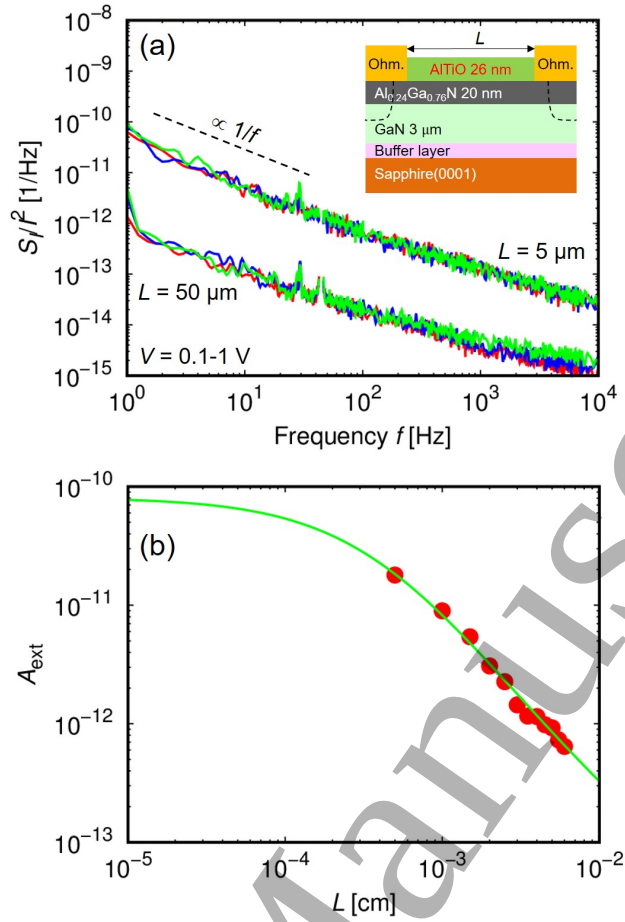


FIG. 7: (a) LFN spectra of the AlTiO/AlGa_N/Ga_N ungated 2T devices (the inset). (b) A_{ext} depending on the access length.

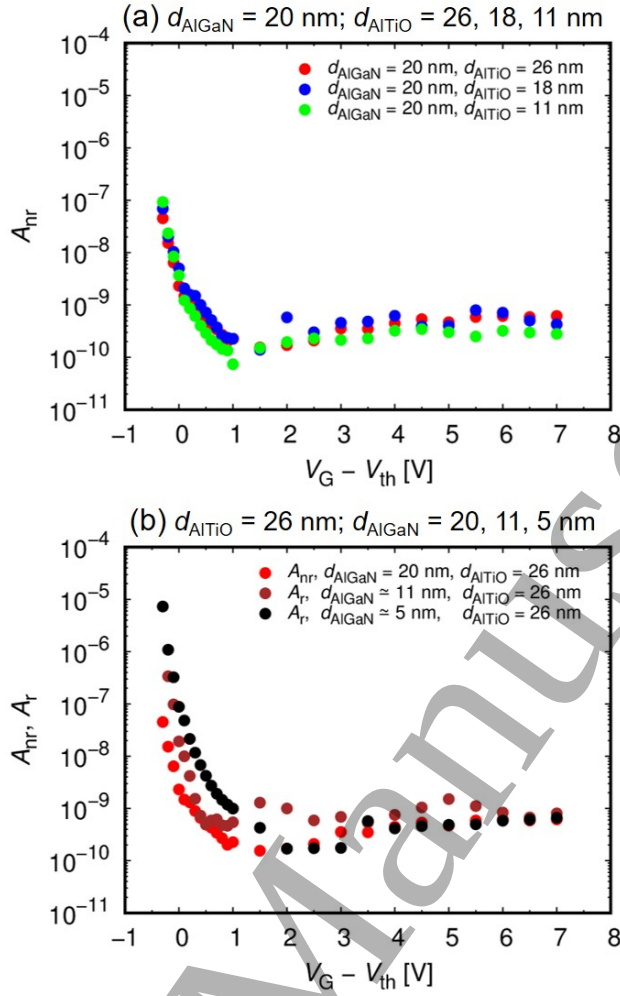


FIG. 8: A_{nr} of the non-recessed FETs and A_r of the partially-recessed FETs as functions of $V_G - V_{th}$.

(a) $d_{AlGaN} = 20$ nm; $d_{AlTiO} = 26, 18, 11$ nm. (b) $d_{AlTiO} = 26$ nm; $d_{AlGaN} = 20, 11, 5$ nm.

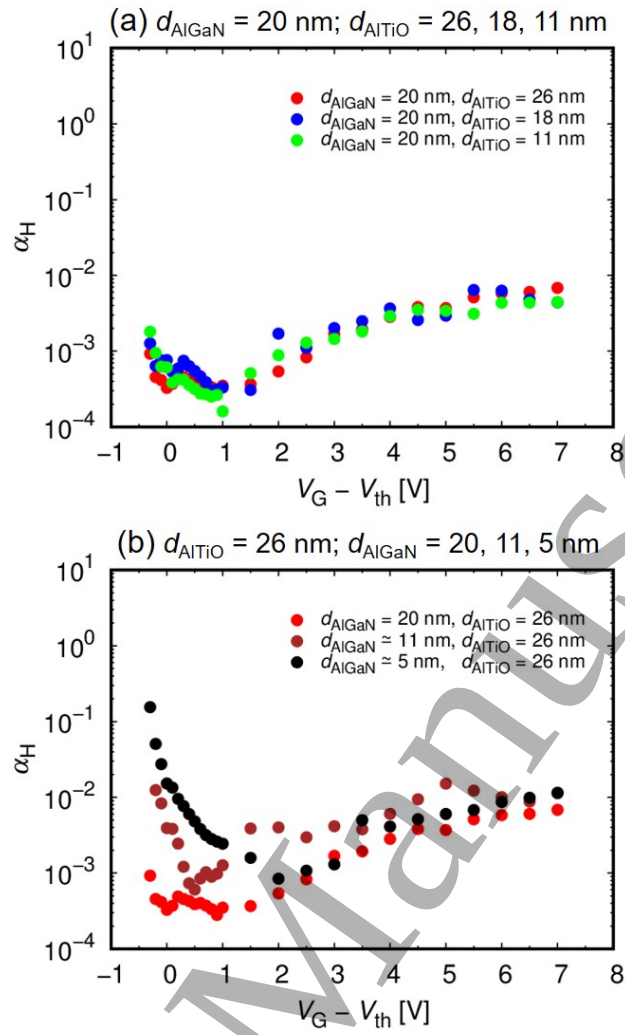


FIG. 9: Hooe parameters α_H of the non-recessed FETs and the partially-recessed FETs as functions of $V_G - V_{th}$. (a) $d_{\text{AlGaN}} = 20 \text{ nm}; d_{\text{AlTiO}} = 26, 18, 11 \text{ nm}$. (b) $d_{\text{AlTiO}} = 26 \text{ nm}; d_{\text{AlGaN}} = 20, 11, 5 \text{ nm}$.

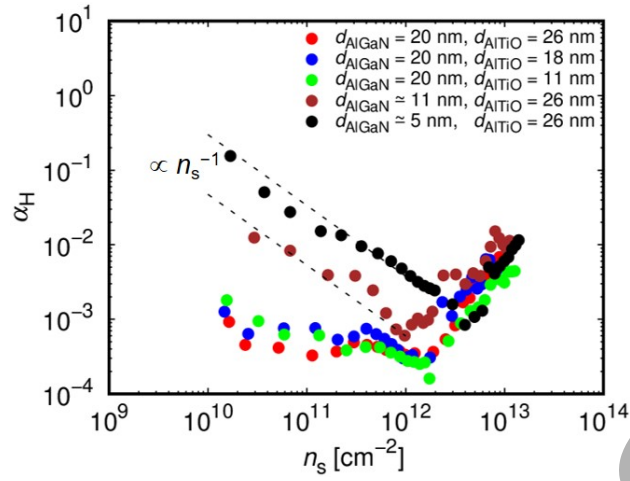


FIG. 10: The Hooge parameter α_H of each FET as a function of the sheet electron concentration n_s .

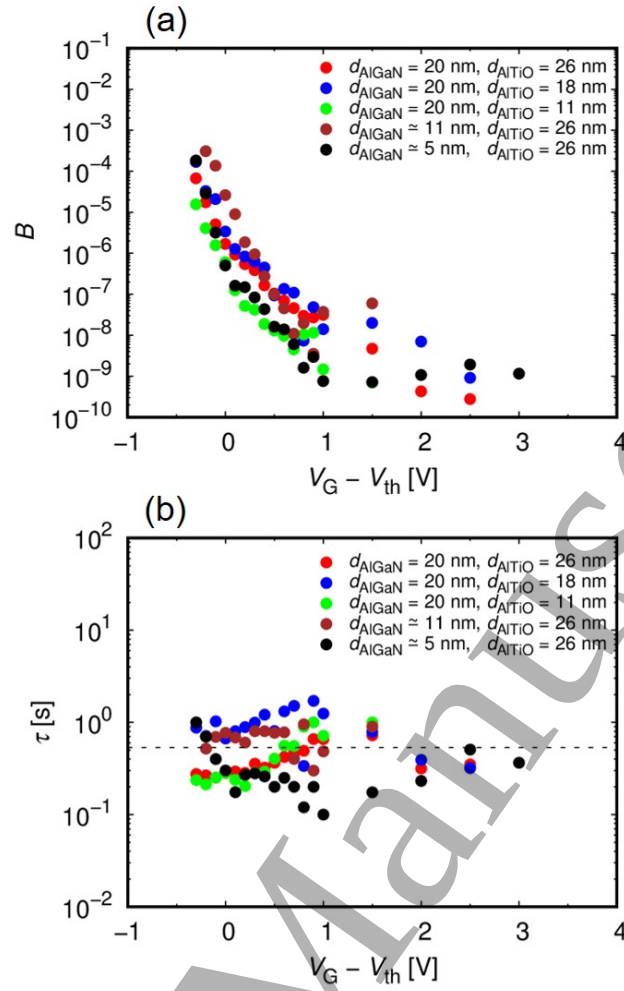


FIG. 11: (a) The prefactor B and (b) the time constant τ for the Lorentzian spectra as functions of $V_G - V_{th}$.

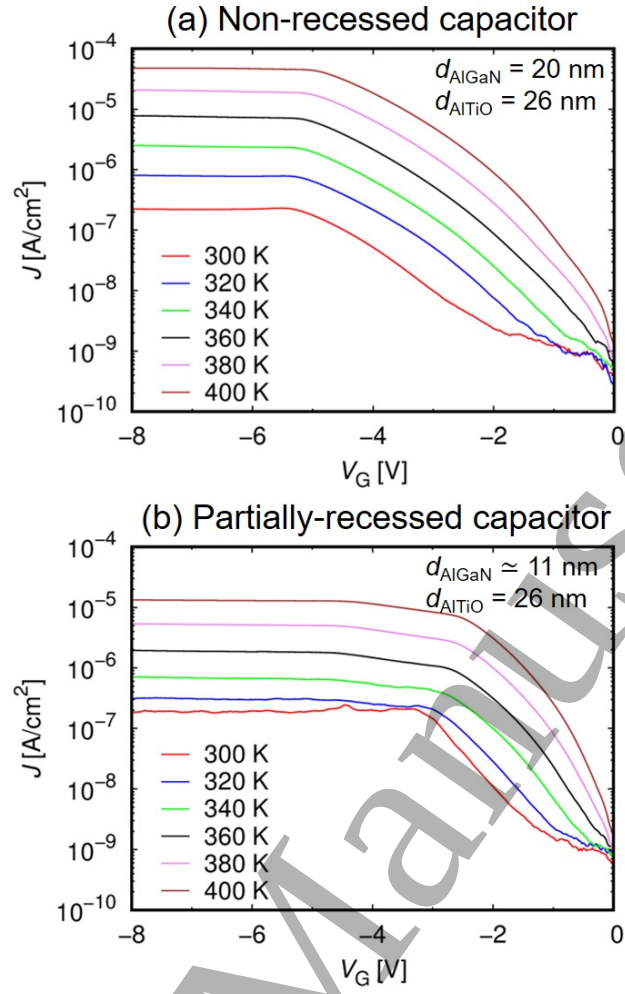


FIG. 12: The gate leakage current density J as a function of V_G at $T = 300\text{-}400 \text{ K}$ for (a) the non-recessed capacitor and (b) the partially-recessed capacitor.

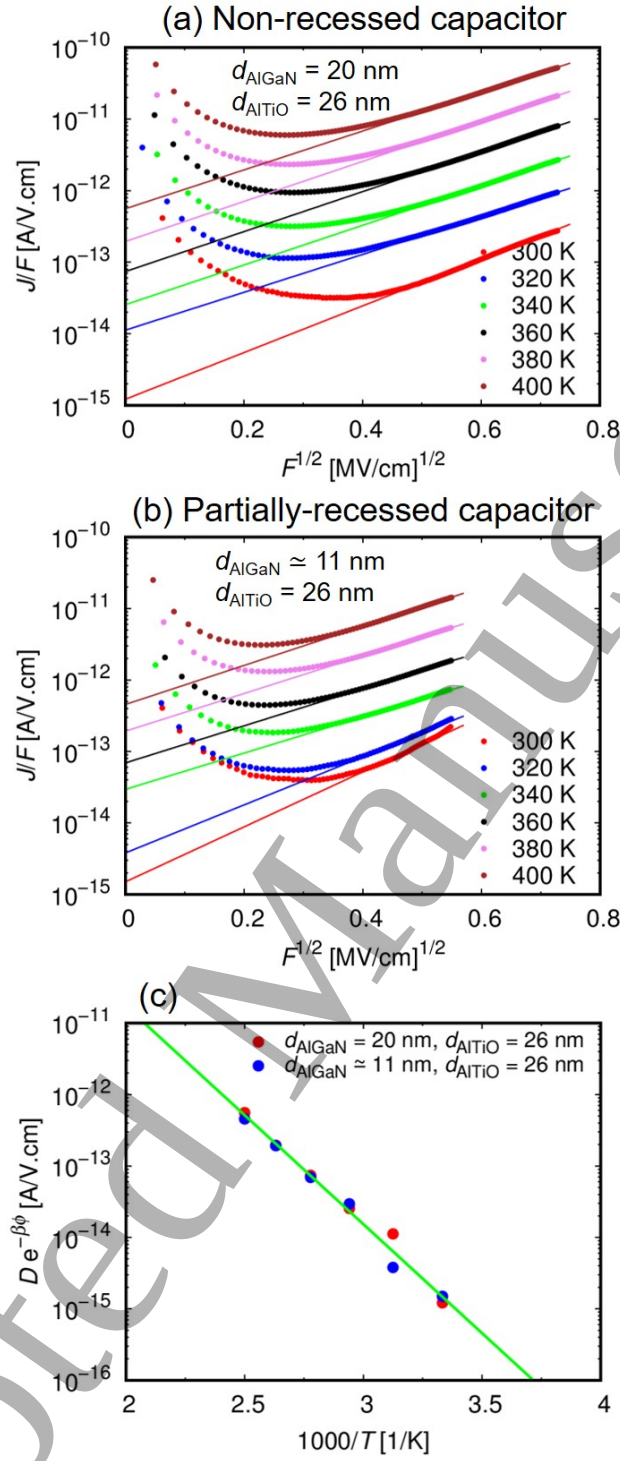


FIG. 13: Poole-Frenkel plots ($J/F\sqrt{F}$) for (a) the non-recessed capacitor and (b) the partially-recessed capacitor. (c) $D \exp(-\beta\phi)$ as a function of $1/T$ with a fitting line.

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