Nano-Scale Metal Transistor Controlling Fowler-Nordheim Tunneling Currents through 16 nm Insulating Channel

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A nano-scale transistor, the metal/insulator tunnel transistor (MITT) with a channel length of only 16 nm, is fabricated by conventional photolithography, and its operation is experimentally studied. The MITT consists of two metal electrodes, the insulating channel inserted laterally between these two electrodes and the third metal gate-electrode formed upon the gate insulator over the insulating channel. The Fowler-Nordheim (F-N) tunneling currents flowing from one metal electrode to the other through the insulating channel are controlled by applying a voltage to the gate electrode. It is found that the MITT can be operated similarly to the semiconductor transistor, and the feasibility of a nano-scale metal transistor is demonstrated.

1 Introduction

The conventional metal/oxide/semiconductor field-effect transistor (MOSFET) has physical and technological limits for sub-micron fabrication.[1] Thus, a nanometer scale transistor operating by a new principle is strongly desired to realize even higher package density of ultra large scale integrated circuits (ULSI). As one of the alternative candidates of MOSFET, the metal/insulator tunnel transistor (MITT), consisting of the metal and insulator without the semiconductor, has been proposed by our group in 1996.[2]

The structure of MITT is briefly illustrated in Fig. 1. A nanometer-scale insulating region, named the tunnel insulator is formed between the metal source and drain electrodes. Just above the tunnel insulator, the gate electrode is formed upon the gate insulator.

In the MITT, the Fowler-Nordheim (F-N) tunneling currents[3] flowing through the tunnel insulator can be controlled by the gate voltage, just as in a conventional MOSFET, since the potential profile near the interface between the metal source electrode and the tunnel insulator is distorted by the electric field from the gate electrode. This is illustrated in Fig. 2, and a detailed explanation appears in reference.[2] The notation ϕ_B and E_F refer to the barrier height and the Fermi energy, respectively.

When the gate electrode is positively biased toward the source electrode, the potential profile at the source-insulator interface is distorted to make the profile even sharper. It is known that F-N tunneling currents are strongly affected by the barrier width through which electrons have to pass. Thus, the F-N tunneling currents can be increased by applying a positive gate bias.

The advantages of MITT are as follows: 1) Since the channel length can be reduced to around 15 nm by using F-N tunneling currents and also since the metal electrodes are directly connected to metal-signal lines, the MITT requires only a nano-scale area for transistor action. 2) An α-ray soft error and radiation damage do not occur at all, since the MITT is made of metal and the insulator without semiconductor. 3) The MITT can be fabricated by a much simpler fabrication process than that of semiconductor devices because the formation of the p-n region is not necessary. 4) High speed operation of the order of pico-seconds is realized, since all signal lines and the electrodes are made of metal, and the drain currents also flow by tunneling phenomena. 5) The insulating channel of MITT is about ten times more tolerable in applying the electric field than the semiconductor channel of MOSFET, since the insulator has about ten times larger dielectric strength than the semiconductor. This is useful for nano-scale devices. 6) In the MITT, it is easy to fabricate three-dimensional circuits by stacking the two-dimensional ones, since the MITT does not require to use crystalline materials in the fabrication process.

Recently, a new technology using the tip of scanning tunnel microscopy has been reported to fabricate nanometer devices.[4,5] E. S. Snow et al.[6] succeeded in fabricating the MITT by using this technology based on our previous suggestion.[2] Their work is useful in checking the fundamental physics in device operation. However, the technology does not appear to be industrially acceptable. Thus, the fabrication of MITT by using conventional technology such as photolithography is strongly required.

The purpose of this paper is to demonstrate the validity of our proposal regarding the MITT through its fabrication using industrially acceptable technology. The MITT with a channel length of 16 nm is fabricated by using only conventional photolithography and its operation is verified. The results clearly demonstrate that the size of transistor can be drastically minimized to the ten nanometer scale by using the MITT instead of semiconductor transistors. Moreover, the MITT can be fabricated by a simple method because the formation of a p-n region is not necessary.

2 Experimental Procedure

1 Fabrication Process

Figure 3 shows the present fabrication process of the MITT using conventional photolithography. The MITT is fabricated as follows[7,8]: 1) The gate insulator and a field insulator are formed by thermal oxidation on an n-type silicon substrate as a gate electrode. 2) A Ti film is evaporated on the gate insulator and the edge of the photoresist is aligned over the gate insulator by using photolithography. 3) The sidewall of Ti under the photoresist is steeply cut by the reactive ion etching (RIE) using chlorine (Cl_2) and boron trichloride (BCl_3) mixture. 4) The sidewall of Ti is anodized in ethyleneglycol dissolved ammonium-tetraborate. 5) A Ti film is evaporated again, upon both the photoresist and the anodized TiOx. 6) A Ti film above the photoresist is removed by lift-off technology, and finally the fabrication of MITT is completed.

The detailed conditions for fabrication of MITT is summarized in Table I. This fabrication process indicates the possibility of fabricating nano-scale MITT by using only conventional photolithography.

3 Transistor Characteristics

The experimentally obtained transfer characteristics are demonstrated in Fig. 4 at 90 K because the drain currents due to the Poole-Frenkel currents are negligible. The structure of the transistor is described in the inset. In this particular case, the length of the tunnel insulator is 16 nm and the thickness of the gate insulator is 10 nm.

This graph shows that the source-drain currents (I_{ds}) are controlled from 10^{-12} A to 10^{-7} A by the gate voltage (V_g) changing from -4 V to +4 V. When V_g is smaller than -2.0 V, the F-N tunneling currents due to applying the drain voltage (V_{ds}) of 3 V are suppressed by the negative gate bias as described in Fig. 4. Of course, it is confirmed that the gate-leakage currents of the order of picoamperes have nothing to affect on the change of I_{ds}. I_{ds} are clearly increased by changing the gate voltage in the scale of 10^5 enough to transfer the signal in the logic circuits.

Figure 5 shows the I-V characteristics of MITT. It is found from this graph that I_{ds} with some fluctuations are slightly saturated by applying the gate voltage of 4.0 V. It is expected that these fluctuations are caused by flowing large I_{ds} through the tunnel insulator. It is also found that the threshold voltage is around -1.0 V.

It is surely confirmed from these results that the operation of MITT is similar to that of conventional MOSFET.

4 Conclusion

It is concluded that the operation of the MITT is similar to that of conventional MOSFET. The MITT fabricated by the conventional photolithography is the promising candidate for the future switching transistor in ULSI.

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Table I: The condition of fabrication process.

RIE condition	
Power of RIE	17.5 mW/cm^2
Flow rate of Cl_2	9.0 sccm
Flow rate of BCl_3	1.0 sccm
Gas pressure	1.0 Pa

Anodic oxidation	
Temperature	25 °C
pH	6.9

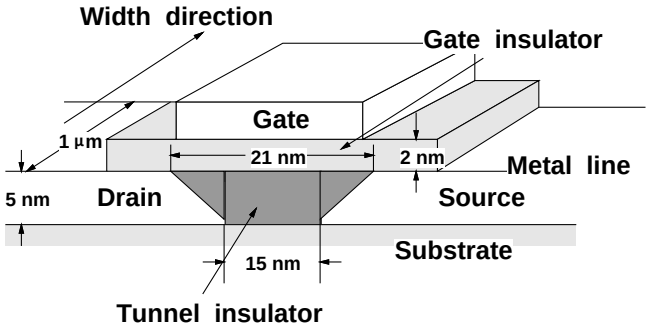

Figure 1. Schematic view of structure of metal/insulator tunnel transistor (MITT).

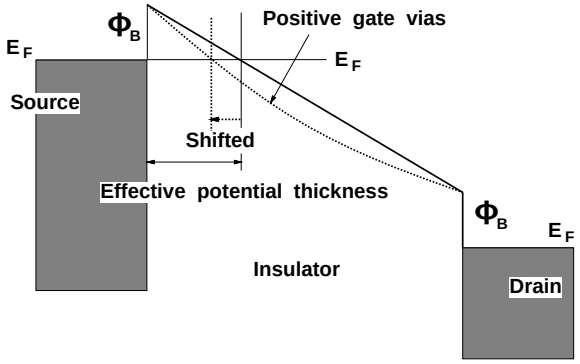

Figure 2. Energy band diagram of source/tunnel insulator/drain in the MITT.

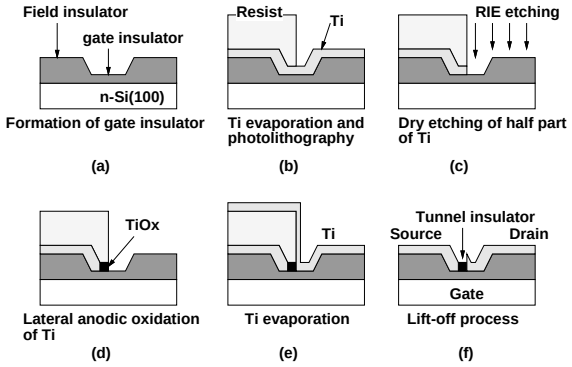

Figure 3. Fabrication process of MITT.

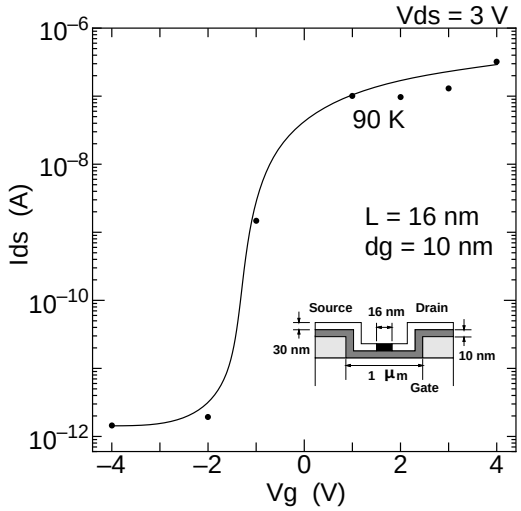

Figure 4. Experimentally obtained transfer characteristics of MITT at 90 K.

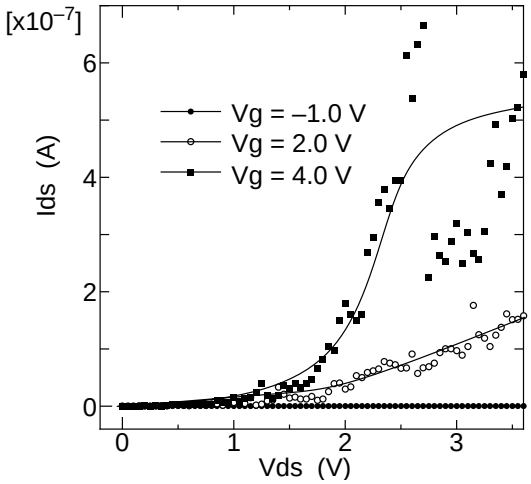

Figure 5. I-V characteristics of MITT.

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Note: the thesis is written in Japanese.

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