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# Study on a new ferroelectric gate field effect transistor memory with an intermediate electrode for data writing

## Introduction:

A field effect transistor with a gate of ferroelectric material (F-FET) has been invented in 1963. Recently, many efforts have been made to put the memory into practical because it has a potential to satisfy requirements of non-destructive readout, high operation speed and high packing density for the near future memory devices. F-FET operates based on the phenomenon that the positive or negative charges are induced in the FET channel depending on the direction of permanent polarization in the ferroelectric film. The writing voltage alters the direction of polarization, which in turn modifies the channel conduction. By detecting the drain current which depends on the channel conduction at a given drain voltage, the memory state is decoded. Thus, F-FET lies within a simple cell structure like a conventional FET and has high operation speed because the channel is already formed before reading. However, F-FET has not been extensively commercialized yet due to some serious technology difficulties. The first problem is the generation of depolarization field in the ferroelectric film due to the present of a buffer layer between the ferroelectric film and Si substrate. The buffer layer must be inserted in order to prevent the chemical reaction between the ferroelectric film and Si. This depolarization field makes the polarization relaxed with time, leading to a short retention time of the memory. The second is the high operation voltage due to voltage dropped on the buffer layer, which means high power consumption. To minimize the high operation voltage, a high dielectric constant material (high-k material) is used as a buffer layer so that the capacitance of the buffer layer is high and the voltage drop on it is reduced. Unfortunately, this causes an unstable performance of the memory operation because of the poor interface of Si with the high-k material buffer layer. In order to overcome these problems, although many efforts have been being made, but no successful solution has been reported.

The purpose of the thesis is to propose and investigate a new operational principle for the F-FET with an intermediate electrode for data writing to improve the serious problems of conventional F-FET memory and to show its usefulness for future memory device. After that, we fabricate a demonstrative structure of the memory using 10 μm rule.

## Operational principle and theoretical investigation of the memory operation:

The basic structure of the new memory is schematically shown in the Fig. 1. The memory consists of a ferroelectric capacitor $C_f$ connected in series to the gate of a metal-oxide-semiconductors-field-effect transistor (MOSFET). This MOSFET is called reading MOSFET (R-FET). The writing voltage $V_W$ is applied to $C_f$ between the top and intermediate electrodes. For data reading, a reading voltage $V_R$ is applied between the top electrode and the source of the MOSFET in series. The new ferroelectric memory operates based on the non-linear capacitance of the $C_f$ when it is positively or negatively polarized. A typical polarization-electric field (P-E) hysteresis loop is plotted in Fig. 2. The $C_{fl}$ and $C_{fh}$ are ferroelectric capacitances of the $C_f$ when it is positively or negatively polarized by a positive or negative writing voltage $\pm V_W$. $C_{fl}$ is much smaller than $C_{fh}$ when the ferroelectric $V_f$ increases from 0 to positive direction during a reading. For data writing, a positive or negative writing voltage $V_W$ is applied only to the $C_f$. For data reading, a positive reading voltage $V_R$ is applied to both $C_f$ and the R-FET. At a given $V_R$, the intermediate voltage $V_I$ between the source and gate of the R-FET (gate voltage of R-FET) depends on the value of $C_f$ as well as input capacitance $C_0$ of the R-FET. $C_0$ hardly depends on voltage. If the ferroelectric capacitor is polarized by a negative writing voltage, $C_f$ is $C_{fh}$. Because $C_f$ and $C_0$ are connected in series, only a small portion of $V_R$ is applied to $C_f$ leading to a high $V_I$ in this case and, consequently, a large drain current $I_D$. On the contrary, if the ferroelectric capacitor is polarized by a positive writing voltage, $C_f$ is $C_{fl}$. Therefore, $V_I$ is low in this case and, consequently, a small or even no $I_D$ is obtained. By detecting the $I_D$ and comparing it to a reference, the memory states will be decoded.

In case of full integration circuit, an additional MOSFET is needed to electrically short the gate electrode of the R-FET. The additional MOSFET is termed writing MOSFET (W-FET). The schematic integrated circuit of the memory is given in Fig. 3. The W-FET connects the gate of R-FET to the bit line. An additional world line is needed to control the W-FET. The configuration with the W-FET connected from the intermediate electrode to the source of the R-FET is termed source-connected configuration (SCC). For data

writing, the W-FET is turned on by biasing the additional word line high, $V_W$ is applied only to $C_f$. Then, this line becomes low and W-FET is turned off. This is data retention. For data reading, $V_R$ is applied to both $C_f$ and R-FET in series, W-FET being OFF.

Generally, the resistance of a MOSFET in OFF state is extremely high but apparently finite. Therefore, for the SCC, a small leakage current from the intermediate electrode to the ground is unavoidable. This leakage current may discharge the induced charge in the intermediate electrode. Consequently, the intermediate voltage $V_I$ is decreased with reading cycles, leading to a short read endurance. To overcome this problem, a new configuration of the memory is proposed. In the new configuration, the W-FET is changed to connect from the intermediate electrode to the drain of the R-FET. This configuration is termed as drain-connected configuration (DCC). The schematic integration circuit of the DCC is given in Fig. 3 (dashed lines). The drain bias voltage $V_D$ suppresses the leakage current of W-FET during $V_I > V_D$ for $V_R$ = high and compensates the charge loss during $V_I < V_D$ during $V_R$ = 0. By this way, it is expected that the read endurance will be improved.

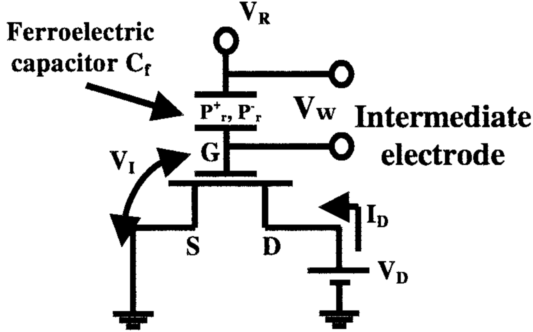


**Fig. 1:** Basic structure of the new memory. $C_f$ is a ferroelectric capacitor and will be polarized to the positive $P^+_r$ or negative $P^-_r$ remanent polarizations.

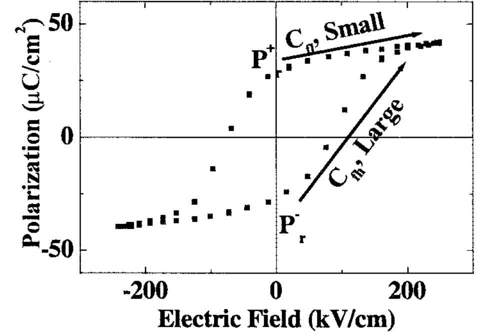


**Fig. 2:** A typical polarization – electric field of a ferroelectric capacitor of 200-nm epitaxial PZT film as ferroelectric material.

Therefore, the new F-FET memory can improve the serious problems of conventional F-FET. Firstly, the memory can operates at low write and read voltage due to no voltage drop on the insulating buffer layer and it's not necessary to saturate the $C_f$ during reading. Secondly, with the intermediate electrode, it is possible to keep both sides of the $C_f$ at the same potential (normally at ground) so that no depolarization field is generated during retention. Also, $SiO_2$ film can be used instead of high-k material to improve the stability of performance.

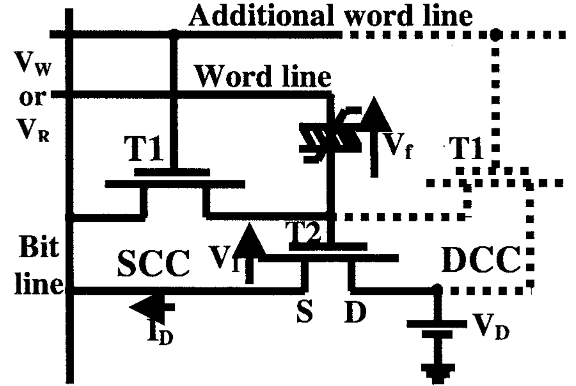


**Fig. 3:** Integrated circuit of the new memory. T1 and T2 are W-FET and R-FET, SCC and DCC are the source-connected and drain-connected configurations.

The intermediate voltage $V_I$ and the difference between threshold reading voltages $\Delta V_{TR}$ which gives a guideline for fabrication of $C_f$ have been theoretically calculated. For a linear analysis, the whole range of reading cycle is divided to M regions with linear system. Within the $i^{th}$ region with $N_i$ reading cycle, the time dependent intermediate voltage $V_{Ii}(t)$ is calculated as

$$V_{Ii}(t) = \frac{1}{2}\left(V_{I0i} - V_{p(i-1)}\right)S(t) + \left[\frac{1}{2}\left(V_{I0i} - V_{p(i-1)}\right) + V_{p(i-1)}\right] exp\left[-\left(\frac{1}{\tau_{fi}} + \frac{1}{\tau_{wi}}\right)\left(t - \sum_{s=1}^{i-1} N_s T\right)\right] + \quad (1)$$

$$+V_D\left\{1 - exp\left[-\left(\frac{1}{\tau_{fi}} + \frac{1}{\tau_{wi}}\right)\left(t - \sum_{s=1}^{i-1} N_s T\right)\right]\right\} + \frac{R_{tw}}{R_f + R_{tw}}\left(\frac{1}{2}V_R - V_D\right)\left\{1 - exp\left[-\left(\frac{1}{\tau_{fi}} + \frac{1}{\tau_{wi}}\right)\left(t - \sum_{s=1}^{i-1} N_s T\right)\right]\right\}.$$

**Experimental results and discussions:**

The basic operation of the memory was verified with a discrete circuit of a MOSFET 2SK704 ($V_{th}$ = 1.7 V, $C_0$ = 700 pF) and a 200-nm-epitaxial PZT film as $C_f$ with $V_R$ = 3 V and $V_D$ = 1 V. The $I_D$ was detected by measuring voltage $V_0$ on a 100 Ω resistor connected to the drain of the reading MOSFET. The experimental results were plotted in Fig. 4. From the figure, we can see that the output of the memory depends upon the polarization state of $C_f$. With series of reading pulses we have series of output. This means the reading is non-destructive. To investigate the read endurance of the memory, a self-made MOSFET was used ($V_{th}$ = 1 V, $C_0$ = 210 pF). The leakage current through the W-FET in OFF state was simulated by a twin diode which has a typical leakage current of 1 pA at 1 V. The $C_f$ is a 200-nm-epitaxial PZT film. The output voltages $\Delta V_0$ were measured as a function of reading cycles for SCC and DCC, and plotted in Fig. 5 and 6, respectively. In the SCC, for the $P^-_r$, the $\Delta V_0$ starts decreasing with reading cycles of ≥ $3.0\text{x}10^7$. For $P^+_r$, $\Delta V_0$ is even decreased faster and finally reached to a saturation of nearly zero. In the DCC, for the $P^-_r$, $\Delta V_0$ is almost constant up to $6\text{x}10^7$. For the $P^+_r$, $\Delta V_0$ is slightly decreased or unchanged. To understand the physics during memory operation, a simulation of $\Delta V_0$ is carried out taking into account the contribution of non-returning domain (represented by the coefficient k). The simulated results are in good agreement with the experiments for k = 0.7, as seen in Fig. 5 and 6. For the SCC, the difference in behavior of $\Delta V_0$ between $P^-_r$ and $P^+_r$ can be explained as follows. There are 3 factors contributing to $\Delta V_0$: 1) the generation of induced charge on the intermediate electrode due to reading from the non-returning domain, 2) the $C_f$ and 3) the time constants $\tau_f = R_f(C_f + C_0)$ and $\tau_w = R_w(C_f + C_0)$, where $R_f$ and $R_w$ are resistances of $C_f$ and the twin diode. According to the simulation, for both SCC and DCC, the $\Delta V_0$ finally reaches a saturation value corresponding to a saturation value of $V_I$,

$$V_I(t\to\infty) = C_{f\infty}V_R/[2(C_{f\infty}+C_0)]+[R_w/(R_w+R_f)](0.5V_R-V_D)+V_D,$$

where $C_{f\infty}$ is $C_f$ at saturated $V_f$ and $V_D$ = 0 for SCC. Because the $C_{f\infty}$ for $P^+_r$ is larger than that for $P^-_r$, $\Delta V_0$ saturates at much higher value for the DCC than for the SCC. Therefore, DCC is much better than SCC in term of read endurance.

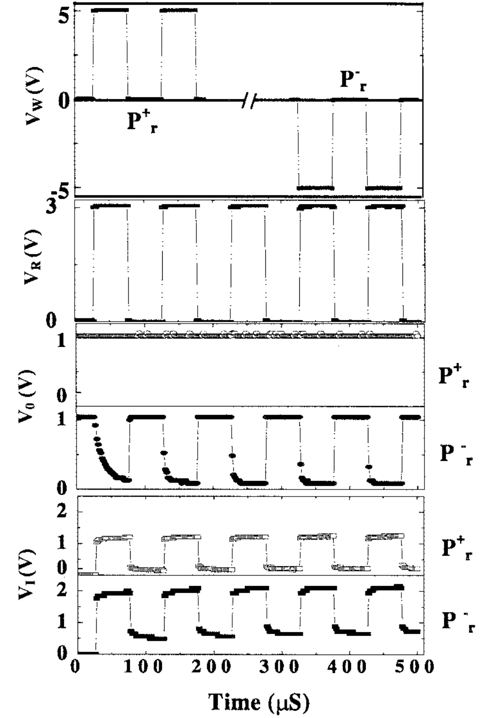


**Fig. 4:** Typical output of the memory for basic operation investigation.

## Conclusions:

A new operational principle for ferroelectric gate field-effect transistor memory has been proposed and it was shown theoretically and experimentally that the new F-FET is possible to overcome the problems of the conventional F-FET. It was also shown that DCC is a good solution to achieve high read endurance.

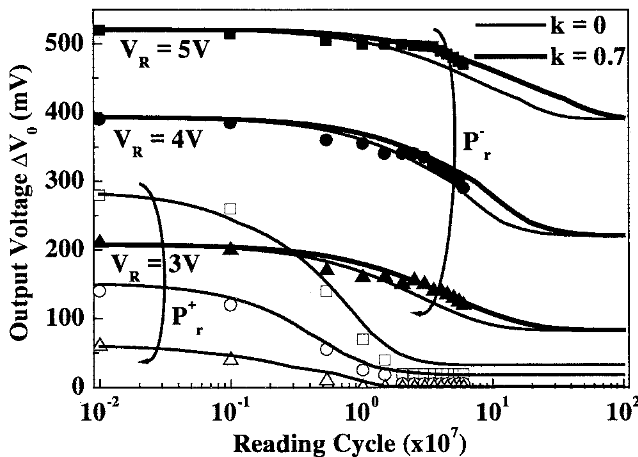


**Fig. 5:** Dependence of $\Delta V_0$ on reading cycle for SCC.

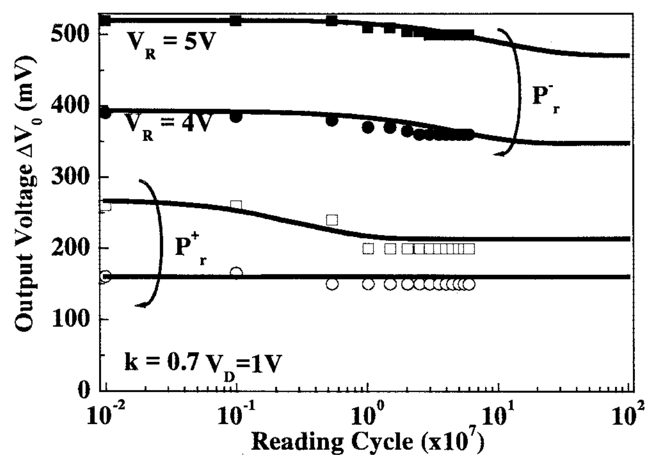


**Fig. 6:** Dependence of $\Delta V_0$ on reading cycle for DCC.