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Fabrication of C_{60} field-effect transistors with polyimide and $Ba_{0.4}Sr_{0.6}Ti_{0.96}O_3$ gate insulators

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A flexible C_{60} field-effect transistor (FET) device has been fabricated with a polyimide gate insulator on the poly(ethylene terephthalate) substrate, and *n*-channel normally off FET properties are observed in this FET device. The field-effect mobility, μ, is estimated to be $\sim 10^{-2}$ cm^2 V^{-1} s^{-1} at 300 K. Furthermore, the C_{60} FET has been fabricated with a high-dielectric $Ba_{0.4}Sr_{0.6}Ti_{0.96}O_3$ (BST) gate insulator, showing *n*-channel properties; the μ value is estimated to be $\sim 10^{-4}$ cm^2 V^{-1} s^{-1} at 300 K. The FET device operates at very low gate voltage, V_G, and low drain-source voltage, V_{DS}. Thus these C_{60} FET devices possess flexibility and low-voltage operation characteristic of polyimide and BST gate insulators, respectively. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2081134]

Field-effect transistors (FETs) with thin films of fullerenes have been extensively studied during the past decades,[1–12] and the potential applications of fullerene FETs in next-generation electronic devices have been discussed based on their high values of field-effect mobility, μ. The first fullerene FET device was fabricated with thin films of C_{60} and a SiO_2 gate insulator by Haddon *et al.*[1] This device showed *n*-channel properties and a high μ value of 0.08–0.30 cm^2 V^{-1} s^{-1}. Subsequently, Haddon developed the C_{70} FET device with the SiO_2 gate insulator which exhibited the *n*-channel performance with the μ value of 2×10^{-3} cm^2 V^{-1} s^{-1}.[2] The μ value of the C_{60} FET device reached 0.56 cm^2 V^{-1} s^{-1} (Ref. 3), which was comparable to the highest μ value realized so far in the *n*-channel FETs with thin films of organic molecules (OFETs) (Ref. 13).

The characteristics such as shock-resistance, structural flexibility, large-area coverage, and portability are the most important advantages expected for the OFETs. Therefore, it is necessary for the SiO_2/Si substrate to be replaced by polymer gate insulators in a realization of the complete flexible OFET devices. In 2004, Someya *et al.* successfully fabricated the flexible and high-performance *p*-channel pentacene FET device with polyimide gate insulator.[14] The flexible and high-performance *n*-channel OFET device is required for a realization of the flexible complementary metal-oxide-semiconductor logic gate circuit, which has many advantages such as low-power consumption, good-noise margin, and ease of design.[15]

The C_{60} FET device with a high-dielectric gate insulator such as $Ba_{0.4}Sr_{0.6}Ti_{0.96}O_3$ (BST) attracts special attention for high-carrier injection into the channel region of C_{60} thin films, because the doping of electrons and holes into C_{60} is expected to yield new materials with novel physical properties, from the analogy with metal-intercalated C_{60} exhibiting superconductivity and metallic behavior. Such novel physical properties are produced by the electron filling to the lowest unoccupied molecular orbital (LUMO) of the C_{60} molecule.[16] Currently, the number of electrons that can be injected into the C_{60} molecules by field-effect doping is at most 0.1 per C_{60} molecule even at the maximum gate voltage V_G^{max}, because of the low-dielectric constant ε_x ($\sim$3.9) of SiO_2 used as an insulating layer. Therefore, new techniques for high-carrier injection, i.e., injection of more than one electron or hole per C_{60} molecule, are required to control the electronic structure of C_{60}.

The maximum density of carriers, N_{max}(cm^{-2}), which can be induced on the dielectric insulating layer, is empirically given by $N_{max} \sim 1.1 \times 10^{13} \varepsilon_x^{1/2}$ since V_G^{max} (MV) $\sim dE_{max} \sim 20d/\varepsilon_x^{1/2}$; d (cm) is the thickness of the insulating layer. The high-carrier injection into C_{60} thin film in the FET device should be realized by using the high ε_x gate insulator. Furthermore, the high-carrier injection into the active layer should achieve the low gate voltage (V_G) and low drain-source voltage (V_{DS}) operation in the FET device. The low-voltage operation is very important in a realizing the practical FET device, because the V_G and V_{DS} required for operation of the OFET device are currently as high as 10–100 V. In the present study, the C_{60} thin-film FET devices with polyimide and BST gate insulators have been fabricated on the poly(ethylene terephthalate) (PET) and the Si substrates, respectively. The fabrication of these FET devices should open a way to the structural flexibility and the low V_G and V_{DS} operation in the OFET device.

Schematic representations of cross-sectional views of the C_{60} FET devices with polyimide and BST gate insulators are shown in Figs. 1(a) and 1(b), respectively. Commercially available PET substrate was cleaned by washing with acetone, 2-propanol, and ultrapure water, and was dried at 190 °C. The Au gate electrodes with thickness of 50 nm were formed on the PET substrate by a thermal deposition under vacuum of 10^{-8} Torr. The films of the polyimide gate insulator were formed by a spin coating of a high-purity

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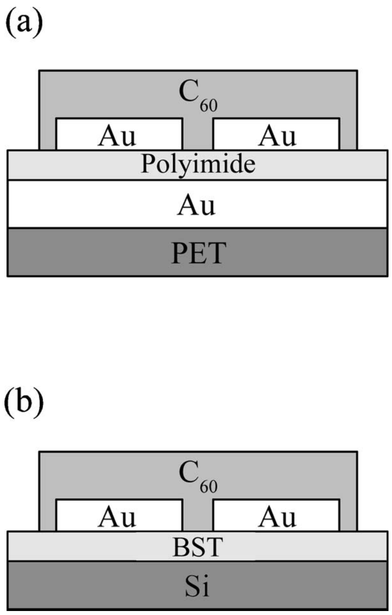

FIG. 1. Schematic representations of cross-sectional view of C_{60} FET devices with a (a) polyimide gate insulator and (b) BST gate insulator.

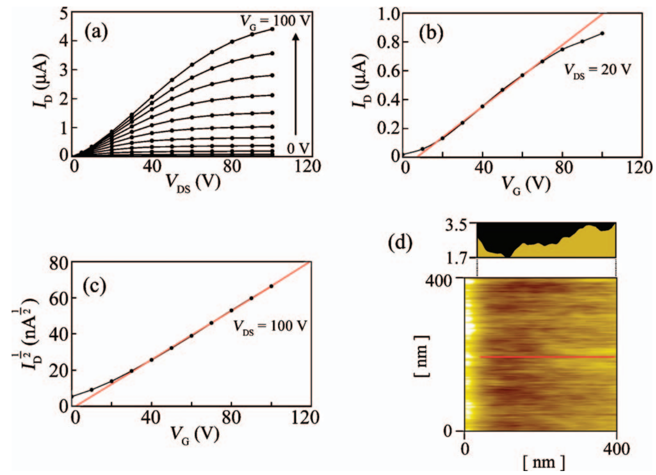

FIG. 2. (Color) (a) I_D-V_{DS} plots, (b) I_D-V_G plot at V_{DS}=20 V, and (c) $(I_D)^{1/2}-V_G$ plot at V_{DS}=100 V for the C_{60} FET with polyimide gate insulator. (d) AFM image of the polyimide surface (bottom); the cross-sectional AFM image (top) observed along the red line. The brightness in the AFM image (bottom) refers to the unevenness of the surface. As the color brightens, the part is closer to the surface.

polyimide precursor (KEMITITE CT4112, Kyocera Chemical) on the Au/PET substrate at 2000 rpm for 5 s and 4000 rpm for 20 s. The films were heated at 100 °C for 10 min and at 180 °C for 1 h. The surface of polyimide films was treated to be hydrophobic with hexamethyldisilazane (HMDS). Fifty (50) nm thickness of Au source-drain electrodes and 150 nm thickness of C_{60} thin films were formed on the substrate by the thermal deposition under 10^{-8} Torr. The channel length L and the channel width W of the C_{60} FET device with a polyimide gate insulator were 30 and 2000 μm, respectively.

The BST layer of the chemical composition $Ba_{0.4}Sr_{0.6}Ti_{0.96}O_3$ was fabricated on the As-doped Si (100) wafer (ρ=0.001–0.004 Ω cm) by the sol-gel method; the isoamyl acetate-amyl alcohol solution of 7 wt % $Ba_{0.4}Sr_{0.6}Ti_{0.96}O_3$ was purchased from Mitsubishi Materials Corporation. The Si wafer was cleaned by washing with acetone, methanol, and H_2SO_4/H_2O_2 (4:1 in volume), and native SiO_2 on the Si wafer was removed by immersing it in dilute HF solution. The wafer was finally washed by ultrapure water. The precursor film of BST was prepared by a spin coating of the $Ba_{0.4}Sr_{0.6}Ti_{0.96}O_3$ solution on the Si substrate at 500 rpm for 3 s and at 2000 rpm for 20 s. The substrate was prebaked at 300–400 °C for 10 min. The spin coating and prebaking were repeated four times before the annealing. The substrate was annealed at 700 °C for 1 h under 100 ml min^{-1} flow of O_2. Fifty (50) nm thickness of source/drain Au electrodes and 150 nm thickness of C_{60} thin films were formed on the BST/Si substrate by thermal deposition under 10^{-8} Torr; the C_{60} FET device with the BST layer treated by HMDS has also been fabricated. The L and W of the C_{60} FET device with a BST gate insulator were 30 and 1000 μm, respectively. The FET properties for all FET devices fabricated in the present study were measured after an annealing at 100–140 °C for 24 h under 10^{-6} Torr.

The drain current I_D versus V_{DS} plots for the C_{60} thin-film FET with a polyimide gate insulator at 300 K are shown in Fig. 2(a). The plots show n-channel normally off FET properties. The plot of I_D versus V_G at V_{DS}=20 V is shown in Fig. 2(b). The I_D increases with increasing V_G to positive up to 100 V. The μ and the threshold voltage, V_T, were determined to be 7.1×10^{-3} $cm^2\ V^{-1}\ s^{-1}$ and 7 V, respectively, from the I_D-V_G plot with the relation, $I_D=(\mu WC_0/L)(V_G-V_T)V_{DS}$, where C_0 is the capacitance per area.[17] The C_0 value was determined to be 1.1×10^{-9} F cm^{-2} from the experimental capacitance, $C(=C_0S)$ measured with an *LCR* meter, where S is the area of electrode. Further, the μ and V_T values of the C_{60} FET with the polyimide gate insulator were estimated to be 1.2×10^{-2} $cm^2\ V^{-1}\ s^{-1}$ and 2 V, respectively, from the $(I_D^{sat})^{1/2}-V_G$ plot [Fig. 2(c)] with the relation $(I_D^{sat})^{1/2}=(\mu WC_0/2L)^{1/2}(V_G-V_T)$ (Ref. 17); the saturation of I_D is clearly observed in Fig. 2(a). The $(I_D^{sat})^{1/2}-V_G$ plot was obtained at V_{DS} of 100 V, and the current on-off ratio, $I_D(V_G=100\ V)/I_D(V_G=0\ V)$, was 160.

The atomic force microscope (AFM) image of the polyimide surface is shown in Fig. 2(d). The maximum depth, D_{max}, from the surface of the polyimide layer was 5.5 nm. The thickness, d, of polyimide was estimated to be 3.0 μm from the C_0 value of 1.1×10^{-9} F cm^{-2} with the relation $C_0=\varepsilon_0\varepsilon_x/d$ by assuming ε_x of 3.8 (Ref. 14), where ε_0 is permittivity in vacuum. The d value of the polyimide layer in this device is larger by 7 times than that, 420 nm, of the SiO_2 layer used by our group in the fullerene FET devices.[9–12] The value of C_0 in the C_{60} FET with 420 nm of SiO_2 layer can be estimated to be $\sim8.2\times10^{-9}$ F cm^{-2} with $C_0=\varepsilon_0\varepsilon_x/d$ as ε_x of the SiO_2 layer is 3.9. Therefore, the C_0 value of the polyimide, 1.1×10^{-9} F cm^{-2}, is smaller than that of SiO_2, 8.2×10^{-9} F cm^{-2}. This implies that the carrier density $N(=C_0V_G/e)$, which can be induced at the same V_G, is smaller in the C_{60} FET with a polyimide gate insulator than that with a SiO_2 layer. This problem can be solved by fabricating the C_{60} FET device with a thinner polyimide layer with high quality.

The plots of I_D versus V_{DS} for the C_{60} FET device fabricated with the crystalline BST layer are shown in Fig. 3(a). The plots show substantially n-channel normally off enhancement-type properties. The I_D increased with increasing the V_G, while at V_G=0 V the I_D was extremely small. When decreasing V_G to the negative value, the small I_D was

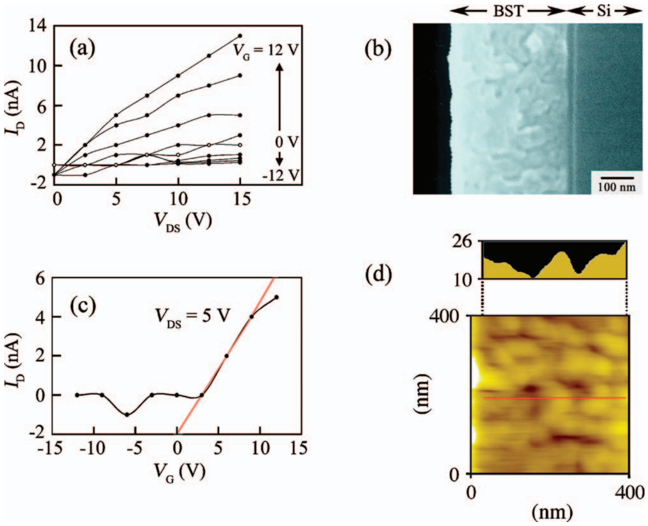

FIG. 3. (Color) (a) I_D-V_{DS} plots, (b) cross-sectional SEM image, (c) I_D-V_G plot at V_{DS}=5 V for the C_{60} FET device with BST gate insulator. (d) AFM image of the BST surface (bottom); the cross-sectional AFM image (top) observed along the red line. In (a), the open circles refer to the I_D-V_{DS} plots at V_G=0 V. The brightness in the AFM image (bottom) refers to the unevenness of the surface. As the color brightens, the part is closer to the surface.

further reduced owing to the depletion of electrons in the channel region. The value of d for the layer was estimated to be 380 nm from the cross-sectional image of the scanning electron microscope (SEM) [Fig. 3(b)]. The μ and V_T values of the FET device were determined to be 4.1×10^{-5} cm^2 V^{-1} s^{-1} and 3 V, respectively, from the I_D-V_G plots [Fig. 3(c)] at V_{DS}=5 V with the relation, $I_D = (\mu W C_0/L)(V_G - V_T)V_{DS}$ (Ref. 17). The C_0 value was estimated to be 8.3×10^{-8} F cm^{-2} from the experimental C. The μ value estimated for the FET device is much lower than those, 0.08–0.56 cm^2 V^{-1} s^{-1}, of the C_{60} FETs with the SiO_2 insulating layer.[1,3,4] Nevertheless, it should be noted that the V_{DS} and V_G values for the FET operation are smaller by one order of magnitude than those for the C_{60} FET with the SiO_2 gate insulator. This result is based on the fact that the high concentration of carriers can be injected even at low V_G owing to the high ε_x gate insulator; the N in the C_{60}/BST FET is 5.2×10^{12} cm^{-2} at V_G=10 V, which is comparable to that in the C_{60}/SiO_2 FET at V_G=100 V, 5.1×10^{12} cm^{-2}. The low μ value can be attributed to a large roughness in the surface of the BST layer. The value of D_{max} for the BST surface can be estimated to be ~35 nm from the AFM image shown in Fig. 3(d); the BST layer was prepared by one-time annealing. Such a large roughness should suppress the carrier transport. The size of crystallite of the BST was estimated to be 20 nm from the x-ray diffraction peak ascribable to 100 reflection, and the size increased with an increase in annealing time at 700 °C. As the D_{max} decreased with an increase in annealing time, the increase in the annealing time may have caused the improvement of carrier transport.

The hydrophobic treatments of the BST thin films were carried out by immersing those into HMDS for 24 h at 300 K. The AFM showed the D_{max} of 10 nm for the HMDS-treated BST surface. The water contact angle increased from 15° to 60° by the HMDS treatment, showing that the BST surface changed to a hydrophobic situation. The I_D-V_{DS} plots showed the n-channel properties with the μ and V_T values of 1.1×10^{-4} cm^2 V^{-1} s^{-1} and −5 V, respectively. This shows clearly that the hydrophobic BST surface can increase the μ value, although the origin remains to be clarified.

In summary, the flexible C_{60} FET device, which exhibits n-channel normally off properties, has been fabricated with a polyimide gate insulator on the PET substrate. Furthermore, the C_{60} FET device, which operates at low V_G and V_{DS}, has been fabricated with the high ε_x gate insulator, BST. The FET device also showed n-channel FET properties. These should open a way towards high-performance fullerene FET devices exhibiting flexibility, portability, and low-voltage operation, and a way towards modification of electronic structure of C_{60} by high-carrier injection, i.e., a realization of novel physical properties.

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[1] R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard, and R. M. Fleming, Appl. Phys. Lett. **67**, 121 (1995).
[2] R. C. Haddon, J. Am. Chem. Soc. **118**, 3041 (1996).
[3] S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara, and Y. Iwasa, Appl. Phys. Lett. **82**, 4581 (2003).
[4] T. Kanbara, K. Shibata, S. Fujiki, Y. Kubozono, S. Kashino, T. Urisu, M. Sakai, A. Fujiwara, R. Kumashiro, and K. Tanigaki, Chem. Phys. Lett. **379**, 223 (2003).
[5] E. Kuwahara, Y. Kubozono, T. Hosokawa, T. Nagano, K. Masunari, and A. Fujiwara, Appl. Phys. Lett. **85**, 4765 (2004).
[6] A. Dodabalapur, H. E. Katz, L. Torsi, and R. C. Haddon, Science **269**, 1560 (1995).
[7] E. J. Meijer, D. M. De Leeuw, S. Setayesh, E. van Veenendaal, B.-H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, and T. M. Klapwijk, Nat. Mater. **2**, 678 (2003).
[8] S. Kobayashi, S. Mori, S. Iida, H. Ando, T. Takenobu, Y. Taguchi, A. Fujiwara, A. Taninaka, H. Shinohara, and Y. Iwasa, J. Am. Chem. Soc. **125**, 8116 (2003).
[9] Y. Kubozono, Y. Rikiishi, K. Shibata, T. Hosokawa, S. Fujiki, and H. Kiatagawa, Phys. Rev. B **69**, 165412 (2004).
[10] K. Shibata, Y. Kubozono, T. Kanbara, T. Hosokawa, A. Fujiwara, Y. Ito, and H. Shinohara, Appl. Phys. Lett. **84**, 2572 (2004).
[11] T. Nagano, H. Sugiyama, E. Kuwahara, R. Watanabe, H. Kusai, Y. Kashino, and Y. Kubozono, Appl. Phys. Lett. **87**, 023501 (2005).
[12] T. Nagano, E. Kuwahara, T. Takayanagi, Y. Kubozono, and A. Fujiwara, Chem. Phys. Lett. **409**, 187 (2005).
[13] P. R. L. Malenfant, C. D. Dimitrakopoulos, J. D. Gelorme, L. L. Kosbar, T. O. Grahama, A. Curioni, and W. Andreoni, Appl. Phys. Lett. **80**, 2517 (2002).
[14] Y. Kato, S. Iba, R. Teramoto, T. Sekitani, T. Someya, H. Kawaguchi, and T. Sakurai, Appl. Phys. Lett. **84**, 3789 (2004).
[15] S.-M. Kang and Y. Leblebici, CMOS *Digital Integrated Circuits, Analysis and Design* (McGraw Hill, New York, 2003).
[16] M. S. Dresselhaus, G. Dresselhaus, and R. C. Eklund, *Science of Fullerenes and Carbon Nanotubes* (Academic, San Diego, 1996).
[17] S. M. Sze, *Semiconductor Devices, Physics and Technology* (Wiley, New York, 2002).