An application to moving picture processing of multi-thread type processors

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1 Introduction

Moving picture processing of real time has to perform an encode fast. However, An encode needs enormous calculation processing. Most processing of encode is Motion compensation processing. The auther design an exclusive processor for movement compensation processing in this study. Therefore, It have to quicken Processing speed of an encode At first, motion compensation processing has much calculation amount. So, a calculation amount has to reduce by application of method. He design the instruction set architecture that was suitable for motion compensation. Processing is possible effectively by making an instruction line with this instruction set architecture. processing speed Moving picture data do not have dependence relationship. Therefore, Each trip of processing can divides to multi-threads. And, to perform multi-thread processing becomes improvement of processing speed.

2 Motion compensation processing

Motion compensation processing need enormous processing time for performing motion vector serach. Motion vector serach compare luminance

value of macro-block range of object frame to find a motion vector with reference frame, it find a summation. Every macroblock of an object frame perform this processing. And, While moving one pixel of macroblock range with a reference frame. All frames area find a summation every each macroblock. Because there is very much calculation amount, to reduce computational complexity apply method. At first, it is hierarchical matching method. This method perform a rough search for a reduction image by this method. It searches that is detailed from the provided most suitable position. Next, it is Search area limitation method. This method supposes that an object does not suddenly move generally, and to limit a search area of a frame.

3 Suggestion method

By a motion vector search, There may be more few Load instruction number of times of an object frame than the Load instruction number of times of a reference frame. By using this characteristic, It reduce the publication number of times of the Load instruction that is memory access instruction. Therefore, processing speed is improved . By publishing a Load instruction with one loop a lot in parallel, Processing process can move to the next instruction without a stall using the data right after a Load of the beginning was over most. Latency of a Load instruction can cover memory access. We understand that many registers are necessary so that a pipeline stall does not occur by register competition.

4 A design of instruction set architecture

A design of instruction set architecture The auther design instruction set architecture to perform a movement vector search. For Load number of times reduction method of suggestion method, A design is necessary so that many registers can appoint it. Instruction set architecuture length and register length assume 32bit length together. Operand length of a register assumes 6bit. Therefore, 64 registers can express it. An Instruction Format is the R format, I format, J format. R format is a format of an operation instruction, And it is three operand methods. I format is memory access

instruction and a condition branch instruction. J format is uncondition branch instruction.

5 A design of a motion vector search processing instruction line handling

By the instruction set architecture, The auther designed the motion vector search processing instruction line. Size of a moving picture used QVGA. As a result, the total step was 64,549,986. Next, The auther make out the code scheduling for an insturuction line, and a number of cycle was estimated. Therefore, The CPI in one thread was 1.087. Therefore, Clock frequency is 2.2GHz need for processing of 30fps of QVGA. Next, he think about moving picture processing of XVGA size. Frame Size of XVGA is bigger than around 10 times QVGA. He perform to improvement of the number of the steps, subdivision of a pipeline stage, multi-thread processing.

6 An application of multi-thread type processor processing

Multi-thread processing evades pipeline hazard by carrying out multi independent threads by pipeline processing in parallel, and it is a method to be able to improve throughput. Subdivision of a pipeline stage improves clock frequency. Therefore, a penalty by pipeline hazard becomes big, but improvement of throughput is possible by multi-thread processing. As a result of stage division, A pipeline stage is 19 steps by an operation instruction, and 47 steps by a load/store instruction. The number of the logic steps of a pipeline is 3 steps. And clock frequency achieves 3.7GHz by 45nm technology. Moving picture data do not have dependence relationship. Therefore, multi-thread processing is suitable. Division method of thread is every macro-bloc of object frame. Multi-thread processing of 16 thread at the maximum is possible by frame size. As a result of XVGA processing, CPI achieved 1.69 in a 1 thread and 1 in a 16 thread. And processing of 30fps is possible 16 thread.

7 Conclusion

In this paper, The author thought quickening processing speed by designing an exclusive processor for motion compensation processing to improve encode speed of a moving picture. At first, he explained motion compensation processing. Instruction set architecture made by suggestion method. instruction line of motion vector search processing designed by instruction set architecture. The code scheduling is performed for a instruction line. He estimated a step, cycle, CPI, and divide a thread to perform a multi-thread. Improvement of CPI was provided by a multi-thread. Finally, motion vector serach processing of XVGA is possible.