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An investigation of correlation between transport characteristics and trap states in *n*-channel organic field-effect transistors

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Transport characteristics in *n*-channel organic field-effect transistors are discussed on the basis of density of states (DOS) for trap states determined with multiple trap and release model. First the trap-free intrinsic mobilities, the activation energies, and total effective DOS for conduction band are determined with the effective field-effect mobility versus temperature plots and total DOS of trap states. Second the general formula for subthreshold swing S applicable to organic field-effect transistors is derived and the surface potentials are determined from the S determined from the transfer curves and the DOS for the trap states according to the general formula. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2908886]

Field-effect mobility μ for thin film organic field-effect transistors (OFETs) is at most $\sim 1\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$, which is lower by three to four orders of magnitude than those in metal-oxide-semiconductor (MOS) field-effect transistors.[1–4] This low μ value in thin film OFETs originates from both facts that π-conduction network is not sufficiently expanded in the whole channel region and that trap states are formed in the gap between highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO). The trap states are produced by existence of impurities, artificial doping, defects, and other disturbance of lattice periodicity. The total shallow and deep trap states were recently estimated by photoinduced carrier transfer measurements.[5,6]

Density of states (DOS) for the trap states $N_t(\varepsilon)$ at the interface between gate dielectric and active layers in OFETs can be determined with multiple trap and release (MTR) model.[7–9] Here ε is the energy measured from LUMO for electron (or HOMO for hole). The $N_t(\varepsilon)$ in unit of $\mathrm{cm^{-2}\,eV^{-1}}$ is given by the following equation:[7]

$$N_t(\varepsilon) = \frac{C_0}{e}\left(\frac{d\varepsilon_a}{dV_G}\right)^{-1}, \tag{1}$$

where C_0, e, ε_a, and V_G are gate capacitance per area, elemental charge, activation energy, and applied gate voltage, respectively. The ε_a was determined from the temperature T dependence of drain current I_D; ε_a is approximately equal to ε. Lang *et al.* determined the $N_t(\varepsilon)$ for pentacene crystal FET and showed an exponential decay for the increased ε above the top of HOMO band and a single peak due to bias-stressed defect.[7]

Recently, we have studied trap states for C_{60} dendrimer Langmuir–Blodgett (LB) film and C_{60} thin film FETs (Ref. 8) on the basis of MTR model. The $N_t(\varepsilon)$ values for the FETs showed a simple exponential decay with an increase in ε.[8] The plots were fitted with the following equation:

$$N_t(\varepsilon) = N_t(0)\exp(-\beta\varepsilon). \tag{2}$$

The DOS, $N_t(0)$, for the trap states at $\varepsilon=0$ and the slope β of exponential DOS tail for LB FET were $8.1\times10^{19}\ \mathrm{cm^{-3}\,eV^{-1}}$ ($6.1\times10^{13}\ \mathrm{cm^{-2}\,eV^{-1}}$) and $6.4\ \mathrm{eV^{-1}}$, respectively, while the $N_t(0)$ and β for C_{60} thin film FET were $2.0\times10^{19}\ \mathrm{cm^{-3}\,eV^{-1}}$ ($1.5\times10^{13}\ \mathrm{cm^{-2}\,eV^{-1}}$) and $5\ \mathrm{eV^{-1}}$.[8] The $N_t(\varepsilon)$ for LB film FET are higher by a factor of 4 than that for C_{60} FET at $\varepsilon=0.1-0.4$ eV. In this estimation,[8] the depth of trap states is assumed as 7.5 nm on the basis of the previous report.[7,10]

In this letter, we have discussed a correlation between DOS of trap states determined by our group for the LB and C_{60} FETs (Ref. 8) and their transfer characteristics. First, intrinsic mobility μ_0, difference between trap state and LUMO level $\varepsilon_a{}'$ and total effective DOS for conduction band N_c have been determined from effective field-effect mobility $\mu_{\mathrm{eff}}(T)$, as a function of T and $N_t(\varepsilon)$ in the C_{60} dendrimer LB and C_{60} thin film FETs. Here, the $\varepsilon_a{}'$ corresponds to the activation energy determined from $\mu_{\mathrm{eff}}(T)$-T plot, and it should be approximately equal to ε_a. Furthermore, the surface potentials ϕ_s's, have been determined for these FETs by use of the new S formula applicable to OFETs developed in this study.

First, the correlation has been investigated between $\mu_{\mathrm{eff}}(T)$ and $N_t(\varepsilon)$. Here, $\mu_{\mathrm{eff}}(T)$ in n-channel FET device is given by[11–14]

$$\mu_{\mathrm{eff}}(T) = \mu_0 \Bigg/ \left\{1 + \frac{N_t}{N_c}\exp\left(\frac{\varepsilon_a{}'}{k_BT}\right)\right\}. \tag{3}$$

The N_t and k_B are the total DOS for the trap states and the Boltzmann constant, respectively. The μ_0 corresponds to the $\mu_{\mathrm{eff}}(T)$ in trap-free FET device. The above formula implies that the increase in N_c by the high crystallinity of thin films or high π-conduction network, and the decrease in N_t by the reduction of defects and impurities play an important role to the realization of high $\mu_{\mathrm{eff}}(T)$ value.

The $\mu_{\mathrm{eff}}(T)$ was obtained from $I_D{}^{1/2}$-V_G plot at $V_{DS}=100$ V with the general formula for saturation drain

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current.[15,16] We can estimate the N_t by using the following expression:

$$\int_0^\infty N_t(\varepsilon)d\varepsilon = \int_0^\infty N_t(0)\exp(-\beta\varepsilon)d\varepsilon = \frac{N_t(0)}{\beta} = N_t. \tag{4}$$

For the LB FET, the N_t has been estimated to be $1.3 \times 10^{19}\ \text{cm}^{-3}$ ($9.5 \times 10^{12}\ \text{cm}^{-2}$) from the $N_t(0)$ of $8.1 \times 10^{19}\ \text{cm}^{-3}\ \text{eV}^{-1}$ ($6.1 \times 10^{13}\ \text{cm}^{-2}\ \text{eV}^{-1}$) and the β of $6.4\ \text{eV}^{-1}$ reported in Ref. 8 according to Eq. (4). The plot of $\mu_{\text{eff}}(T)$-$1000/T$ for the LB FET is shown in Fig. 1(a). The plot can be well fitted by Eq. (3), and the μ_0, $\varepsilon_a{}'$ and N_c for LB FET have been determined to be $0.02\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$, 100 meV, and $1.1 \times 10^{20}\ \text{cm}^{-3}$ ($8.3 \times 10^{13}\ \text{cm}^{-2}$), respectively. The μ_0 of $0.02\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ is the maximum value of this LB FET expected in the case of trap free. This small μ_0 value implies the formation of incomplete π-conduction network responsible for the n-channel transport because the value is directly associated with the mobility of free carriers in the conduction band. The $\varepsilon_a{}'$ is almost the same as that, 110 meV, for the pentacene thin film FET,[11] which was estimated with the same equation as Eq. (3); the grain size of pentacene thin films was 100–200 nm.

Furthermore, the μ_0, $\varepsilon_a{}'$, and N_c values for C_{60} thin film FET have been determined to be $0.37\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$, 120 meV, and $2.6 \times 10^{20}\ \text{cm}^{-3}$ ($2.0 \times 10^{14}\ \text{cm}^{-2}$), respectively, from the fitted line [Fig. 1(a)]. The μ_0 for C_{60} FET is higher by a factor of 20 than that of the LB FET, but the $\varepsilon_a{}'$ is almost the same as that for the LB FET. The small μ_0 reflects the small mobility of free carriers, which is produced by a large phonon scattering and scattering by the defects (disorder of lattice periodicity).[16] Therefore, it can be concluded that the lattice disorder of LB films is larger than that of C_{60} thin films formed by thermal deposition. On the other hand, the same $\varepsilon_a{}'$ suggests the same width in the distribution of trap states. Therefore, the similar slope found in the $N_t(\varepsilon)$-ε plots for LB and C_{60} thin film FETs (shown in Ref. 8) is consistent with almost the same $\varepsilon_a{}'$ found in these devices. The $\varepsilon_a{}'$ of ~100 meV shows a broad distribution of trap states in both FETs.

The N_c values for LB and C_{60} are 8.3×10^{13} and $2.0 \times 10^{14}\ \text{cm}^{-2}$, respectively. The N_c for C_{60} is slightly higher than that for LB FET, showing that the crystallinity of C_{60} thin films is higher than that of LB films. We tried to estimate the DOS for conduction band for the ideal close-packed layer of C_{60}. Here, it should be noticed that the depth of the channel for C_{60} thin films is the monolayer scale, 1 nm,[17] rather than the trap depth, 7.5 nm.[7,10] The number of C_{60} molecules for 1 nm is $1.4 \times 10^{14}\ \text{cm}^{-2}$, and the number of levels can be calculated to be $8.4 \times 10^{14}\ \text{cm}^{-2}$ by a consideration of both threefold degenerated LUMO levels and two spin states.[18] The N_c for real C_{60} FET device ($2.0 \times 10^{14}\ \text{cm}^{-2}$) is less than a quarter of the expected value for ideal close-packed layer ($8.4 \times 10^{14}\ \text{cm}^{-2}$), showing that the real C_{60} thin films are disordered. Thus, the total effective DOS for conduction band could be obtained from the $N_t(\varepsilon)$ value and the $\mu_{\text{eff}}(T)$-T plot.

The S is defined by the following equation:[16]

$$S = \frac{dV_G}{d\log(I_D)} = \ln 10 \Bigg/ \left(\left[\frac{e}{k_BT} - \left\{\frac{d}{d\phi_s}\left(-\frac{d\phi_s}{dx}\right) \Bigg/ \left(-\frac{d\phi_s}{dx}\right)\right\}\right]\frac{d\phi_s}{dV_G}\right), \tag{5}$$

where x is the depth of C_{60} thin films; the position at $x=0$ refers to the interface between SiO_2 gate dielectric and C_{60} thin films. Equation (5) is available for I_D-V_G plot in any V_{DS} region. In general analysis for MOS FET which operates in an inversion regime, the second term in the parentheses of denominator of the right side of Eq. (5) can be neglected because this term is replaced by $1/(2\phi_S)=1/[2\phi(0)]$, where $\phi(0)$ is the potential $\phi(x)$ at $x=0$ in the depletion regime, and $1/(2\phi_s)$ is very small compared to e/k_BT in the weak inversion regime. When the second term is neglected and

$$\frac{d\phi_s}{dV_G} = \left[1 + \frac{eN_t(\varepsilon) + C_D}{C_0}\right]^{-1}$$

is introduced into Eq. (5), the S is given by well known formula[16]

$$S = \left(\frac{k_BT}{e}\right)(\ln 10)\left[1 + \frac{eN_t(\varepsilon) + C_D}{C_0}\right], \tag{6}$$

where C_D is the depletion region capacitance. Here, it should be noted that the C_D is strictly vanishing in the accumulation regime because the depletion layer is not formed. However, as previously reported,[8] the theoretical S values, 2.2 V/decade for LB FET and 1.8 V/decade for C_{60} FET, calculated with Eq. (6) at $C_D=0$ were smaller by a factor of 5 than the experimental S determined from I_D-V_G plots in $V_{DS}=100$ V at 300 K (10.2 V/decade for the LB FET and 7.9 V/decade for the C_{60} FET) [Figs. 1(b) and 1(c)].

Highly purified C_{60} should be an intrinsic semiconductor with band gap E_G of 2.6 eV,[19] but the thin films of C_{60} formed by thermal deposition of normal grade of C_{60} (purity > 99.5%) show n-type semiconductorlike electronic structures.[20] Therefore, the channel region is concluded to be formed by major carriers (or electrons) in the real n-channel C_{60} thin film FET, showing that Eq. (6) must be fundamentally changed to the formula which is applicable to the OFETs, i.e., accumulation region. In the accumulation regime, the second term cannot be neglected because it is not represented by $1/(2\phi_s)$ and actually $1/(2\phi_s)$ is not small in comparison with e/k_BT.[16] In the accumulation regime of n-type semiconductor, the $\phi(x)$ thin films can be represented as

$$\phi(x) = \frac{k_BT}{e}\left[\ln\frac{1}{\cos^2\left(C + \frac{x}{\sqrt{2}L_D}\right)}\right]$$

and L_D is the Debye length, and C is $\cos^{-1}[\exp(-e\phi_s/2k_BT)]$. By considering the relation $d\phi_s/dx = [d\phi(x)/dx]_{x=0}$ and by substituting the above relation for $\phi(x)$ into Eq. (5), the S is newly given by[21]

$$S = \left(\frac{k_BT}{e}(\ln 10)\left[1 + \frac{eN_t(\varepsilon)}{C_0}\right]\right) \Bigg/ \left(1 - \frac{1}{2}\left[\left\{1 - \exp\left(\frac{-e\phi_s}{k_BT}\right)\right\}^{-1}\right]\right). \tag{7}$$

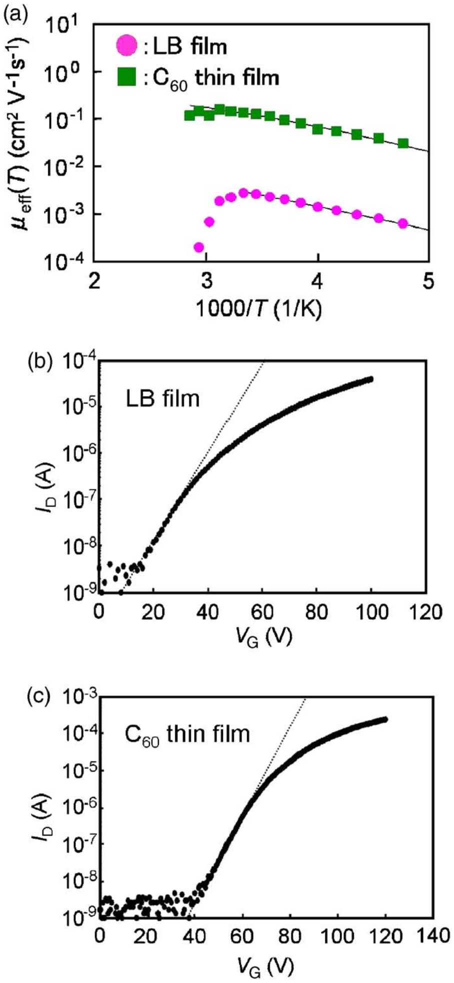

FIG. 1. (Color online) (a) $\mu_{\mathrm{eff}}(T)-1000/T$ plots for the C_{60} dendrimer LB FET and C_{60} thin film FETs are shown together with the fitting line with Eq. (3). The large deviation of $\mu_{\mathrm{eff}}(T)$ from the fitted line, which is found in the low $1000/T$ region ($T>300$ K) of the LB FET, is due to the transition caused by a thermal fluctuation of C_{60} dendrimer (Ref. 8). Therefore, the $\mu_{\mathrm{eff}}(T)$ above 300 K in the LB FET was not used for the curve fitting. I_D-V_G plots for (b) C_{60} dendrimer LB and (c) C_{60} thin film FETs. In (b) and (c), the fitted lines are drawn in order to estimate $S=[d\log(I_D)/dV_G]^{-1}$.

In the accumulation regime, $|\phi_s|$ is known to be only a few $k_BT/e=25.9$ mV at 300 K. Equation (7) refers to the S formula for the electron accumulation of n-type semiconductor. As $\phi_s \ll 0$ for the weak inversion region, i.e., hole layer in n-type semiconductor, Eq. (7) becomes Eq. (6) where $C_D \neq 0$. Thus, Eq. (7) can give the S value in all regime of channel conduction in FET devices with n-type semiconductor. It should be noticed that in the weak inversion regime, the S can be given by Eq. (6) for both p- and n-type semiconductors but Eq. (7) can be associated with only n-type semiconductor.

We can estimate the ϕ_s for LB and C_{60} FETs by substituting the experimental S estimated from I_D-V_G plot [Figs. 1(b) and 1(c)] and the $N_t(\varepsilon)$ at the corresponding V_G ($<V_{\mathrm{th}}$) into the new S formula, Eq. (7). The ϕ_s value for C_{60} dendrimer LB FET has been estimated to be 26 mV from $N_t(\varepsilon)=2.5\times10^{18}$ cm^{-3} eV^{-1} (1.9×10^{12} cm^{-2} eV^{-1}) and the experimental S of 10.2 V/decade, while that for C_{60} thin film FET was 27 mV from $N_t(\varepsilon)=2.1\times10^{18}$ cm^{-3} eV^{-1} (1.6×10^{12} cm^{-2} eV^{-1}) and the experimental S of 7.9 V/decade. These positive and small ϕ_s values indicate weak electron accumulation at V_G lower than V_{th} in both LB and C_{60} FETs.

Thus a clear correlation between $\mu_{\mathrm{eff}}(T)$ and N_t has been found and the N_c could be well estimated for OFETs. Furthermore, the reliable ϕ_s could be obtained from the experimental S and the DOS of trap states on the basis of the universal S formula applicable to OFETs developed in this study. The ϕ_s values confirmed a formation of electron accumulation layers in C_{60} dendrimer LB and C_{60} thin film FETs.

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[21] The following equations:

$$\left[\frac{e}{k_BT}-\left\{\frac{d}{d\phi_s}\left(-\frac{d\phi_s}{dx}\right)\right\}\Big/\left(-\frac{d\phi_s}{dx}\right)\right]\frac{d\phi_s}{dV_G} = \frac{e}{k_BT}\left[1-\frac{1}{2\sin^2 C}\right]\left[1+\frac{eN_t(\varepsilon)}{C_0}\right]^{-1}$$

and

$$\frac{1}{\sin^2 C}=\left[1-\exp\left(\frac{-e\phi_s}{k_BT}\right)\right]^{-1},$$

are used in this derivation, and $C_D=0$ in the accumulation regime.