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# Ultrathin silicon nitride gate dielectrics prepared by catalytic chemical vapor deposition at low temperatures

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The feasibility of using ultrathin silicon nitride ( $\text{SiN}_x$ ) films, prepared by catalytic chemical vapor deposition (Cat-CVD) method, as an ultrathin gate dielectric is reported. The effects of postdeposition treatments carried out using hydrogen ( $\text{H}_2$ )-decomposed species or  $\text{NH}_3$ -decomposed species formed by catalytic cracking of  $\text{H}_2$  and  $\text{NH}_3$  are also studied. A small hysteresis loop is seen in the  $C-V$  curve of as-deposited Cat-CVD  $\text{SiN}_x$  films. The leakage current in the case of these films with equivalent oxide thickness (EOT) of 3 nm is slightly larger than that in the conventional thermal  $\text{SiO}_2$  films of similar EOT. However, it is found that the properties of Cat-CVD  $\text{SiN}_x$  films are markedly improved by the postdeposition  $\text{H}_2$  or  $\text{NH}_3$  treatments, that is, the hysteresis loop disappears and the leakage current decreases by three orders of magnitude. © 2000 American Institute of Physics. [S0003-6951(00)01943-4]

As semiconductor devices are scaled down to submicron dimensions, the conventional processing temperatures of approximately  $900^\circ\text{C}$  will be incompatible with the desired device structure. For example, the conventional high-temperature formation process of gate dielectrics changes the impurity profile formed in the substrate. Thus, the gate dielectric must also be formed at temperatures below  $550^\circ\text{C}$ .<sup>1</sup> Because the dielectric constant of  $\text{SiN}_x$  is about twofold that of  $\text{SiO}_2$ , the  $\text{SiN}_x$  film is one of the candidate films for replacing the  $\text{SiO}_2$  gate dielectric.<sup>2</sup> Therefore, the lower growth temperature of  $\text{SiN}_x$  films is a key for the fabrication of future ultralarge-scale integrated circuits (ULSI).

The catalytic chemical vapor deposition (Cat-CVD) method is a new technique, in which deposition gases are decomposed by catalytic cracking reactions with a heated catalyzer placed near substrates so that  $\text{SiN}_x$  films are deposited at substrate temperatures of approximately  $300^\circ\text{C}$  without the aid of plasma or photochemical excitation.<sup>3,4</sup> Thus, the surfaces of the substrates and the films do not sustain plasma damage. In effect, we have already succeeded in depositing high-quality  $\text{SiN}_x$  films as thick as 300 nm as passivation films by this method using a gas mixture of  $\text{SiH}_4$  and  $\text{NH}_3$ .<sup>5</sup> When the flow rate of  $\text{NH}_3$  exceeds 50–100 times that of  $\text{SiH}_4$ , nearly stoichiometric ( $\text{Si}_3\text{N}_4$ ) films are formed in which the hydrogen content is as low as a few at. %. Under these conditions, the  $\text{Si}_3\text{N}_4$  films have adequate insulating properties, that is the resistivity and breakdown electric field are larger than  $10^{14} \Omega \text{ cm}$  and several  $\text{MV/cm}$ , respectively. Additionally, it is known that Cat-CVD is useful not only for film deposition but also for surface modification of semiconductors, such as direct nitridation of  $\text{Si}$ <sup>6</sup> and  $\text{GaAs}$ .<sup>7</sup>

In the present letter, the feasibility of using Cat-CVD  $\text{SiN}_x$  films as ultrathin gate dielectrics for ULSI devices is

studied. Particularly, the effects of postdeposition treatments by using the  $\text{H}_2$ -decomposed species or  $\text{NH}_3$ -decomposed species formed by catalytic cracking of  $\text{H}_2$  and  $\text{NH}_3$  are studied.

The Cat-CVD apparatus is schematically illustrated in Fig. 1. A tungsten wire (diameter  $0.5 \text{ mm } \phi$  and total length 1300 mm) is used as the catalyzer and placed beneath the substrate at a distance of 40 mm. A catalyzer is coiled, pinned by molybdenum wires and spread parallel to the substrate with an area of  $65 \text{ mm} \times 70 \text{ mm}$ . The deposition chamber (diameter 200 mm, height 200 mm) is made from stainless steel. The sample substrates are attached to a substrate holder which is heated by a heater. A thermocouple is mounted just beside the substrate on the substrate holder to measure the holder temperature ( $T_h$ ). This includes the effect of thermal radiation from the catalyzer, which is heated electrically. The temperature of the catalyzer ( $T_{\text{cat}}$ ) is estimated by both an electronic infrared thermometer placed outside a quartz window (emissivity is 0.4) and from the temperature dependence of the electric resistivity of the cata-

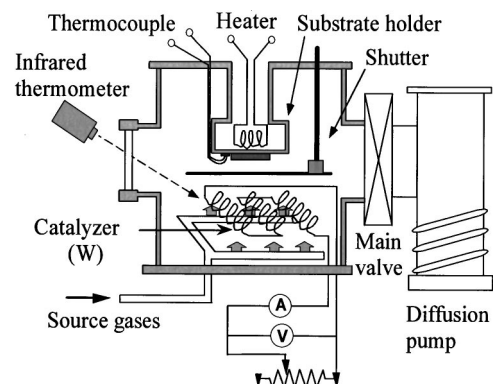


FIG. 1. Schematic diagram of a Cat-CVD apparatus.

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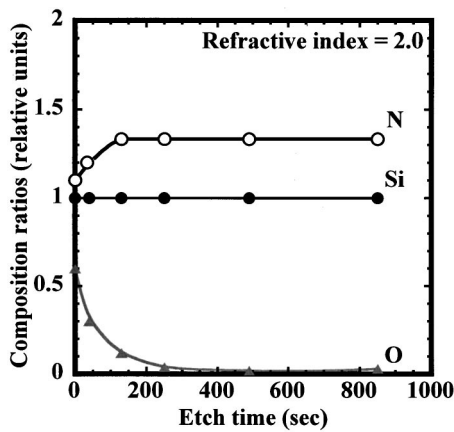


FIG. 2. Distribution of Si, O and N in the depth direction measured by XPS with as-deposited Cat-CVD  $\text{SiN}_x$ .

lyzer. The  $\text{SiH}_4$  and  $\text{NH}_3$  gas mixture is introduced into the chamber from many stainless steel nozzles placed below the catalyzer. These gases were decomposed at the heated catalyzer. The gas pressure ( $P_g$ ) is measured by an electronic capacitance manometer and it is kept at several mTorr. The chamber is pumped down to about  $5.0 \times 10^{-7}$  Torr by a rotary and an oil diffusion pump before deposition. The chamber pressure during deposition is controlled by the main valve between the diffusion pump and the chamber.

An *n*-type Czochralski (Cz)-Si(100) wafer with a resistivity of 0.85–1.50  $\Omega\text{cm}$  is degreased and cleaned by the RCA method.<sup>8</sup> Then, it is dipped in 0.5% diluted HF for 0.5 min. After the cleaning, the wafer pieces are immediately loaded into the Cat-CVD chamber. Then, the chamber is evacuated to  $5 \times 10^{-7}$  Torr. The deposition conditions of the  $\text{SiN}_x$ , the flow rate of  $\text{SiH}_4$  gas,  $\text{FR}(\text{SiH}_4)$ , and that of  $\text{NH}_3$ ,  $\text{FR}(\text{NH}_3)$ , are 1.1 and 60 sccm, respectively.  $\text{FR}(\text{H}_2)$  is kept at 50 sccm when  $\text{H}_2$  is used for post  $\text{SiN}_x$  deposition treatments, and  $\text{FR}(\text{NH}_3)$  is 60 sccm when  $\text{NH}_3$  issued. In both the deposition and post  $\text{SiN}_x$  deposition treatments,  $T_{\text{cat}}$  and  $T_h$  are 1800–1900 °C and 300 °C, and the gas pressures of deposition and postdeposition treatments are 0.01 Torr, respectively.

The electrical properties of the deposition films are evaluated by fabricating a metal-insulator-semiconductor (MIS) ( $\text{Al}/\text{SiN}_x/\text{Si}$ ) capacitor structure with the electrode area of  $3 \times 10^{-2} \text{mm}^2$ . In these samples, no postmetal annealing treatments are performed. The capacitance–voltage ( $C$ – $V$ ) characteristic is measured at the frequency of 1 MHz and with the sweep rate of 0.1 V/s using a SANWA model MI-319A. The leakage current density–voltage ( $J$ – $V$ ) characteristics are measured using a Hewlett-Packard semiconductor parameter analyzer model 4156A. The measurement of the refractive index of  $\text{SiN}_x$  is carried out by the ellipsometry method using a helium-neon laser of 632.8 nm wavelength. The conditions of  $\text{SiN}_x$  films are characterized by *ex situ* x-ray photoelectron spectroscopy (XPS) using monochromatic Al  $K\alpha$  radiation. The binding energies are calibrated to the adventitious carbon peak at 284.6 eV. Measurements of the depth profile of each atom are carried out using XPS by etching using the argon sputtering.

Figure 2 shows the as-deposited Cat-CVD  $\text{SiN}_x$  films, the depth profiles of Si, O and N are measured by XPS. The

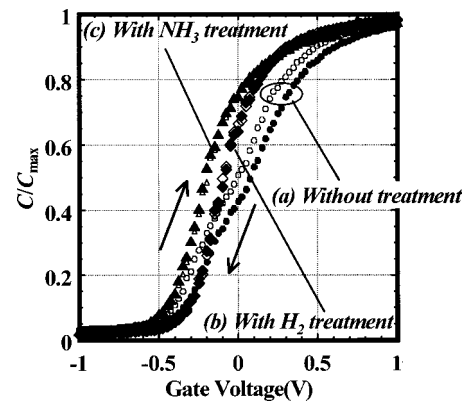


FIG. 3.  $C$ – $V$  characteristics with Cat-CVD  $\text{SiN}_x$ . (a) Without postdeposition treatments, (b) with postdeposition  $\text{H}_2$  treatments and (c) with postdeposition  $\text{NH}_3$  treatments.

horizontal axis shows the sputter etch time by argon, corresponding to the depth, and the vertical axis shows the composition ratio of N and O in normalizing Si as 1. It is found the composition ratio of Si to N is 1.33 at a certain depth and O is not detected. This means that the stoichiometric  $\text{SiN}_x$  ( $\text{Si}_3\text{N}_4$ ) films are formed. A high density of oxygen that exists at the film surface appears to be caused by adsorption of the atmosphere because the evaluation is carried out by *ex situ* XPS. The refractive index of this film is 2.0.

The  $C$ – $V$  characteristics of the Cat-CVD  $\text{SiN}_x$  films measuring diodes are shown in Fig. 3. A small hysteresis loop is seen in the  $C$ – $V$  curve as-deposition sample. However, the hysteresis loop disappears from the  $C$ – $V$  curve following the postdeposition  $\text{H}_2$  or  $\text{NH}_3$  treatments for 60 min. The interface trap density ( $D_{\text{it}}$ ) calculated by the Terman method<sup>9</sup> of the as-deposited sample is  $4.2 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ . However, the value of  $D_{\text{it}}$  is reduced to  $1.2 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$  following the postdeposition  $\text{H}_2$  or  $\text{NH}_3$  treatments, but is still much larger than that of conventional thermal  $\text{SiO}_2$  films. On the other hand, the flatband voltage is shifted to a negative value following the postdeposition  $\text{NH}_3$  treatments. We consider that the  $\text{SiN}_x$  film is nitrified by the postdeposition  $\text{NH}_3$  treatments.

The EOT measured using MIS diodes with the Cat-CVD  $\text{SiN}_x$  films is shown in Fig. 4. The thickness of the  $\text{SiN}_x$  films measured using an ellipsometer is about 4.3 nm while the

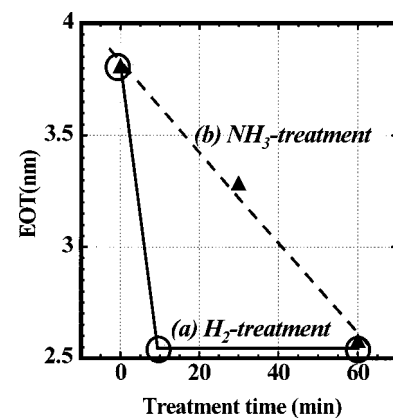


FIG. 4. EOT measured on MIS diodes at different treatment times with Cat-CVD  $\text{SiN}_x$ . (a) With postdeposition  $\text{H}_2$  treatments and (b) with postdeposition  $\text{NH}_3$  treatments.

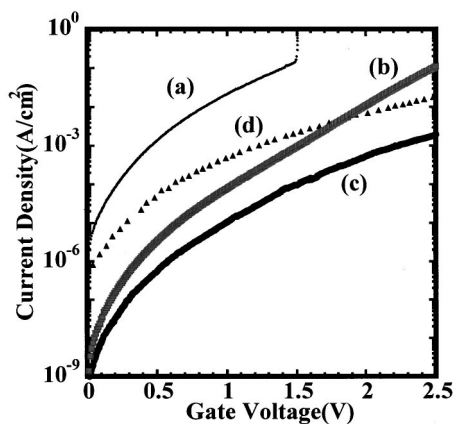


FIG. 5. The  $J$ - $V$  characteristics with Cat-CVD  $\text{SiN}_x$ . (a) Without postdeposition treatments (EOT=2.97 nm), (b) with postdeposition  $\text{H}_2$  treatments (EOT=2.91 nm), (c) with postdeposition  $\text{NH}_3$  treatments (EOT=2.78 nm) and (d) thermal  $\text{SiO}_2$  (EOT=2.8 nm) (see Ref. 10).

EOT measured using MIS diodes in the accumulation mode is about 2.5–3.8 nm. The EOT decreases since the dielectric constant of the films is likely to increase following these treatments, but the refractive index remains unchanged.

Figure 5 shows the leakage currents measured for Cat-CVD  $\text{SiN}_x$  films and for conventional thermal  $\text{SiO}_2$  films<sup>10</sup> of about 2.9 nm of EOT. It is found that the leakage currents are significantly decreased following the postdeposition treatments for 60 min. This is also increases the dielectric constant and reduces the trap-assisted tunneling currents. The postdeposition treatments for Cat-CVD  $\text{SiN}_x$  films reduce the leakage currents by several orders of magnitude compared with that of conventional thermal  $\text{SiO}_2$  films of similar EOT.

Figure 6 shows the N 1s XPS spectra measured for Cat-CVD  $\text{SiN}_x$  films. The postdeposition treatments for 60 min results in the formation of  $\text{N}=\text{Si}_3$  bonds as shown in the spectrum, because the N 1s peak energy (397.5 eV) is the same as that of the conventional thermal CVD  $\text{Si}_3\text{N}_4$ .<sup>11</sup> Without postdeposition treatments, nitrogen atoms may form  $\text{N}=\text{Si}_2$  bonds, since the N 1s peak energy (398.0 eV) is higher than that of the conventional thermal CVD  $\text{Si}_3\text{N}_4$ .<sup>12</sup>

The preparation of high quality ultrathin  $\text{SiN}_x$  films can be realized at 300 °C using the Cat-CVD system. In particular, the postdeposition treatments of Cat-CVD  $\text{SiN}_x$  films play a remarkable role in reducing the leakage currents by several orders of magnitude, compared with that of conventional thermal  $\text{SiO}_2$  films of similar EOT, and in improving the quality of the films. The results demonstrate that ultrathin

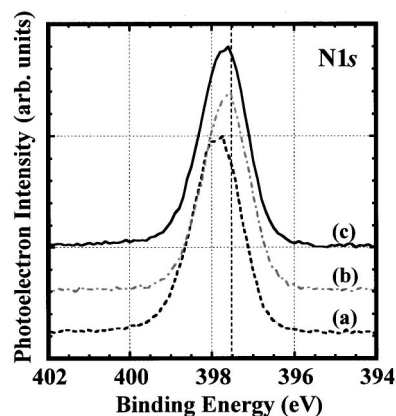


FIG. 6. N 1s XPS spectra from (a) without postdeposition treatments, (b) with postdeposition  $\text{H}_2$  treatments and (c) with postdeposition  $\text{NH}_3$  treatments.

Cat-CVD  $\text{SiN}_x$  films can be used as gate dielectrics for ULSI devices. This technology is highly promising for fabricating future  $\text{SiN}_x$  gate MIS field effect transistors.

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<sup>1</sup>Y. Saito, K. Sekine, M. Hirayama, and T. Ohmi, Ext. Abst. International Conference on Solid State Devices and Materials, 1998, pp. 24 and 25.

<sup>2</sup>S. C. Song, H. F. Luan, Y. Y. Chen, M. Gardner, J. Fulford, M. Alen, and D. L. Kwong, Tech. Dig. Int. Electron Devices Meet., 373 (1998).

<sup>3</sup>H. Matsumura and H. Tachibana, Appl. Phys. Lett. **47**, 833 (1985).

<sup>4</sup>H. Matsumura, Jpn. J. Appl. Phys., Part 1 **37**, 3175 (1998).

<sup>5</sup>S. Okada and H. Matsumura, Jpn. J. Appl. Phys., Part 1 **36**, 7035 (1997).

<sup>6</sup>A. Izumi and H. Matsumura, Appl. Phys. Lett. **71**, 1371 (1997).

<sup>7</sup>A. Izumi, A. Masuda, and H. Matsumura, Thin Solid Films **343,344**, 528 (1999).

<sup>8</sup>W. Kern and D. A. Puotinen, RCA Rev. **31**, 187 (1970).

<sup>9</sup>L. M. Terman, Solid-State Electron. **5**, 285 (1962).

<sup>10</sup>T. P. Ma, IEEE Trans. Electron Devices **45**, 680 (1998).

<sup>11</sup>T. Ogata, M. Inoue, T. Nakamura, N. Tsuji, K. Kobayashi, K. Kawase, H. Kurokawa, T. Kaneoka, Y. Ono, and H. Miyoshi, Tech. Dig. Int. Electron Devices Meet., 597 (1998).

<sup>12</sup>S. R. Kaluri and D. W. Hess, Appl. Phys. Lett. **69**, 1053 (1996).