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Description	

## Analysis on Operation of a F-FET Memory With an Intermediate Electrode

Tran Dang Khoa and Susumu Horita

**Abstract**—An operation model of a ferroelectric gate field-effect transistor memory with an intermediate electrode was proposed and analyzed. Read endurance characteristics of the memory during a consecutive reading was simulated using this model. The simulation results showed good agreement with the experimental data.

**Index Terms**—Capacitor, ferroelectric, ferroelectric devices, ferroelectric film, ferroelectric memory, field-effect transistors (FET).

### I. INTRODUCTION

Ferroelectric gate field-effect transistor (F-FET) memory has been massively investigated thanks to its novel features such as nondestructive, high-operation speed and high packing density [1]. However, F-FET has not been commercialized due to some serious problems, including high operation voltage, short retention time and unstable performance [2]–[4]. In order to overcome these problems, Shimada *et al.* [5] and Horita *et al.* [6] proposed a new operational principle of F-FET memory with an intermediated electrode inserted between the ferroelectric film and the metal–oxide–semiconductor FET (MOSFET) used for data reading, or R-FET. For data writing, an additional MOSFET connected between the intermediate electrode and the source of R-FET is employed, called W-FET. A schematic integrated circuit (IC) of the memory is shown in Fig. 1. Although this new F-FET requires more cell area than the conventional F-FET, it is possible to reduce the cell area by using the common region of source or drain between the two FETs and by fabricating the W-FET over the R-FET with an insulating layer between them like a structure of static random access memory (SRAM) with a thin-film transistor (TFT). During data reading (W-FET is OFF), the memory can be considered as a system of a ferroelectric capacitor  $C_f$  connected in series with the input capacitor  $C_0$  of R-FET. The intermediate voltage  $V_I$  (at the gate of R-FET) can be simply expressed as  $V_I = C_f V_R / (C_f + C_0)$  when a reading voltage  $V_R$  is applied to the system.

When  $V_I$  is equal to the threshold voltage  $V_{th}$  of R-FET, the threshold reading voltage  $V_{TR}$  is equal to  $(C_f + C_0)V_{th}/C_f$ . Assuming that  $C_0$  is independent of voltage and that the polarization–voltage ( $P$ – $V$ ) hysteresis loop of  $C_f$  is approximated as in Fig. 2, the difference of  $V_{TR}$  between the positive remanent polarization  $P_r^+$  and the negative remanent polarization  $P_r^-$  states,  $\Delta V_{TR}$ , which gives guidelines for fabrication of  $C_f$  is calculated as

$$\Delta V_{TR} = V_{TR}^+ - V_{TR}^- = (1 - C_{fl}/C_{fh})(C_0 V_{th}/C_f - V_{fc1}). \quad (1)$$

Here,  $C_{fl}$  and  $C_{fh}$  are linear ferroelectric capacitances from the  $P_r^+$  state, and the  $P_r^-$  state to positive voltage direction, respectively. The  $V_{fc1}$  is called “ferroelectric critical voltage,” which characterizes a voltage at which  $C_f$  changes from  $C_{fl}$  to  $C_{fh}$ . When  $V_{TR}^- < V_R < V_{TR}^+$ , the drain current  $I_D$  of the R-FET is zero for the  $P_r^+$  state and is

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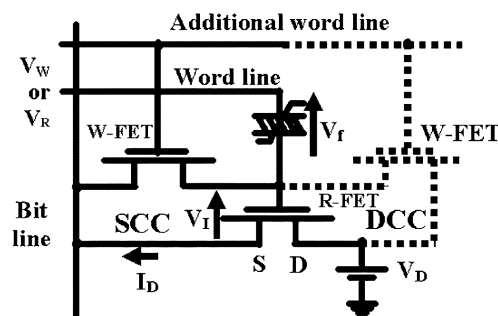


Fig. 1. IC of the new memory. (Dashed line) SCC and DCC, respectively.

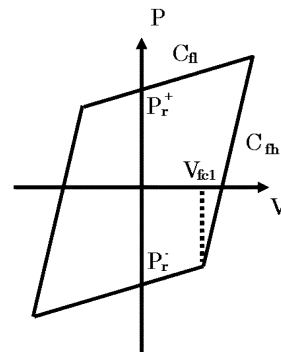


Fig. 2. Approximated  $P$ – $V$  hysteresis loop used to calculate  $\Delta V_{TR}$ .

nonzero for the  $P_r^-$  state. Therefore, by detecting  $I_D$  at a given  $V_R$ , the memory state is decoded.

The detailed merits of the new F-FET memory and experimental data to verify the operational principle had been mentioned in [6]. Fig. 3 shows a schematic model of ideal nondestructive operation of the new F-FET memory for the  $P_r^-$  state, where

- is for retention condition with the memory charge or remanent polarization of  $Q$ ;
- is for reading condition using positive reading pulse voltage;
- is for just finishing reading.

In Fig. 3(b), the applied voltage to  $C_0$  is  $\Delta Q/C_0$ , defining  $\Delta Q$  as a charge supplied from the reading voltage source. In Fig. 3(c), the voltage  $\Delta Q/C_0$  of  $C_0$  acts like a battery in a moment to charge the  $C_f$  with  $\Delta Q$ . So, after reading the memory, the memory state is the same as Fig. 3(a) of the initial state. Therefore, this memory readout is nondestructive. However, actually, due to a leakage current of W-FET in OFF state as shown in Fig. 4 of the equivalent circuit, this new F-FET memory encounters changes of  $V_I$  and  $Q$  during a consecutive data reading, which leads to a short read endurance. As a solution to this issue, we proposed a new configuration, the drain-connected configuration (DCC) as seen in Fig. 1 and Fig. 4 (dashed lines), which has experimentally proven its usefulness in [6].

In this brief, we propose an operation model of the new F-FET memory and analyze its time-dependent output during a consecutive reading. The simulation results in both the source-connected configurations (SCC) and the DCC are compared with the experimental data obtained by using a discrete circuit constructed with a self-made MOSFET and self-deposited ferroelectric film.

### II. OPERATION MODEL

In this model, we neglect the leakage current of  $C_f$  and  $C_0$  as they are assumed to be much smaller than that of W-FET in OFF state.

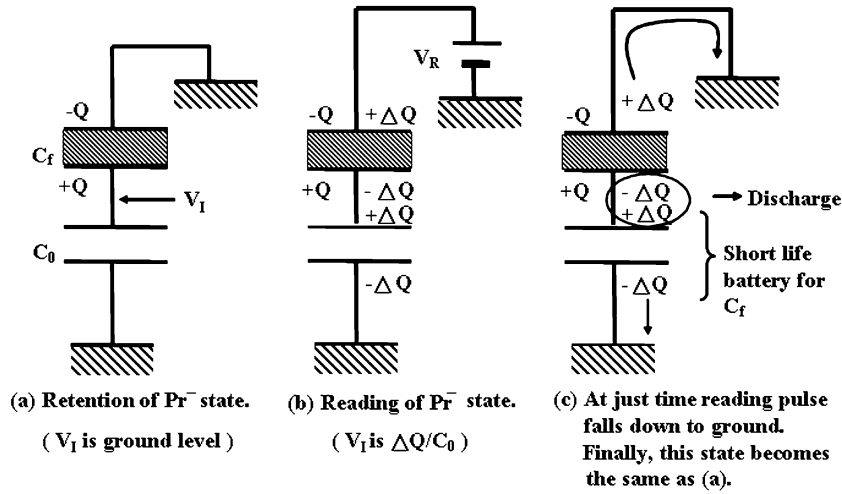


Fig. 3. Schematic model of ideal nondestructive operation of the new F-FET memory for the  $P_r^-$  state and a positive reading voltage  $V_R > 0$ .

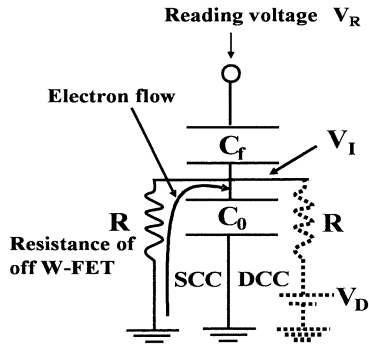


Fig. 4. Equivalent circuit of the new F-FET memory for a positive reading voltage  $V_R > 0$ .

Because the differential capacitors  $C_f$  and  $C_0$  depend nonlinearly on ferroelectric voltage  $V_f$  and  $V_I$ , respectively, when the reading pulse voltage increases from 0 to  $V_R$  on the rising slope of the reading square pulse,  $V_I$  can be calculated as

$$V_I = \int_0^{V_R} \frac{C_f(V_f)}{C_f(V_f) + C_0(V_I)} dV_R. \quad (2)$$

$V_I$  becomes rapidly steady-state just after application of reading pulse in the short term. However, in the long term,  $V_I$  at high reading voltage decreases gradually with the consecutive reading cycle due to the leakage current of W-FET. The decreasing rate is governed by a time constant  $\tau = R(C_f + C_0)$  with  $R$  as a resistance of W-FET in OFF state. Therefore, more reading cycles make  $V_I$  decreased and  $V_f$  increased because reading voltage =  $V_f + V_I$ . This means that  $C_f$ , dependent on  $V_f$ , is varied with reading cycle, in particular, for the  $P_r^-$  state. In addition, when the first reading pulse rises up to  $V_R$  and decreases to zero,  $V_I$  does not fall to zero as normally expected but a voltage  $\Delta V_p$  which indicates that  $V_f = -\Delta V_p$  because of  $V_I + V_f = 0$ , zero reading voltage. Also, from the second reading,  $V_I$  is added by  $\Delta V_p$ . The  $\Delta V_p$  originates from the polarization domains, which do

not return to virgin remanent polarization states once they are switched [6]. Also, since  $V_f$  is increased with reading cycle as mentioned above,  $\Delta V_p$  is possibly increased with it. Defining  $\Delta V_f$  as the increase of  $V_f$  when  $V_f$  is increased due to  $V_I$  decrease during high reading voltage,  $\Delta V_p$  can be expressed by  $\Delta V_p = k \Delta V_f \Delta C_f / (C_f + C_0)$ , where  $\Delta C_f = C_f(V_f) - C_f(0)$ , and  $k$  is the nonreturning domain ratio. Physically,  $\Delta C_f$  means that a pure ferroelectric capacitance is equal to the difference between the total capacitance and the paraelectric capacitance assuming  $C_f(V_f = 0)$  is due to only the paraelectricity and  $k \Delta V_f \Delta C_f$  is the nonreturning domain charge or the remaining charge at the intermediate electrode due to  $\Delta V_f$ .

We calculate  $V_I(t)$  for DCC, where  $t$  is the time from the start of measurement, with consecutive unipolar square voltage pulse train as reading voltage. When the height of the pulse is  $V_R$ , the pulse train is a superposition of an ac part with the amplitude of  $V_R/2$  and a dc offset of  $V_R/2$ . For a linear analysis, the whole range up to the total reading cycle  $N_{max}$  is divided into  $D$  regions with linear systems. Within the  $i^{th}$  region with  $N_i$  reading cycle, the intermediate voltage  $V_{li}(t)$  is calculated in (3), shown at the bottom of the page, where  $S(t) = 1$  during high reading voltage and  $-1$  during zero reading voltage and  $T$  is a period of reading pulse. Here,  $V_{IAC}$  is induced from the ac part of the reading pulse train and  $V_{IT}$  is a sum of the drain bias  $V_D$  and an exponential term which is resulted from the dc offset of the reading pulse train. Also,  $\tau_i$  is time constant equal to  $R(C_{fi} + C_0)$  and  $C_{fi}$  is the mean differential ferroelectric capacitance between  $C_f$  at high reading voltage and at zero reading voltage in the first reading pulse of the  $i^{th}$  region.  $V_{I0i}$  is  $V_{li}$  at the first reading cycle of the  $i^{th}$  region. Also,  $V_{n(i-1)}$  is a sum of  $V_{I(i-1)}$  at the end of the  $(i-1)^{th}$  region and  $\Delta V_{p(i-1)}$  due to  $\Delta V_f$  generated in the  $(i-1)^{th}$  region. That is

$$V_{n(i-1)} = V_{I(i-1)} \left( \sum_{s=1}^{i-1} N_s T \right) + \Delta V_{p(i-1)}. \quad (4)$$

Finally, the intermediate voltage was converted with help of transconductance characteristics of R-FET to output voltage  $\Delta V_0 = I_D R_D$ , where  $R_D$  is drain resistance, compared with the experimental data.

$$V_{li}(t) = \underbrace{0.5(V_{I0i} - V_{n(i-1)})S(t)}_{V_{IAC}} + \underbrace{V_D + [0.5(V_{I0i} - V_{n(i-1)}) + V_{n(i-1)} - V_D] \exp \left[ - \left( t - \sum_{s=1}^{i-1} N_s T \right) \tau_i^{-1} \right]}_{V_{IT}} \quad (3)$$

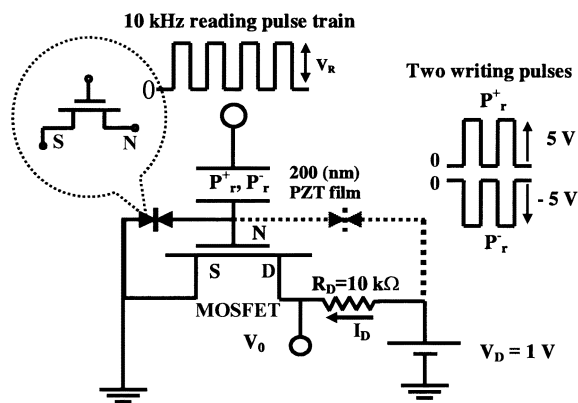


Fig. 5. Experimental circuit and conditions in the read endurance investigation. R-FET is a self-made MOSFET and the W-FET is simulated by twin diodes with typical leakage current of 1 pA at 1 V. The solid line connection of the twin diode is for the SCC and the dash line is for the DCC.

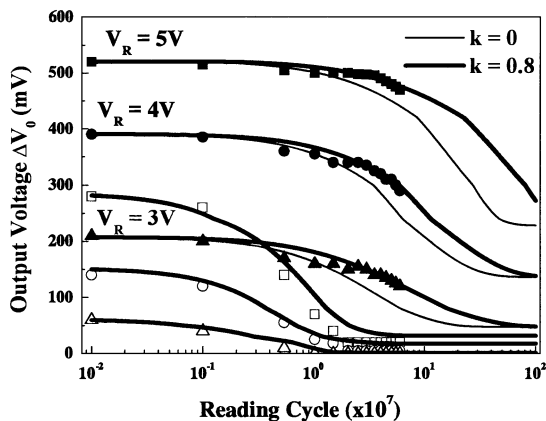


Fig. 6. Read endurance characteristics for SCC. The bold and fine lines are the simulated results for  $k = 0.8$  and  $k = 0$ , respectively. The closed and opened symbols indicate the data for the  $P_r^-$  and  $P_r^+$  states, respectively. The square, circle and triangle marks are denoted experimental data of  $V_R = 5, 4, \text{ and } 3$  V, respectively.

### III. RESULTS AND DISCUSSIONS

The experimental results were obtained from the circuit shown in Fig. 5. The ferroelectric capacitor was a 200-nm-thick epitaxial PZT film on an Si substrate. Its area was  $78.5 \times 10^{-6}$  cm<sup>2</sup>. R-FET is a self-made MOSFET ( $C_0 = 200$  pF,  $V_{th} \approx 1$  V). To simulate W-FET in OFF state, two diodes connected back-to-back in series (called twin diodes) was used for both SCC and DCC (solid and dashed lines in Fig. 5, respectively). Typical leakage current of the twin diode was about 1 pA at 1 V. The writing voltage is two positive or two negative square pulses of 5 V at 10 kHz for the  $P_r^+$  state and  $P_r^-$  state, respectively. The reading voltage is a serial square pulse train of 3, 4, or 5 V at 10 kHz. The leakage currents of the ferroelectric capacitor and the gate oxide of the self-made MOSFET were 0.1 pA and less than 0.01 pA at 1 V, respectively, which were much smaller than that of the twin diode.

The experimental and simulation results of  $\Delta V_0$  as a function of reading cycle for SCC are shown in Fig. 6 and for DCC in Fig. 7. (The experimental data and preparation of the used ferroelectric film had been mentioned in [6].) In SCC, for the  $P_r^-$  state,  $\Delta V_0$  is constant up to about  $3.0 \times 10^7$  reading cycles, but starts decreasing with more reading cycles. For the  $P_r^+$  state,  $\Delta V_0$  is even decreased faster and finally reached a saturation of nearly zero after about  $10^7$  reading cycles. The decrease of  $\Delta V_0$  is resulted from  $V_f$  decrease due to the loss

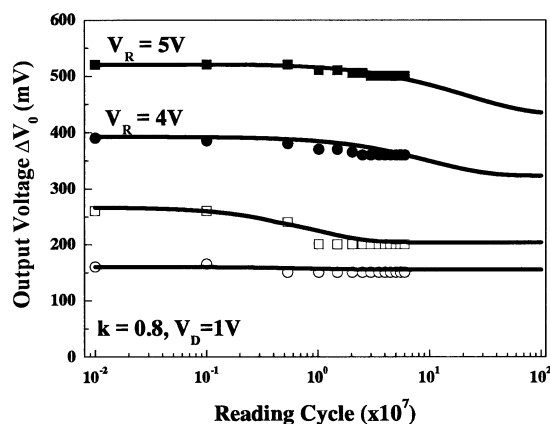


Fig. 7. Read endurance characteristics for DCC. The symbols definitions are the same as those in Fig. 6.

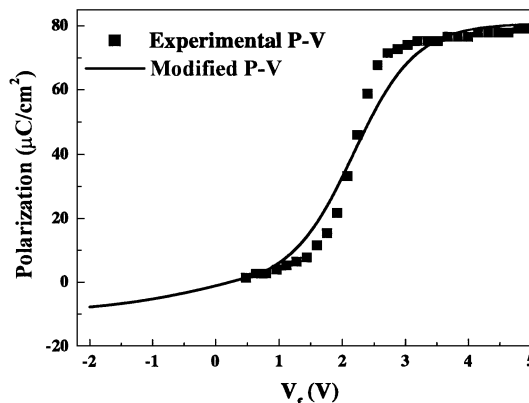


Fig. 8. Experimental and modified  $P$ - $V$  characteristics used in the simulation. The experimental data were measured by a ramping voltage from 0 to 5 V in one direction.

of charges at the intermediate electrode through the twin diode. On a contrary,  $\Delta V_0$  for both polarization states in DCC are almost constant within the experimental range of  $6 \times 10^7$  reading cycles.

To carry out the simulation, the differential capacitance  $C_f$  is determined from a corresponding  $P$ - $V$  hysteresis loop measured by a Sawyer-Tower circuit with ramping voltage. For the  $P_r^+$  state, the  $C_{fp}$  was calculated from an experimental  $P$ - $V$  loop and was found to be about 200 pF and hardly depends on  $V_f$ . For the  $P_r^-$  state, the  $C_{fn}$  were determined from a modified  $P$ - $V$  loop based on an actual experimental  $P$ - $V$  loop as in Fig. 8. This is because the ferroelectric capacitor during a consecutive reading is subjected to many switching cycles so that the  $P$ - $V$  characteristics are somewhat modified and differs from the loop determined from a single cycle. It can be seen from Fig. 7 that the simulation results are in good agreement with the experimental data for  $k = 0.8$ , which means that our model is physically acceptable. Also, the difference in tendency of  $\Delta V_0$  between the  $P_r^-$  and  $P_r^+$  states can be explained as follows. There are three factors contributing to  $\Delta V_0$ : nonreturning domain charge as origin of  $\Delta V_p$  in the simulation, the  $C_f$  and the time constant  $\tau$  which depends on the  $C_f$ . The reasons for larger  $\Delta V_0$  in the  $P_r^-$  state than in the  $P_r^+$  state are 1)  $C_{fn}$  larger than  $C_{fp}$  and 2) large  $\Delta V_p$  for the former. This larger  $\Delta V_p$  is due to larger  $C_{fn}$  which means that more ferroelectric domains are subject to switching. The faster decrease of  $\Delta V_0$  in the  $P_r^+$  state than that in the  $P_r^-$  state is due to 1) shorter  $\tau$  and 2)  $\Delta V_p = 0$  in the  $P_r^+$  state. The shorter  $\tau$  is due to  $C_{fp}$  smaller than  $C_{fn}$ .  $\Delta V_p = 0$  in the  $P_r^+$  state is due to  $\Delta C_f = 0$ . Further, in the  $P_r^-$  state, because a higher  $V_R$  gives a

higher  $V_f$  so that the  $C_f$  is increased,  $\tau$  becomes longer and the onset of saturation of  $\Delta V_0$  is extended by increasing  $V_R$ .

According to the simulations, for both SCC and DCC,  $\Delta V_0$  finally reaches a saturation corresponding to a saturation value of  $V_I$ ,  $V_I(t \rightarrow \infty) \equiv V_{ISS} = C_{f\infty} V_R / [2(C_{f\infty} + C_0)] + V_D$ , where  $C_{f\infty}$  is the  $C_f$  at a saturated  $V_f$ . Because  $V_{ISS}$  of DCC is  $V_D$  higher than that of SCC,  $\Delta V_0$  in DCC saturates at higher value, i.e., DCC is a better configuration in term of read endurance.

Physically, in DCC, positive charges are supplied from the drain or discharged from the intermediate electrode depending on a competition between the  $V_D$  and the  $V_I$ . During the reading voltage is high,  $V_I$  is normally higher than  $V_D$ . Positive charges are lost from the intermediate electrode to the drain. When the reading voltage is zero,  $V_I$  is lower than  $V_D$ , positive charges are supplied to the intermediate electrode. This helps maintain a high  $V_I$  against reading cycle and lead to a better read endurance for DCC.

#### IV. CONCLUSION

An operation model of a ferroelectric gate field-effect transistor memory (F-FET) has been proposed and analyzed by a simulation. The simulation results were compared to the experimental data and show a good agreement with each other. It was found that, the read endurance is mainly decided by the time constant which is dependent on the ferroelectric capacitances of the memory. In SCC, the memory suffers a short read endurance due to leakage current of W-FET in OFF state. In DCC, the read endurance is improved because positive charges are supplied from the drain to the intermediate electrode, which keeps the intermediate voltage decreasing at a lower rate and saturates at a higher value.

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## A-Si:H-Based LCLV With an CdTe and VOPc Multiple Absorption Layers

Qi Kangcheng, Cheng Jianbo, Ge Changjun, and Wang Jimin

**Abstract**—A-Si:H-based liquid crystal light valve (LCLV) is described in this brief. This LCLV employs cadmium telluride (CdTe) and Vanadyl phthalocyanine (VOPc) multiple absorption layers. The multiple absorption layers have high absorption ability in the visible and near-infrared range, which ensures the LCLV to have a high sensitivity and high reading to writing light isolation ratio. Therefore the LCLV with CdTe and VOPc multiple absorption layers has a higher performance compared with a valve with only a CdTe absorption layer. The LCLV has a peak response at the wavelength of 700 nm and is suitable for projection displays.

**Index Terms**—Absorption layer, cadmium telluride (CdTe), liquid crystal light valve (LCLV), projection displays, Vanadyl phthalocyanine (VOPc).

#### I. INTRODUCTION

Liquid Crystal Light Valves (LCLVs) are devices suited for wavelength conversion, incoherent-to-coherent light conversion and for image amplification. Therefore, these devices are applied in optical processing [1], optical correlation research [2], and in projection displays [3]. The following properties makes LCLVs particularly attractive: high photo-to-dark conductivity ratio, large-area coverage, excellent spatial resolution, appropriate wavelength response, thin-film type, and low-temperature deposition of a-Si:H film. A-Si:H film is sensitive to red and near-infrared (IR) light, so, an a-Si:H-based LCLV is suitable for being applied in wavelength conversion equipments and in projection displays. In projection displays, light from CRTs or other sources representing the red, green, and blue primary light is projected onto the photoconductive layer of the corresponding LCLV. The resistance of the photoconductive layer decreases due to the generation of carriers (electrons and holes) that are formed by the incident light. Decrease of the resistance of the photoconductive layer will increase the voltage applied to the liquid crystal (LC) layer. The reading light generated by a light source is polarized and divided into red, green, and blue beams with high intensity. Each beam incidents upon its corresponding LCLV and is reflected. Because the reading light has a high intensity, the writing image can be considered as being amplified.

The reading light that penetrates through the reflection layer can also generate carriers just as the reading light. This effect is equivalent to the addition of a constant light intensity to the writing image, which will decrease the modulation of the writing image. As a result, the output image will be blurred. In LCLVs, there is an absorption layer to absorb the penetrating reading light. The photosensitivity of the photoconductive layer, the absorption capability of the absorption layer and the reflectivity of the reflection layer together determine the amplification of the LCLV. The best way to get high amplification is increasing the reflectivity of the reflection layer and the absorption ability of the absorption layer. In this brief we present a novel a-Si:H-based LCLV employing a structure of CdTe and VOPc absorption layers, which have never been reported before.

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