High-performance C_{60} thin-film field-effect transistors with parylene gate insulator

Yoshihiro Kubozono,[1,a)] Simon Haas,[2] Wolfgang L. Kalb,[2] Pierre Joris,[2] Fabian Meng,[2] Akihiko Fujiwara,[3] and Bertram Batlogg[2,b)]
[1]*Research Laboratory for Surface Science, Okayama University, Okayama 700-8530, Japan*
[2]*Laboratory for Solid State Physics, ETH Zürich, 8093 Zürich, Switzerland*
[3]*Japan Advanced Institute of Science and Technology, Ishikawa 923-1292, Japan*

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C_{60} field-effect transistors (FETs) have been fabricated with parylene gate dielectric on Si/SiO_2, on polyethylene terephthalate, and commercially available transparent sheet substrates. The best performance of the C_{60} FET device is achieved with parylene as gate dielectric: field-effect mobility of 0.41 $cm^2\,V^{-1}\,s^{-1}$ and on-off ratio of $\sim 10^7$. The excellent FET characteristics are recorded without any annealing, and the devices were kept in He atmosphere after an exposure to air. This result suggests the parylene gate dielectric to be highly H_2O repellent. The mechanical flexibility and air-exposure effect were studied for the C_{60} FET with parylene gate dielectric. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2959819]

Much effort has been directed to the development of *n*-channel enhancement-type field-effect transistor (FET) devices with organic molecules because the devices are compatible with mechanical flexibility and large-area coverage.[1,2] These properties are the most important advantages expected in the FET devices with organic molecules (organic FETs), and the mechanical flexibility additionally ensures some shock resistance, i.e., the device is not easily destroyed by a mechanical shock. For the realization of flexible organic FET devices, polymeric gate insulators and substrates are indispensable. Some materials such as C_{60},[3–6] pentacene,[7–12] and rubrene[13–17] are used as active layers in organic FET devices owing to their high field-effect mobility μ. C_{60} and pentacene show a μ value of ~ 1 $cm^2\,V^{-1}\,s^{-1}$ in thin film FET devices,[3–12] while rubrene shows a very high μ of ~ 20 $cm^2\,V^{-1}\,s^{-1}$ in single crystal FET devices.[13–17] We recently fabricated C_{60} thin film FET devices with a polyimide gate insulator, exhibiting a μ of $\sim 10^{-2}$ $cm^2\,V^{-1}\,s^{-1}$.[18] This value is relatively high among the *n*-channel organic FET devices with polymer gate insulators.[19–21] However, it is still lower by one order of magnitude than that, ~ 0.5 $cm^2\,V^{-1}\,s^{-1}$, in C_{60} thin film FETs with SiO_2 gate insulator.[4–6]

In this study, C_{60} thin film FET devices with parylene gate insulator have been fabricated on Si/SiO_2 and polyethylene terephthalate (PET) substrates as well as on commercially available transparent sheets, and their transport properties have been measured in He atmosphere, after exposing the devices to ambient air. Mechanical bending and air-exposure effects on μ were investigated for the C_{60} FET with parylene dielectric insulator.

C_{60} thin film FET devices in this study were fabricated in top contact configuration, as shown in Fig. 1(a). The commercially available $Si(100)/SiO_2$ wafer, PET, and transparent sheets were used as substrates after washing with acetone and isopropanol. For the gate electrodes, the Au thin films with thickness of 45 nm were formed on top of a thin Cr adhesion layer (5 nm) by thermal deposition on the Si/SiO_2 substrates, and Au thin films of 50 nm were formed on PET and transparent sheets. The parylene gate dielectric films were applied on the Au-coated substrates by polymerization of parylene-C by use of a homemade reactor. In this reactor, parylene-C was thermally evaporated at 120 °C, and the parylene-C was introduced into the quartz tube heated up to 680 °C to induce the polymerization. The parylene polymer films were formed on the Au-coated substrates maintained at room temperature. The base pressure at all stages was kept to ~ 40 Torr by a dynamical pumping. The films thickness was estimated from the weight of the parylene films formed on the reference glasses placed near the device substrates. The thicknesses of parylene films were 1.00–1.37 μm, and capacitance per area C_0 was estimated from the thickness and the dielectric constant of parylene (ε_x=3.10). 50 nm thick C_{60} thin films were formed on the parylene-coated substrate, and finally the source and drain Au electrodes of 50 nm were evaporated on top of the C_{60} thin films. The films of Cr, Au, and C_{60} are thermally deposited at 10^{-6} Torr background pressure.

The complete FET devices were finally transferred through air to a He filled glove box (<0.1 ppm O_2 and <1 ppm H_2O), where the FET characteristics were measured with a semiconductor parameter analyzer (HP 4155A). It is worth pointing out that the devices were not annealed in vacuum, as usually done for C_{60} based devices. In the measurement of air-exposure effect, the C_{60} FET device with parylene gate dielectric was exposed to air at ~ 300 K and relative humidity of 29% and the FET characteristics were

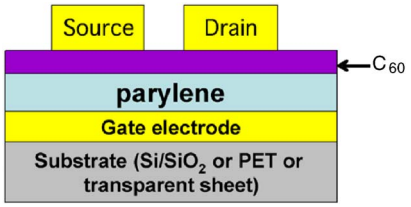

FIG. 1. (Color online) Device structure of C_{60} FET with parylene dielectric.

a)Electronic mail: kubozono@cc.okayama-u.ac.jp.
b)Electronic mail: batlogg@phys.ethz.ch.

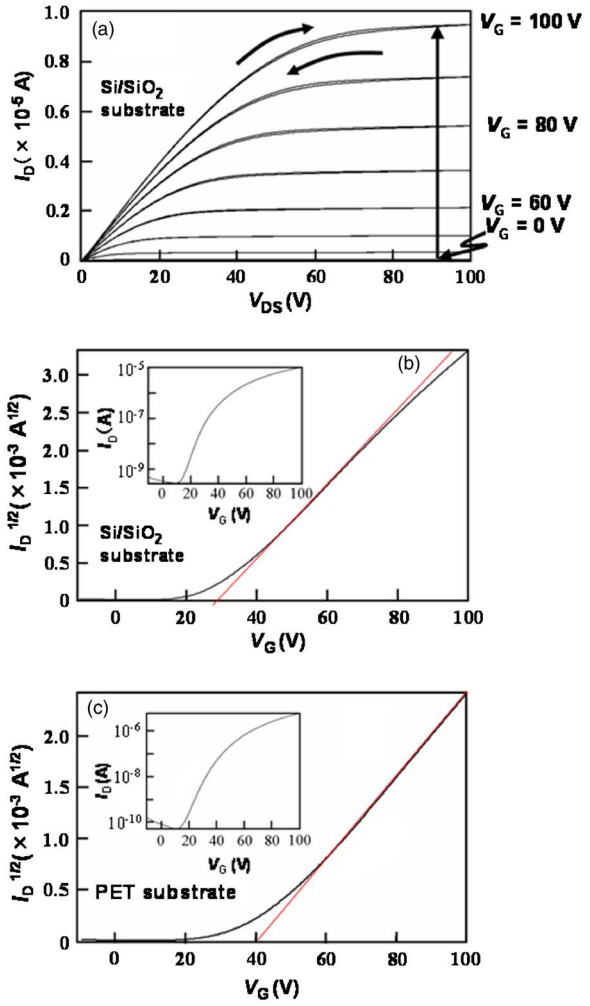

FIG. 2. (Color online) (a) Output and (b) transfer curves for a C_{60} FET with parylene dielectric on Si/SiO_2 substrate. (c) Transfer curve for a C_{60} FET with parylene dielectric on PET substrate. Transfer curves are shown at $V_{DS}=100$ V (saturation regime). Insets of (b) and (c): transfer curves on a logarithmic scale. Output curves were measured in both forward (bias-increase) and reverse (bias-decrease) measurement-modes, while transfer curves were measured only in forward measurement mode.

measured by a semiconductor parameter analyzer (Keithley 4200-SCS).

We fabricated four C_{60} FETs with 1.21 μm parylene films and four C_{60} FETs with 1.05 μm parylene films on Si/SiO_2 substrates. Typical FET characteristics for C_{60} FET with parylene dielectric on Si/SiO_2 substrate are shown in Fig. 2(a). All fabricated FETs exhibited *n*-channel normally off FET behavior. The μ, on-off ratio, threshold voltage V_{th}, and subthreshold swing S were determined from the transfer characteristics in the saturation regime. A typical $I_D^{1/2}$-V_G plot is shown in Fig. 2(b). The μ values for these devices are between 0.1 and 0.4 $cm^2\ V^{-1}\ s^{-1}$. The on-off ratio is in the range of 10^3–10^7. As a common trend, the μ was found to be higher for thinner parylene films. For the four C_{60} FET devices with a 1.21 μm parylene film, the μ was 0.15 ± 0.03 $cm^2\ V^{-1}\ s^{-1}$, while for the four devices with a 1.05 μm parylene film, the μ was 0.32 ± 0.07 $cm^2\ V^{-1}\ s^{-1}$.

The threshold voltage V_{th} was 29 ± 2 V for the C_{60} FET devices with 1.05 μm parylene films, and 47 ± 3 V for 1.21 μm parylene films. The higher V_{th} for the thicker parylene insulator can be qualitatively understood by a decrease in C_0 of gate dielectric because the smaller C_0 requires a higher V_G to fill the trapping states which is closely related to the V_{th}. No similar trend could be observed for the S. The lowest S was 1.2 V/decade, and $SC_0=2.3$ nF V/(cm^2 decade).

It is particularly noteworthy that the very good FET characteristics in our devices are easily observed without any annealing, in spite of the exposure to air during transferring them from the evaporation chamber to the glove box. For comparison, no FET behavior in C_{60} FET devices with SiO_2, polyimide, and $Ba_xSr_{1-x}TiO_3$ gate insulators could be observed previous to annealing after the devices were exposed to air for a few minutes. The elimination of O_2 and H_2O (especially the elimination of H_2O) was absolutely required for *n*-channel FET operation.[3–6,18] However, our parylene films have never required such a pretreatment, and the annealing of the device at 100 °C at 10^{-6} Torr for 44.5 h even caused a device degradation: μ values of 0.18 and 0.11 $cm^2\ V^{-1}\ s^{-1}$ before annealing were reduced to 0.054 and 0.049 $cm^2\ V^{-1}\ s^{-1}$, respectively. An *n*-channel operation in C_{60} FETs with parylene gate dielectric without the need for annealing is one of important results of this study.

The highest μ value (0.41 $cm^2\ V^{-1}\ s^{-1}$) in C_{60} FET devices with parylene dielectric is obtained without any prior annealing after exposure to air for ~15 min, and it is comparable to the highest μ, ~0.5 $cm^2\ V^{-1}\ s^{-1}$, except for epitaxial C_{60} thin film FET with buffer layer of pentacene[22] or special polymers.[23] Here, it should be noted that the previous C_{60} FET devices exhibiting a high μ value were fabricated without any exposure to air,[4,6] or the characteristics were measured after a sufficient elimination of H_2O by vacuum annealing.[3,5] It follows, therefore, that the surface of parylene films is highly H_2O repellent and through the strong reduction of H_2O-related traps the combination of parylene with organic semiconductors can be highly beneficial for the charge carrier mobility in FET devices.

Four C_{60} FETs with parylene gate dielectric on PET substrate were fabricated, and all FETs showed *n*-channel normally off behavior. For these devices, the μ value was 0.28 ± 0.03 $cm^2\ V^{-1}\ s^{-1}$ and the on-off ratio was 10^5–10^6. The characteristics are consistent with those of the C_{60} FET with parylene dielectric on Si/SiO_2 substrates. The FET parameters were determined from the transfer curves in saturation with $V_{DS}=100$ V [Fig. 2(c)]. The C_{60} FETs on the PET substrates are flexible device, and μ of 0.33 $cm^2\ V^{-1}\ s^{-1}$ recorded for one FET is one of the highest μ reported for flexible *n*-channel FET devices with thin films of organic molecules as the active layer.[18–21] The value of 0.33 $cm^2\ V^{-1}\ s^{-1}$ is also comparable to the highest values (0.26–1.0 $cm^2\ V^{-1}\ s^{-1}$) in *p*-channel flexible FETs with pentacene thin films.[12,24,25]

The effect of mechanically bending of the flexible FET device has been investigated by use of an C_{60} FET with parylene dielectric (thickness of 1.00 μm) formed on Au-covered commercially available transparent sheet. The μ, on-off ratio, and V_{th} of this device were 0.072 $cm^2\ V^{-1}\ s^{-1}$, 10^4, and 42 V which is somewhat lower than those of the C_{60} FET devices fabricated on the PET substrates. The dependence of μ on the mechanical bending is shown in Fig. 3(a). The mechanical bending is performed along the direction parallel to current flow, as shown schematically in the inset of Fig. 3(a). The μ value decreases gradually with decreasing bending radius r. At the minimal bending radius of 2 mm, μ became 0.030 $cm^2\ V^{-1}\ s^{-1}$, which is ~40% of the initial

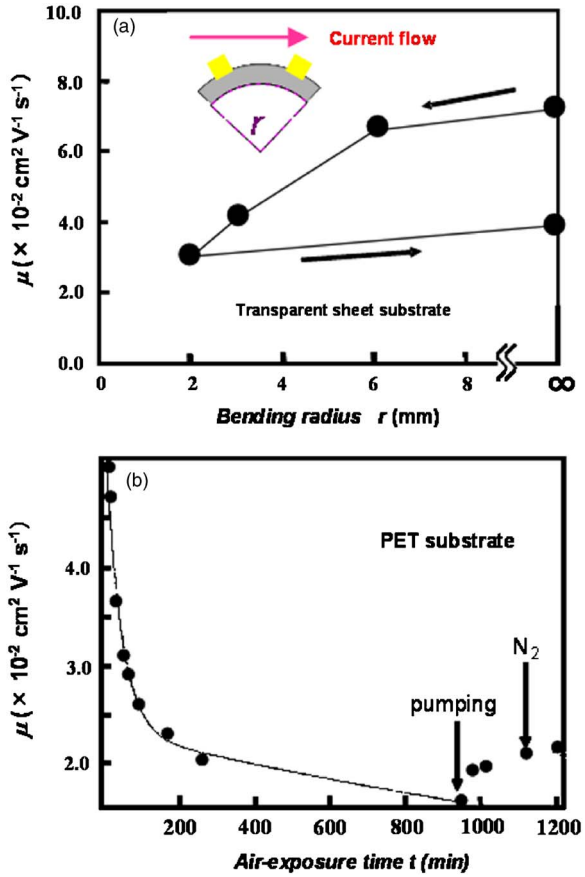

FIG. 3. (Color online) (a) Mechanical bending effect on μ for C_{60} FET with parylene dielectric on transparent sheet and (b) air-exposure effect on μ for C_{60} FET with parylene dielectric on PET.

value (0.072 $cm^2\ V^{-1}\ s^{-1}$). After the device was bent down to r of 2 mm, it was again returned to $r=\infty$. The μ value increased up to 0.039 $cm^2\ V^{-1}\ s^{-1}$, but did only recover to ~55% of the initial value. The mechanical bending of device down to r of 2 mm resulted in irreversible damage to the C_{60} FET device. Nevertheless, it is interesting to note that the μ remains essentially constant down to $r=6$ mm [Fig. 3(a)], which induces sufficient flexibility of this device. The on-off ratio and V_{th} values of the flexible device did not change when r was decreased down to 2 mm.

One of four C_{60} FET devices with 1.37 μm parylene films on the PET substrates, was bent parallel to the direction to the current flow. The direction is the same as that shown in the inset of Fig. 3(a). The device showed a μ of 0.29 $cm^2\ V^{-1}\ s^{-1}$ before the mechanical bending, which decreased to 0.016 $cm^2\ V^{-1}\ s^{-1}$ (5.5% of the flat device) at r of 2 mm. Thus, the damage for C_{60} FET on PET caused by mechanical bending was larger than that on the transparent sheet, which can be attributed to the fact that PET substrate used in this study was thicker and more rigid than transparent sheet.

Air-exposure-time (t) dependence of μ for the C_{60} FET with parylene dielectric on PET substrate is shown in Fig. 3(b). The μ-t plot showed a biexponential decay [$\mu \sim A_1 \exp(-t/\tau_1)+A_2 \exp(-t/\tau_2)$], with the lifetime $\tau_1 = 17$ min and $\tau_2 = 13\,000$ min, $A_1/A_2 = 1.0$, and the FET device was found to operate at least for more than 15 h under the atmospheric conditions. In contrast, in general FET characteristics cannot be observed in C_{60} FET with SiO_2 gate dielectric even after a short-time exposure to air for less than 1 h. The origin of the biexponential decay for μ is not clear at present, but we can at least stress that the surface of parylene is highly H_2O repellent in comparison with that of SiO_2. As shown in Fig. 3(b), the μ value slightly increased either when air in the measurement cell was dynamically pumped down to 10^{-6} Torr or when air was replaced by dry N_2 gas.

In conclusion, the C_{60} thin film FET devices with parylene gate dielectric show an excellent FET performance with mechanical flexibility and *n*-channel operation for more than 15 h under atmospheric conditions.[3–6] In this study, it has been demonstrated that C_{60} FET with parylene gate dielectric has a possible application for practical organic electronics which are available in atmospheric conditions.

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