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SIMULATED THROUGHPUT EFFICIENCY OF TD-SAW ARQ SYSTEM IN DIGITAL MOBILE RADIO

Indexing terms: Telecommunications, Mobile radio systems, Digital communication systems, Radiocommunication

Computer simulation results for the throughput efficiency of stop-and-wait automatic-repeat-request with time diversity reception (TD-SAW ARQ) are presented for digital mobile radio channels. It is shown that the efficiency η in the TD-SAW ARQ system does not decrease as much as in the SAW ARQ system, when the maximum Doppler frequency f_D becomes large.

Introduction: In recent years, the need for error-free data communication over mobile radio channels has been increasing significantly. However, in mobile radio, multipath fading appears on receiver signals owing to multipath propagation resulting from reflection of the transmitted waves by buildings. One efficient method for reducing the fading effect is forward error correction (FEC). Although it is widely recognised that FEC can improve bit error rate performance, error-free transmission can hardly be achieved by FEC alone.

A systematic strategy for eliminating the effect of the bit errors occurring in the received data is automatic-repeat-request (ARQ). In the ARQ system, an error control code is used for correcting and detecting errors. The receiver requests retransmission via a feedback channel when any uncorrectable errors are found in the received data block. Various ARQ systems have been proposed by many researchers.[1–3] Throughput efficiencies for these ARQ systems have been analysed in Rayleigh fading channels.[4] However, if the actual speed of motor vehicles is taken into consideration, the efficiency seems to be insufficient for real data communication.

Recently, Adachi *et al.*[5,6] have presented a new method, time diversity (TD)-ARQ, for improving the efficiency in digital mobile radio using received signal strength information (RSSI). In the TD-ARQ system, the receiver stores the received vector and the RSSI values corresponding to each bit in a received block in memory, and requests retransmission if the received vector is decoded as erroneous. The stored RSSI values are compared with those corresponding to the bits in the newly received (retransmitted) vector. The bits in the stored vector with RSSI values lower than those in the newly received block are replaced, as in the time diversity system, by the retransmitted bits, and then the reconstructed vector is decoded. If the reconstructed vector is decoded as erroneous, retransmission is requested again. The TD-ARQ concept can be incorporated into various ARQ systems.

This letter applies the TD-ARQ concepts to stop-and-wait (SAW) ARQ and presents computer simulation results for the efficiencies in the slow Rayleigh fading channels encountered in mobile radio. A comparison is then made with a conventional SAW ARQ scheme.

Throughput efficiency: Time-varying Rayleigh envelopes were computer-simulated based on a model in which a mobile station moves with constant speed and many multipath waves with identical amplitude and uniformly distributed phase come from all directions. The ARQ protocol was carried out in the simulated non-frequency-selective Rayleigh fading channel assuming noncoherent FSK modulation. A cyclic redundancy code (CRC), which has 16 parity check bits, was assumed for the error detection. The feedback channel was assumed to be error-free. This assumption is feasible because only 1-bit information (positive and/or negative acknowledgments) is sent through the feedback channel.

In mobile radio applications the propagation delay is very small compared with terrestrial or satellite communication systems. Therefore the idle time, during which the transmitter waits for a response from the receiver, is spent running programs in the transmitter and receiver for ARQ protocol control.

Sketches of the computer simulation results for the efficiency η against $f_D T$, where T^{-1} is the bit rate, and the average received signal/noise power ratio (SNR), are shown in Fig. 1*a* for SAW ARQ and in Fig. 1*b* for TD-SAW ARQ, when the $(N, K) = (1024, 1008)$ code is used for error detection, and the round-trip delay time × bit rate = 64 bits. All

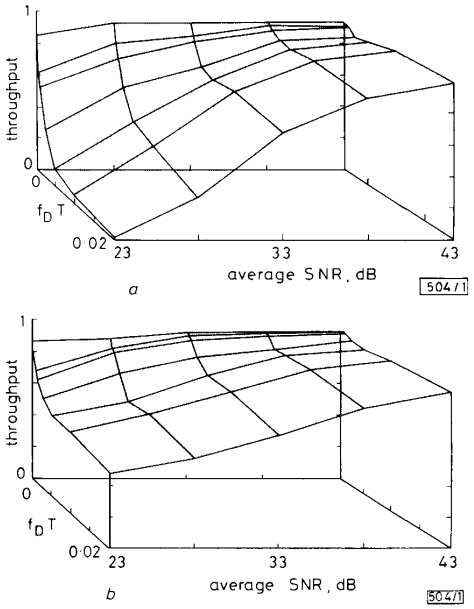

Fig. 1 *Computer simulation results for (a) SAW ARQ and (b) TD-SAW ARQ*
Round-trip delay = 64 bits, (1024, 1008) code

the error patterns are assumed to be detected, as in References 2 and 3. The efficiencies approach $\eta_{max} = (K/N)/\{1 + (\text{round-trip delay time} \times \text{bit rate})/N\} = 0{\cdot}926$ as the average SNR becomes large.

It is widely recognised that the channel capacity of a memoryless channel is lower than that of memory channels such as mobile radio channels without bit interleaving. A Rayleigh fading channel approaches being memoryless as $f_D T$ becomes large. Therefore, the efficiency in ARQ systems for large $f_D T$ is worse than that for small $f_D T$. This feature is clearly indicated in the Figures. However, the efficiency in the TD-SAW ARQ system for large $f_D T$ does not decrease rapidly, as observed in the SAW ARQ system. This is because the more times the retransmission is repeated, the more the error probability of the bit in the reconstructed block is reduced by time diversity.

It is found from the Figure that improvement in the efficiency is greater using TD-SAW ARQ for large $f_D T$ than for small $f_D T$. This is because a greater reduction in bit error probability is obtained by time diversity, as the correlation between RSSI values corresponding to each transmission becomes smaller. The smaller fading correlation can be achieved by larger $f_D T$. For example, we consider two cases in which the bit rate is 16 kbit/s and the vehicle is moving at a speed of 102 km/h, which corresponds to $f_D T = 0{\cdot}01$ for a carrier frequency of 1·5 GHz, and a speed of 26 km/h which corresponds to $f_D T = 0{\cdot}025$. When the average SNR = 23 dB and the block size $N = 1024$, the efficiency for TD-SAW ARQ

is about 0·5 both for $f_D T = 0{\cdot}01$ and 0·0025, while that for SAW ARQ decreases from 0·35 to 0·05 when $f_D T$ varies from 0·0025 to 0·01.

Optimal block size: When the block size N is small, the overhead due to the round-trip delay time and the CRC check bits degrade the efficiency. On the other hand, when N is too large, the increase in the probability of retransmission degrades the efficiency. Therefore, an optimal block size exists at which the efficiency can be maximised. The efficiencies in SAW and TD-SAW ARQ systems against block size N are shown in Fig. 2 for $f_D T = 0{\cdot}0025$. The optical block size was

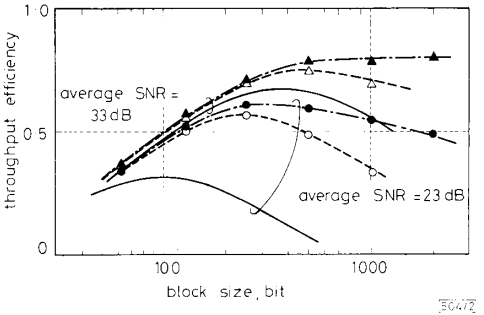

Fig. 2 *Throughput efficiency against block size for SAW and TD-SAW ARQ*

Round trip delay = 64 bits, simulation results, $f_D T = 0{\cdot}0025$
○△ SAW ARQ ●▲ TD-SAW ARQ
——— theoretical curve for SAW ARQ in memoryless channel

given by Morris[7] for a memoryless channel, and is also plotted in the Figure. It is found from the Figure that not only the efficiencies are improved over those of a memoryless channel, but also that the optimal block size is enlarged. When the average SNR is 23 dB, the optimal block size for the TD-SAW ARQ system is about 300 bits. This is almost the same as the optimal size in the SAW ARQ system, while it is about 100 bits for the memoryless channel.

It can be seen from the Figure that an efficiency nearly equal to the optimal value can be achieved over a broader range of N for TD-SAW ARQ compared with SAW ARQ. This means that communication efficiency is not degraded as severely for the TD-SAW ARQ system when the block size is not optimal.

Conclusion: The throughput efficiency in a digital mobile radio channel for TD-SAW ARQ was evaluated through computer simulation. As the maximum Doppler frequency becomes large, the efficiency η for the TD-SAW ARQ system is not degraded as is observed in the SAW ARQ system. Therefore, data communication with reasonable throughput can be achieved by TD-SAW ARQ, even when the vehicle velocity changes.

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PARITY GENERATOR CIRCUIT USING A MULTISTATE RESONANT TUNNELLING BIPOLAR TRANSISTOR

Indexing terms: Semiconductor devices and materials, Bipolar devices, Tunnelling, Logic devices

A four-bit parity generator circuit using a single resonant tunnelling bipolar transistor (RTBT) exhibiting two negative transconductance regions in the characteristics, is demonstrated. The circuit uses only one transistor as compared to 24 needed in conventional logic. The present circuit also provides significant advantages over previous parity generator circuits using resonant tunnelling diodes. The same circuit, when used with only two input bits, will act as an exclusive-NOR gate.

Resonant tunnelling (RT) devices with multiple negative differential resistance have been of considerable interest in recent years as functional devices for circuit applications.[1–6] Various circuits involving reduced complexity have been demonstrated so far.[2–4] However, all these circuits were constructed using two terminal RT devices, and thus suffered from lack of gain and input/output isolation. Recently, we have demonstrated a resonant tunnelling bipolar transistor (RTBT) exhibiting multiple negative differential resistance (NDR) and negative transconductance.[7,8] In this letter we present a 4-bit parity generator using a single resonant tunnelling bipolar transistor (RTBT) with two peaks in the current/voltage (I/V) characteristics that offers dramatic reduction in the number of components over conventional parity checkers.

The device structure, grown lattice matched to an n^+ InP substrate by molecular beam epitaxy, is essentially a $Ga_{0.47}In_{0.53}As$ *npn* transistor with two $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ RT double barriers (DBs) in the emitter, as described in References 7 and 8.

Fig. 1*b* shows the common-emitter transfer characteristic of a transistor with two DBs in the emitter taken at 77 K with collector–emitter bias $V_{CE} = 4{\cdot}5$ V. As discussed in References 7 and 8, at a constant V_{CE}, as the base emitter voltage V_{BE} is increased, the emitter current and hence the collector current

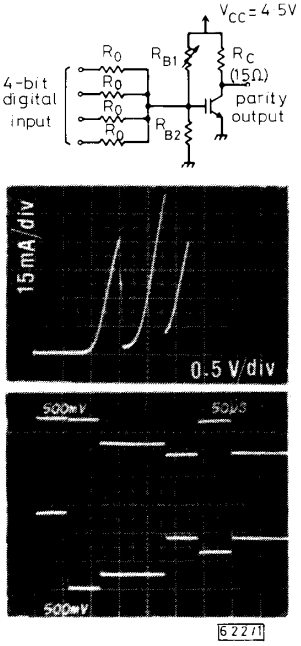

Fig. 1

a Four-bit parity generator circuit using an RTBT ($R_0 = 15\,k\Omega$, $R_{B1} \sim 6{\cdot}9\,k\Omega$, $R_{B2} = 2{\cdot}4\,k\Omega$ and $R_C = 15\,\Omega$)
b I_C/V_{BE} curve with constant $V_{CE} = 4{\cdot}5$ V
c Collector (top trace) and base (bottom trace) waveforms in parity generator circuit, at 77 K