Epitaxial Lift-Off of InGaAs/InAlAs Metamorphic High Electron Mobility Heterostructures and Their van der Waals Bonding on AlN Ceramic Substrates

Yonkil Jeong, Masanori Shindo, Masashi Akabori*, and Toshi-kazu Suzuki†

Center for Nano Materials and Technology,
Japan Advanced Institute of Science and Technology (JAIST),
1-1 Asahidai, Nomi, Ishikawa 923-1292, Japan

We have carried out epitaxial lift-off (ELO) of $In_{0.57}Ga_{0.43}As/In_{0.56}Al_{0.44}As$ metamorphic high electron mobility heterostructures and their van der Waals bonding (VWB) on AlN ceramic substrates. Using a metamorphic heterostructure with an AlAs sacrificial layer and an InGaAs graded buffer grown on GaAs(001), thin film Hall-bar devices on AlN ceramic substrates were successfully fabricated by ELO and VWB. The Hall-bar devices exhibit very high electron mobilities, such as 11000 cm^2/V-s at room temperature (RT) and 84000 cm^2/V-s at 12 K. The RT mobility is the highest ever reported for ELO devices. This is the first report on ELO for metamorphic devices.

*Present address: Institute of Bio- and Nanosystems (IBN-1), Research Centre Juelich, 52425 Juelich, Germany

†Corresponding author. E-mail address: tosikazu@jaist.ac.jp

Metamorphic crystal growth of lattice-mismatched compound semiconductor systems has attracted much attention, because it can remove the restrictions of the lattice-matching condition between device layers and substrates. In particular, high indium content InGa(Al)As metamorphic devices, such as metamorphic high electron mobility transistors[1–3] and metamorphic heterojunction bipolar transistors,[4,5] on GaAs substrates, which have practical merits in comparison with InP substrates, were extensively developed. We have freedom of choice regarding the indium content in the metamorphic devices, which should be optimized considering the trade-off between speed and power performances.[6,7] One of the most important issues of the metamorphic devices is to reduce unfavorable influences of crystalline defects, because these defects, dislocations and stacking faults, often cause deterioration of device performance. Therefore, thicker metamorphic buffer layers are employed to obtain lower defect density in the device layers. However, there are problems associated with the thick buffers containing high-density defects, such as increasing growth costs, high thermal resistances, and possible leakage currents or parasitic capacitances. Because of the low thermal conductivity of the GaAs substrates compared with the InP substrates, the thermal resistance in the metamorphic devices is rather problematic.[8] In order to reduce the leakage current or the parasitic capacitance, the material choice for the buffers is restricted.

In this work, for a solution of these problems, we propose an application of epitaxial lift-off (ELO) process to the metamorphic devices. In this process, the device layer is separated from the substrate and the buffer, by selective etching of a sacrificial layer. Accordingly, all of the problems associated with the buffers can be eliminated, and we can reuse the substrate and the buffer for the next growth, reducing the costs. ELO processes are important for heterogeneous integration (HI) in combination with bonding techniques, for example, van der Waals bonding (VWB).[9–13] Thin film compound semiconductor devices, typically with thickness of ~ 1 μm, separated from the original substrates of $\gtrsim 600$ μm thickness by the ELO, can be integrated on arbitrary host substrates. Recycling the original substrate, we can obtain an HI system with the minimized mass of compound semiconductors, which are sometimes harmful materials. Moreover, the ELO process does not need substrate thinning in contrast to the transferred-substrate process.[14,15] Therefore, the ELO technology is favorable also from the viewpoint of industrial waste reduction and resource conservation. Although there have been many results on ELO devices for GaAs lattice-matched systems,[16–19] few studies have been carried out for lattice-mismatched systems. The combination of ELO and metamorphic lattice-mismatched growth will open up many possibilities; it is acceptable to grow a considerably thick buffer on a conventional substrate, leading to a "virtual substrate" with a desired lattice constant and reduced defect density for the ELO device growth and the HI.

As an example of the proposal, we investigated the ELO of $In_{0.57}Ga_{0.43}As/In_{0.56}Al_{0.44}As$ metamorphic high electron mobility heterostructures on GaAs and their VWB on AlN ceramic

substrates. By means of molecular beam epitaxy, we have grown a metamorphic buffer consisting of an $In_xGa_{1-x}As$ step graded buffer (SGB) and an $In_{0.56}Al_{0.44}As$ buffer. The InGaAs SGB has $x = 0.19 \rightarrow 0.62$ with $\Delta x = 0.054$ and 100 nm each step thickness, and the InAlAs buffer is 100 nm thick. After the growth of the metamorphic buffer, a very thin AlAs sacrificial layer of 3 nm thickness was grown. Finally, we have grown a modulation-doped InGaAs/InAlAs metamorphic device layer consisting of an $In_{0.56}Al_{0.44}As$ barrier (1.9 μm), an $In_{0.57}Ga_{0.43}As$ channel (30 nm), an $In_{0.56}Al_{0.44}As$ spacer (20 nm), a Si δ-doping, an $In_{0.56}Al_{0.44}As$ barrier (40 nm), and an $In_{0.57}Ga_{0.43}As$ cap (10 nm). The indium contents were precisely confirmed by symmetric and asymmetric X-ray diffraction measurements. We have employed slightly higher indium contents than the InP lattice-matched system, according to the freedom of choice regarding the indium contents. The InGaAs SGBs are usually not preferred for metamorphic devices because of their parallel conduction or leakage currents, as well as parasitic capacitances. However, we employed the InGaAs SGB, because there is no need to concern its influence on device operation after the ELO. Moreover, it is advantageous for selective etching of the AlAs sacrificial layer, in comparison with the InAlAs SGB, whose low indium content regions are etched during the sacrificial layer etching. In the device layer, the channel and the barrier are almost lattice-matched to each other. On the other hand, there is a 4 % lattice-mismatch between the device layer and the sacrificial layer, and also between the top of the metamorphic buffer layer and the sacrificial layer. Figure 1 shows a cross-sectional transmission electron microscope image of the grown structure. There is a tendency for dislocations to be confined to the bottom region, which can be attributed to the alloy hardening gradient.[20] In spite of the 4 % lattice-mismatch, the influence of the thin AlAs sacrificial layer on the device layer is not serious. It should be noted that, concerning the AlAs sacrificial layer thickness, there is a trade-off between the device layer crystal quality and the ELO process easiness; thicker sacrificial layers lead to easier and fast ELO processes, but lower crystal qualities. Thus, we fixed the AlAs sacrificial thickness at 3 nm, which results in a defect density on the order of 10^8 cm^{-2}, similar to usual metamorphic devices.[6,7]

Using the metamorphic heterostructure, we have fabricated thin film Hall-bar devices on AlN ceramic substrates by using ELO and VWB. The AlN has favorable properties for device applications: a high thermal conductivity suitable for efficient heat management, a high electrical resistivity for low leakage currents, and a lower dielectric constant for lower parasitic capacitances. Figure 2(a) shows a schematic fabrication process. After device mesa-etching, the thin film device layer is separated by ELO etching, selective etching of the AlAs sacrificial layer using the 12.5 % HF solution. The separated device layer is then bonded onto the AlN ceramic substrates by a VW force, followed by the conventional photolithography and lift-off process of Ti/AuGeNi/Au ohmic electrodes. Since the separated thin film device layers are very fragile, we must take care in the handling and bonding processes to avoid a damage.

One of the successful procedures is as follows. The sacrificial layer etching in the HF solution is carried out using the resist on the device layers for the device mesa-etching. The resist improves the yield of the ELO process, supporting the device layers and suppressing their deformation and damage. For example, we employed the resist of ~ 0.2 μm-thick LOL-2000 consisting of polydimethylglutarimide and ~ 2 μm-thick OMR-85 consisting of rubber and bisazide on it; the purpose of the former is the enhancement of adherence between the resist and the device layers. During the sacrificial layer etching, there was a weak [110] direction roll-up tendency of the device layers, which direction is different from [100] for pseudomorphic strained systems.[21] This can be attributed to a weak strain caused by small lattice-mismatch between the channel and the barrier. After the sacrificial layer etching, the device layer with the substrate is moved from the HF solution into deionized water, in which the device layer with the resist is transferred onto the AlN substrate. After drying, the resist is removed from the device layer on the AlN by O_2 plasma ashing. By dropping a small amount of water near the interface between the device layer and the AlN, and subsequent drying, we can obtain a sufficiently firm VWB for the following electrode formation process. The AlN ceramic substrate has the root mean square surface roughness $\gtrsim$15 nm, which is rather rough and disadvantageous for the VWB. In order to obtain firmer bonding, hydrophilic surface pre-treatments using O_2 plasma were effective. Figure 2(b) shows a picture of a separated device layer in deionized water during the process (left), and an optical microscope image of a successfully fabricated Hall-bar device bonded on the AlN ceramic substrate, whose current flowing direction is [100] (right). The outer size of the device is about 900×1400 μm^2. The channel width is 50 μm, and the maximum mesa width of the device including contact regions is 400 μm. For this device size, the needed sacrificial layer etching time was 20-30 min. On the other hand, for the ELO of larger samples, it is effective to use a supporting wax on the surface. Larger area samples up to 3×3 mm^2 were successfully epitaxial-lifted off with the wax on the surface, whose needed sacrificial layer etching time was several hours, and bonded on an AlN substrate, followed by a wax removal. The larger samples can be used for various characterizations, such as X-ray diffraction and photoluminescence measurements. Detailed characterization results will be discussed elsewhere.

Hall measurements were carried out for the ELO Hall-bar device. Figure 3 shows temperature dependence of electron mobility and sheet electron concentration, with results for the on-wafer counterpart before ELO. We obtain very high electron mobilities for the ELO device, such as 11000 cm^2/V-s at room temperature (RT) and 84000 cm^2/V-s at 12 K. The measurements were stable and reproducible. The obtained RT mobility is the highest ever reported for ELO devices,[16–18] owing to the high indium content and the successful ELO and VWB processes. Moreover, the mobility is higher than that obtained by the transferred-substrate using the substrate etching-out technique for an InP lattice-matched system.[15] We confirmed

that, with high reproducibility, these high electron mobilities are obtained for many devices and all the current flowing crystalline directions. The mobility behavior of the ELO Hall-bar device is almost the same as that of the on-wafer counterpart. Since the ohmic contacts of the on-wafer counterpart are non-alloyed and shallow, influences of the parallel conduction of the metamorphic buffer are not so prominent. However, in the high temperature region, we find differences in the sheet electron concentration; the on-wafer counterpart exhibits higher values than the ELO device, due to the parallel conduction of the metamorphic buffer, which also causes a parasitic capacitance. The ELO device is completely free from these problems. This is a proof of that the restriction in the metamorphic buffer material choice can be removed.

In summary, based on the proposal of the application of ELO to metamorphic lattice-mismatched growth, we have successfully carried out ELO of $In_{0.57}Ga_{0.43}As/In_{0.56}Al_{0.44}As$ metamorphic heterostructures and their VWB on AlN ceramic substrates. The obtained devices show very high electron mobilities, owing to the high indium content and the successful ELO and VWB processes. We consider that this technology will be useful for many future applications including the HI on arbitrary host substrates, such as silicon, ceramic, glass, and plastic.

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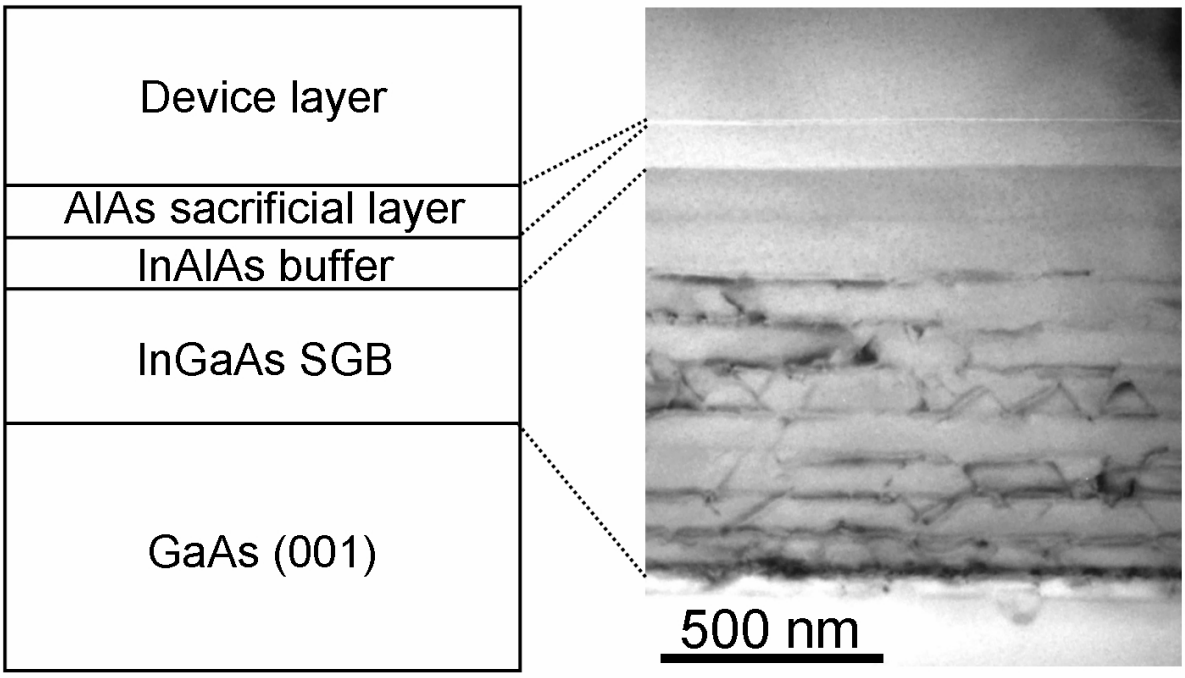
Figure captions

Figure 1:
A cross-sectional transmission electron microscope image of the InGaAs/InAlAs metamorphic heterostructure.

Figure 2:
(a) A schematic of the device fabrication process. (b) A separated device layer in deionized water during the process (left) and a successfully fabricated Hall-bar device on an AlN ceramic substrate (right).

Figure 3:
Temperature dependence of electron mobility and sheet electron concentration of the ELO and the on-wafer Hall-bar devices.



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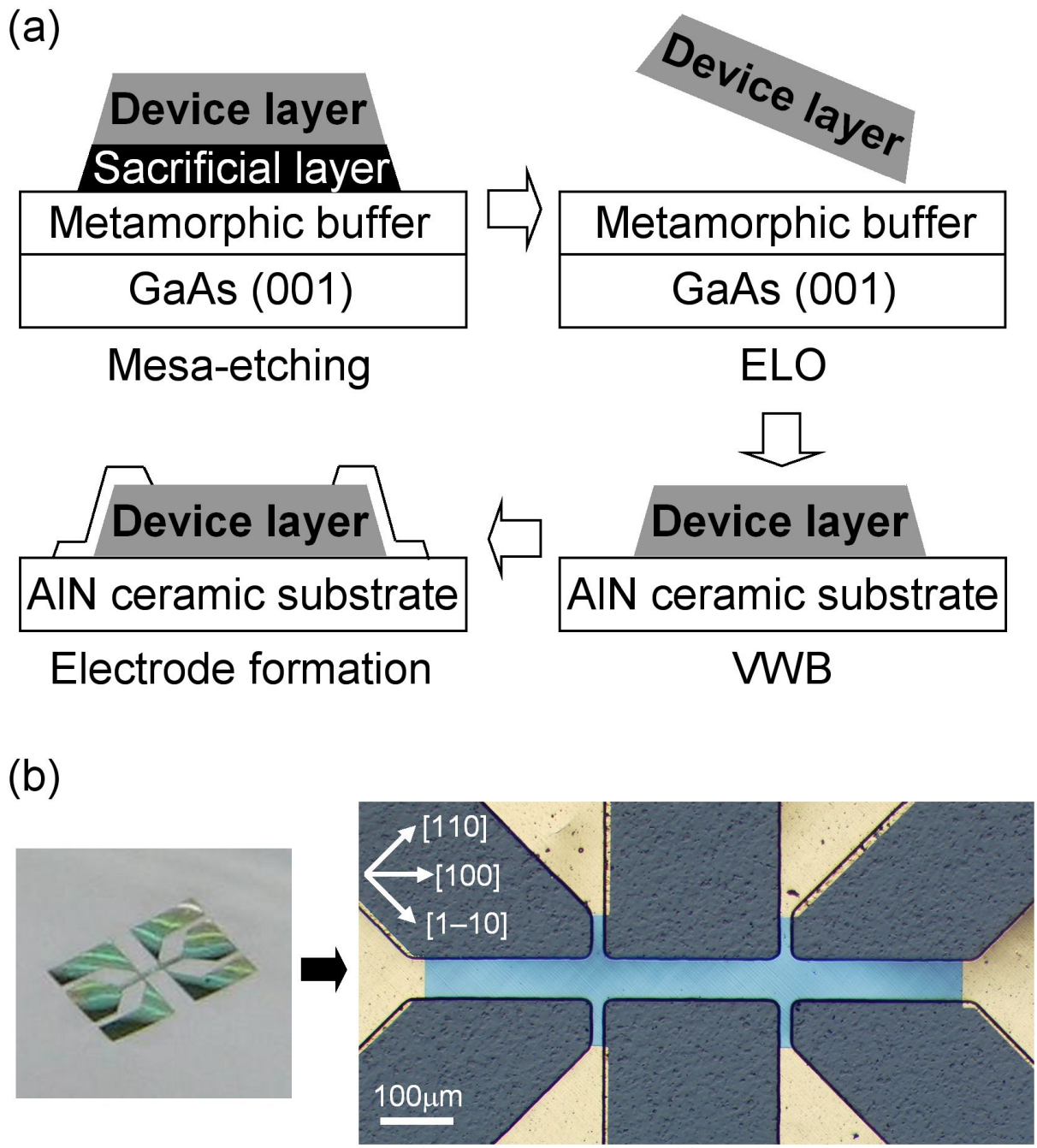

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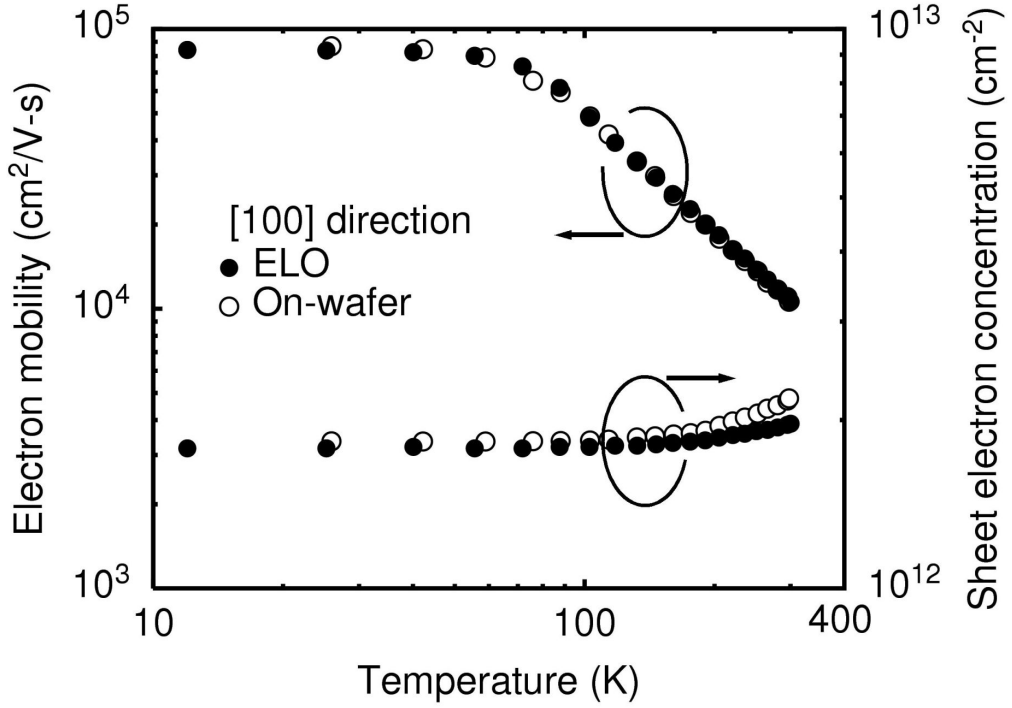

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