A 1K-Gate GaAs Gate Array

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Abstract — **1050-gate arrays have been successfully designed and fabricated. Chip size is 3.75×3.75 mm. A basic cell can be programmed as an E/D-type DCFL three-input NOR gate. Speed performance measured at 0.2 mW/gate power dissipation was as follows. Unloaded (fanout = 1) propagation delay time was 100 ps/gate. Load dependence of the delay time was 65 ps/1 mm interconnection line, 27 ps/fanout, and 3.33 ps/crossover load. This leads to 350 ps/gate delay under the assumed loading condition of interconnection line length = 3 mm and three fanouts.**

The gate array was applied to a 6×6 bit parallel multiplier circuit. The 10.6 ns multiplication time was measured at 380 mW power consumption. The operation speed of the personalized circuit can be well described by the basic performance provided by ring oscillator measurement.

I. INTRODUCTION

TEN years have passed since the first GaAs digital IC was reported in this journal [1]. Great progress has been made in GaAs material and process technology, especially for the past several years, which has brought state-of-the-art GaAs IC's into LSI level integration [2]–[5].

From the system viewpoint, more and more logics are desired to be integrated in a single chip to make the best of GaAs high-speed capability. The reason is that the multi-SSI/MSI chip system has to include millimeter/centimeter-range interconnections between chips, where even an electromagnetic wave requires 10–100 ps to travel, while the propagation delay inside the GaAs IC chip is almost in the same time range. Among the several circuits available to GaAs, which include BFL, SDFL, DCFL, and SCFL, DCFL (direct-coupled FET logic) is the simplest and shows the least power consumption. It seems that only DCFL can realize more than several thousand gate logics in a chip, taking into account the power limit in a single chip.

The gate array approach is also effective for GaAs as well as for Si IC's in enabling logic designers to obtain desired logic functions relatively easily. To date, GaAs gate arrays with hundreds of gates in a chip have been reported [6]–[9].

This paper reports on the successful fabrication of a 1K-gate GaAs gate array using DCFL circuitry, emphasizing that the GaAs DCFL has the potential of obtaining high speed and higher integration than any other circuitry. Application to a 6×6 bit parallel multiplier and its complete operation will also be described.

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II. DESIGN

A. FET Size Determination

The gate array performance largely depends on the FET size for each gate. Prior to the final design, three kinds of gate array basic cells were fabricated and evaluated. Basic cells were implemented by *E/D*-type DCFL to make three-input NOR programmable. The three kinds include EFET/DFET gate widths of 10/5 (type A), 20/10 (type B), and 40/20 (type C) in microns, respectively. Loaded propagation delay time versus power dissipation characteristics were measured, taking basic cell FET size as a parameter. Empirical loaded propagation delay time t_{pd} is given by

$$t_{pd} = t_{pd1} + (F-1)\cdot\Delta t_{pdF} + L\cdot\Delta t_{pdL} + C\cdot\Delta t_{pdC}$$

where

t_{pd1} = unloaded (fanout = 1) propagation delay time

Δt_{pdF} = increase in delay time/fanout

Δt_{pdL} = increase in delay time/unit interconnection length

Δt_{pdC} = increase in delay time/one crossover load

F = number of fanouts

L = interconnection line length

C = number of crossovers as a load.

Δt_{pdF}, Δt_{pdL}, and Δt_{pdC} as functions of power dissipation and basic cell FET size are shown in Figs. 1, 2, and 3, respectively. These data have been obtained by measuring the waveforms of 15-stage ring oscillators with various kinds of loads listed in Table I. Fig. 4 shows the gate array chip, where seven different ring oscillators are constructed using 20/10 μm EFET/DFET gate width (type B). Gate arrays for the other two types of basic cells (types A and C) were also fabricated on the same wafer. Thus, process conditions are completely the same through types A, B, and C. The design rules for these three types of ring oscillators are also identical, except for gate width. Therefore, the measured characteristics can be directly compared with each other. Comparison results indicate gate width tradeoffs for basic cell FET's.

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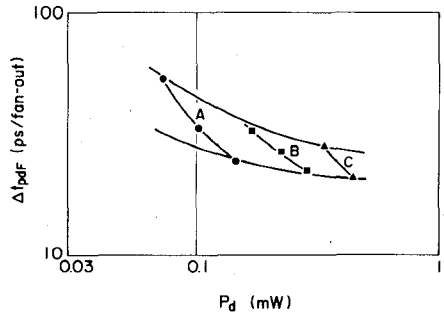


Fig. 1. Propagation delay time increase per fanout as functions of power dissipation and basic cell FET size. $V_{DD}=1$ V.

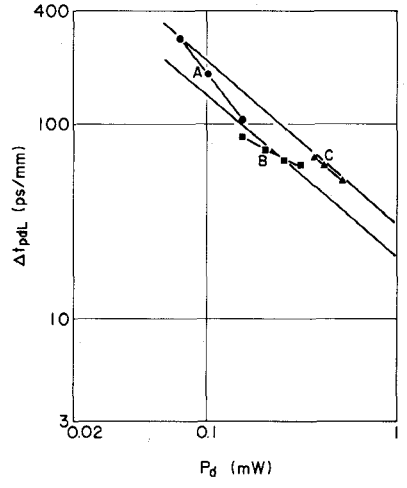


Fig. 2. Propagation delay time increase per 1 mm interconnection line load as functions of power dissipation and basic cell FET size. $V_{DD}=1$ V.

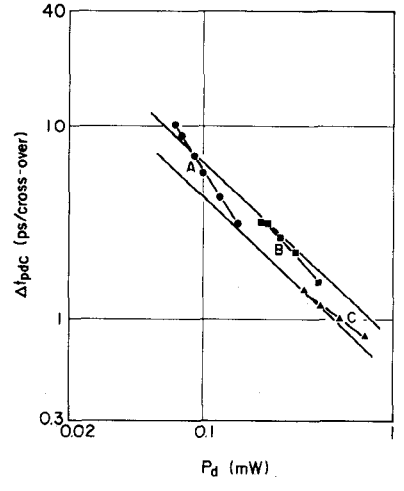


Fig. 3. Propagation delay time increase per one crossover load as functions of power dissipation and basic cell FET size. $V_{DD}=1$ V.

Figs. 2 and 3 show that the switching energy for an additional load is constant, regardless of the basic cell FET size. This is supported by the following simple analysis.

Given load capacitance C_L, electric charge Q is expressed as

$$Q = C_L \cdot \Delta V \propto i_c t_{pd} \tag{1}$$

where ΔV is the E/D DCFL logic swing, i_c is the charging current, and t_{pd} is the propagation delay time. i_c is determined by the saturation current for load DFET. Power dissipation P_d is proportional to $i_c V_{DD}$, where V_{DD} is the supply voltage. Thus,

$$P_d \propto i_c V_{DD}. \tag{2}$$

Equations (1) and (2) yield

$$W = P_d t_{pd} \propto C_L \cdot \Delta V \cdot V_{DD}. \tag{3}$$

It can be concluded that $P_d t_{pd}$ is constant with a fixed load capacitance, even if FET size is changed.

For fanout dependence, simple analysis by (1) gives

$$t_{pd} \propto C_L \cdot \Delta V / i_c.$$

Both C_L and i_c are proportional to FET gate width.

TABLE I
RING OSCILLATORS WITH VARIOUS KINDS OF LOADS

15-stage ring oscillators
Loading condition
F.O. = 1
F.O. = 3
F.O. = 5
L = 1 mm
L = 2 mm
L = 3 mm
Number of cross-over = 64

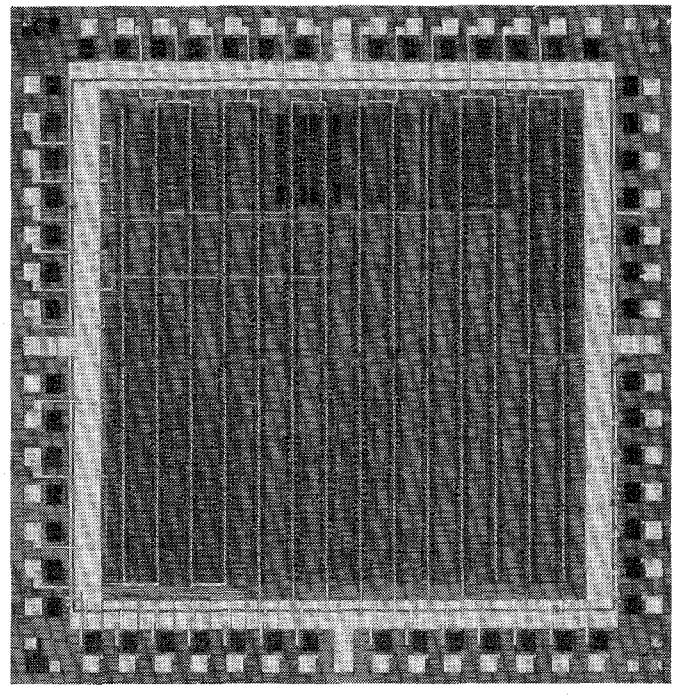


Fig. 4. Gate array performance evaluation chip. 15-stage ring oscillators using 20/10 μm wide EFET/DFET DCFL basic cells with various kinds of loads are constructed. The chip configuration is the same as the final version of the 1K-gate gate array.

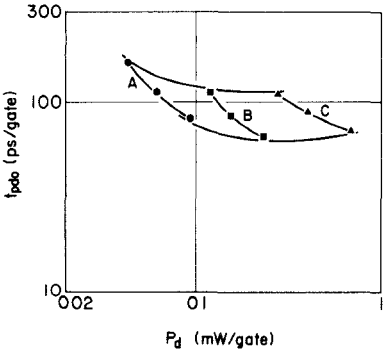


Fig. 5. Propagation delay time versus power dissipation for compact ring oscillators as a function of basic cell FET size

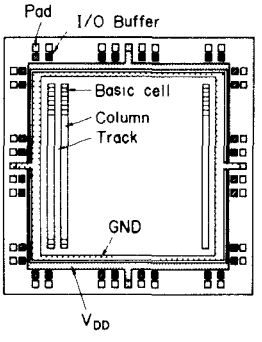


Fig. 6 Chip design representation for the final version of 1K-gate gate array.

Therefore, Δt_{pdF} ideally does not depend on FET size. The same conclusion can be applied to intrinsic propagation delay time t_{pd0}, measured on the compact ring oscillators, where interconnection line length between inverters is laid out to be minimized (Fig. 5). Both Δt_{pdF} and t_{pd0} have a little bit larger value for type A than for the other two types. This implies that parasitic capacitance exists, which cannot be counted as either interconnection line or crossover load. This parasitic capacitance might be associated with the FET electrode layout. However, details are not known.

These measured data served as support materials for making the decision in regard to FET size. The decision was also made, taking into account the required gate array specifications on speed, power, and chip size.

Type B was adopted as the final design for 1K-gate gate array, because of its Δt_{pdF} advantage over type A and smaller power consumption than type C, with almost the same Δt_{pdF} value. The 0.2 mW/gate power dissipation for type B is also favorable, when targeting future several-thousand-gate gate arrays, which makes the 1K-gate gate array a good experimental step towards higher integration.

B. Chip Layout

Fig. 6 shows the schematic representation of the final version of the 1K-gate GaAs gate array. It is identical with the chip shown in Fig. 4 and also with the application chip described later.

Chip size is 3.75×3.75 mm. Fig. 7 shows the layout and the equivalent circuit representation for the basic cell,

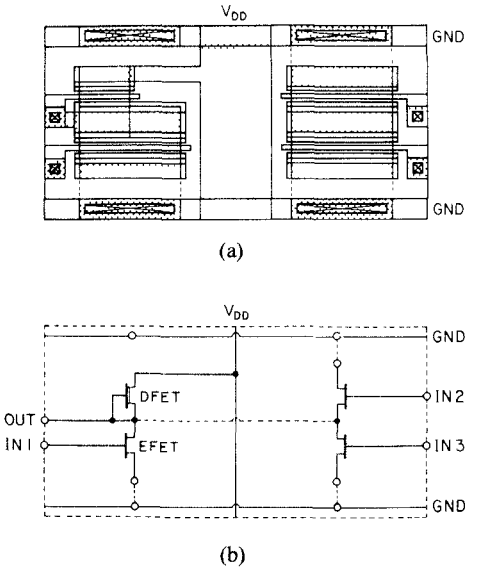


Fig. 7. Basic cell used in the chip shown in Fig. 6. (a) Layout (b) Equivalent circuit representation. EFET/DFET gate width is 20/10 μm.

which measures 34×75 μm and can be programmed as a DCFL three-input NOR gate. The nominal gate width/length values are 10/1 (μm) for DFET load and 20/1 for EFET drivers. Source and drain contacts are formed onto the heavily doped n-type region and nominal n^+-n^+ spacing is 2 μm. There are 14 columns and each column has 75 basic cells, totalling 1050 gates in a chip. Between the columns, there are 13 interconnection tracks whose width is 108 μm. The design rules of 2 μm line width, 3 μm line spacing, and 2×2 μm contact hole allow 13 first-level interconnection lines to run in each track parallel to the column direction. The second-level interconnection lines (3 μm wide and 4 μm spacing) can run across the column with the restriction that they should not run above the FET gate region. Actually, three second-level line can run across the basic cell, which is not used as a gate, or one second-level line can run across the basic cell in use.

In order to avoid the low noise margin problems associated with DCFL circuitry, various measures were employed for the power supply line layout, especially for the ground lines. Among them was the layout wherein ground lines were realized by second-level metallization to minimize sheet resistance. In addition, a ground line which is connected to each basic cell runs vertically to the column direction, which reduces the number of basic cells connected to each ground line, resulting in low current and low voltage drop in each ground line. In the design phase, power supply lines are laid out so that the potential difference between ground level for any basic cell and ground pad should be less than 50 mV and the voltage drop at any point in the V_{DD} lines should be less than 200 mV.

Surrounding the array region are the V_{DD} and ground (GND) main lines, and 56 I/O buffers and pads. Two V_{DD} and two GND pads are also provided.

The circuit used for an I/O buffer is shown in Fig. 8. It consists of 2 DFET's and 8 EFET's. All FET's have 80 μm

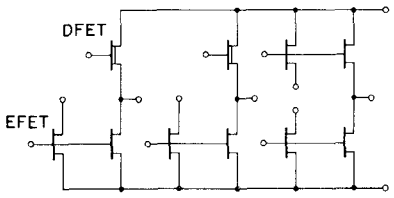


Fig. 8. I/O buffer cell circuitry.

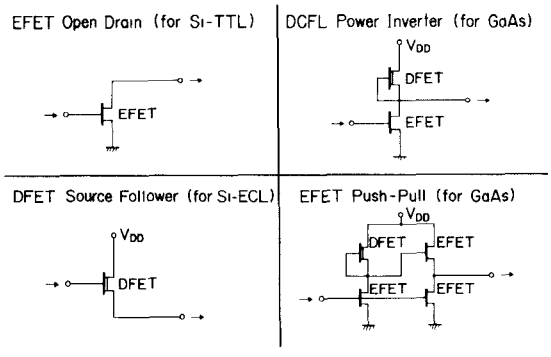


Fig. 9. Examples of output buffer circuit programming.

gate width. They can be programmed as either an input or output buffer.

It is well known that there is an orientation effect on GaAs MESFET I-V characteristics [10]. In order not to be affected by this effect, all the FET's are placed parallel to each other in terms of gate width direction, including I/O buffers and basic cells. Therefore, the I/O buffer cell is designed to be square-like in shape to aid in achieving a space-efficient layout. As a result, the I/O buffer cell occupies an about 110×120 μm area adjacent to a pad.

Input buffers are DCFL power inverters. As shown in Fig. 9, available output buffers include EFET open drain circuits for Si–TTL interfaces, DFET source followers for Si–ECL interfaces, DCFL power inverters, and EFET push-pull circuits for interfacing with GaAs circuits of the same type. A specific buffer can be selected by the interconnection layout masks for each interfacing purpose.

III. Fabrication Process

Table II summarizes the fabrication process used for 1K-gate gate array. The key feature is the Pt-buried gate technique, which uses the Pt reaction with GaAs at around 400°C to control FET threshold voltage [11]. Average threshold voltage was 0.1 V for EFET and -0.7 V for DFET. Standard deviation in the threshold voltage was 53 mV for EFET's and 110 mV for DFET's across a wafer.

Thickness and sheet resistivity values were 6000 Å and 0.1 $\Omega/\square$ for first-level metallization and 1.2 μm and 0.02 $\Omega/\square$ for second-level metallization.

Lithography used through all processes was optical with contact/proximity exposure.

IV. Gate Array Performance

Examples of EFET and DFET *I-V* characteristics used in basic cells are shown in Fig. 10. As described in Section II, propagation delay time dependence on the interconnection line length and the number of fanouts and crossovers was evaluated by measuring ring oscillators under various loads at $V_{DD} = 1$ V. The obtained results are as follows. The unloaded propagation delay time was 100 ps/gate and the delay time increased at a rate of 65 ps/mm, 27 ps/fanout and 3.33 ps/crossover at power dissipation of 0.2 mW/gate, where nominal crossover area was 2×3 μm. This leads to $t_{pd} = 350$ ps/gate under an assumed loading condition of interconnection line length = 3 mm and three fanouts.

SPICE-II simulation was performed to understand ring oscillator operation. The SPICE-II JFET model was applied. Using EFET and DFET *I-V* characteristics shown in Fig. 10 and assuming 0.9 fF/μm^2 nonbiased gate junction capacitance, the simulated unloaded delay time coincided very well with the measured value. The simulation also

TABLE II
Fabrication Process for 1K-Gate GaAs Gate Array

• Substrate	Cr-doped 2"ϕ LEC wafer
• Active layer formation	$^{28}Si^{+}$ selective implantation directly into the substrate
n^{+}-Source & Drain	200 keV 30×10^{13} cm^{-2}
DFET	150 keV 2.8×10^{12} cm^{-2}
EFET	100 keV 3.2×10^{12} cm^{-2}
• Annealing	Capless 850°C 15 min AsH_3 + Ar
• Ohmic contact	AuGe/Au 420°C 2min alloy
• Gate metal	Pt(50nm) 400°C sintering
• 1st metal	Ti/Pt/Au
• Spacing dielectric	CVD SiO_2 (600 nm)
• Contact hole	Au via metal
• 2nd metal	Ti/Pt/Au

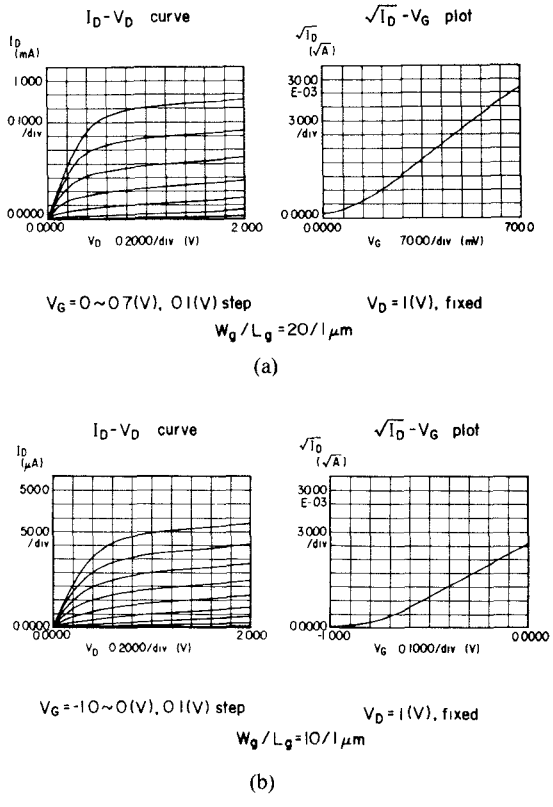


Fig. 10. Examples of EFET(a) and DFET(b) *I-V* characteristics used in a basic cell.

TABLE III
PERFORMANCE OF 1K-GATE GaAs GATE ARRAY

Chip size	3.75 mm × 3.75 mm
Basic cell	3-INPUT NOR (DCFL)
FET size (mask)	10/1 (μm) DFET load 20/1 (μm) EFET driver
FET source-drain spacing	2 μm (n^+-source, drain)
Design rule for interconnection	
1st level	2-μm wide, 3-μm spacing
2nd level	3-μm wide, 4-μm spacing
contact hole	2 μm × 2 μm
FET performance measured	
g_m	110 mS/mm
V_{th}	0.1 V(EFET), -0.7 V(DFET)
L_g (gate length)	1.0 μm
Propagation delay time	
unloaded (fan-out=1)	100 ps/gate
power level	0.2 mW/gate
dependence on load	27 ps/fan-out 65 ps/mm 3.33 ps/cross-over
Propagation delay time under loading condition of L=3 mm, Fan-out=3	350 ps/gate (0.2 mW/gate)

showed that additional fixed 1 fF capacitive load increases delay time by 1.09 ps. This value was combined with the measured t_{pd} dependence on interconnection line length (= 65 ps/mm), and it was found that first-level interconnection line capacitance was 60 fF/mm, which agrees very well with the numerically calculated value reported elsewhere [12].

The gate array performance is summarized in Table III.

V. APPLICATION

The gate array has been applied to a 6×6 bit parallel multiplier circuit. Fig. 11 shows the applied gate array chip. 378 internal gates and 24 I/O buffer cells are used to implement the circuit employing a carry-save algorithm, which is illustrated in Fig. 12. The critical path is shown by the thick arrow in the figure. A full adder (FA) and half adder (HA) are constructed using NOR gates and inverters, as shown in Fig. 13.

Approximately 70 percent of the array area is occupied for interconnection purposes. Layout is not compact and is not optimized. However, this layout appeared to be good enough to demonstrate the feasibility of using the GaAs gate array at 1K-gate level integration. Output buffers selected were 160 μm wide EFET push-pull circuits.

A functional test was performed at $V_{DD}=1.5$ V. An example of low frequency test results with high load impedance at the output buffer is shown in Fig. 14. The input data pattern was $10000S \times 111111$. A sequential 0/1 pulse was applied to the least significant input bit $A0$. This test is the so-called ripple test. Complete operation was confirmed, as shown in the figure. Logic swings at all outputs are large enough to drive DCFL inputs of other GaAs IC's.

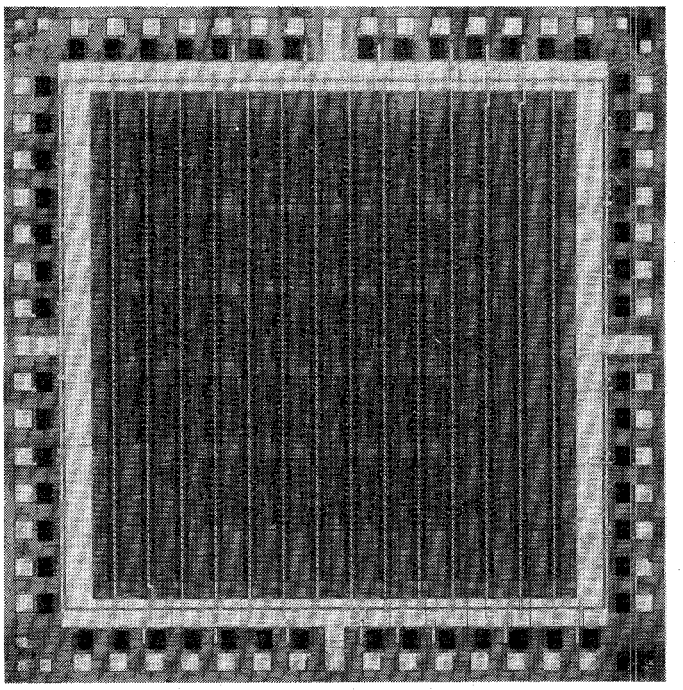


Fig. 11. Gate array chip applied to 6×6 bit parallel multiplier.

Multiplication time measurement was also performed for the chip which passed the low frequency test. The test pattern for multiplication time measurement was $S00001 \times 111111$. S went from the 0 to the 1 state and was applied to the most significant input bit $A5$. Fig. 15 shows the waveforms of product bits $P10$ and $P11$ measured by wafer probing. The probe system was a 50 Ω system, calibrated for high-speed testing. The rise time of the applied input was about 2 ns, which was determined by the pulse generator performance used and the bandwidth of the wafer probing system. Multiplication time is the time between the input rise and the $P10$ output fall. It is not clear at which moment the input rise signal transient makes the input buffer invert the signal. It is also not clear which moment of the down slope for the $P10$ output waveform reveals the multiplication completion point. In spite of these uncertain factors, it can be said that the multiplication time is less than 10.6 ns, where total power consumption is 380 mW, including I/O buffer circuit operation.

On the other hand, multiplication time was calculated using the gate array performance data listed in Table III. The loading conditions at a specific logic gate along the critical path were evaluated by looking at the actual layout to calculate propagation delay time at the gate. Multiplication time was calculated as the sum of the propagation delay times at each gate along the critical path. The calculated multiplication time was 8.5 ns. This agrees fairly well with 9 ns, which is the measured value obtained by taking the time between the middle of the input rise and the moment when the output just begins to fall as the multiplication time.

Therefore, the speed performance of the personalized gate array can be reasonably explained and estimated, using the basic performance obtained through ring oscillator results.

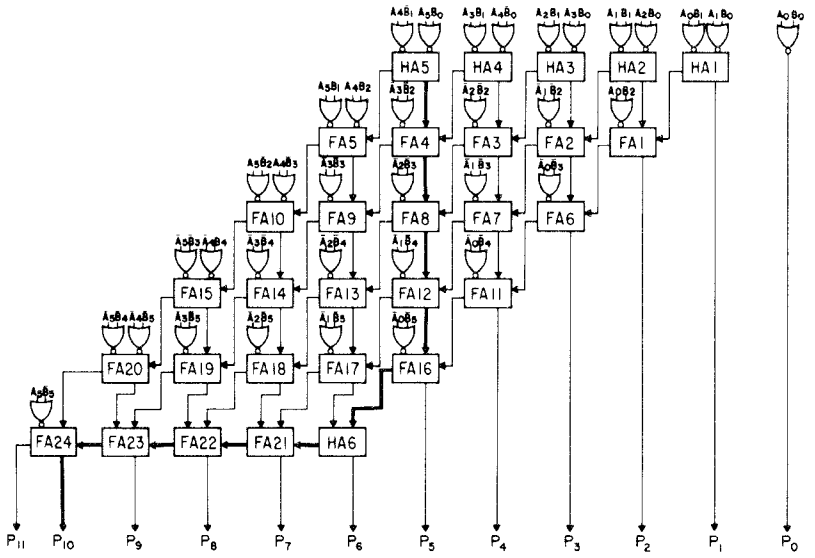


Fig. 12. Block diagram for 6×6 bit parallel multiplier. Carry-save algorithm is used. Thick arrow shows the critical path.

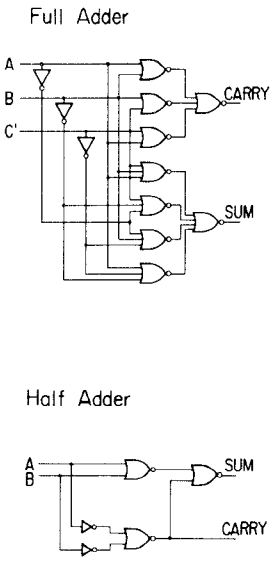
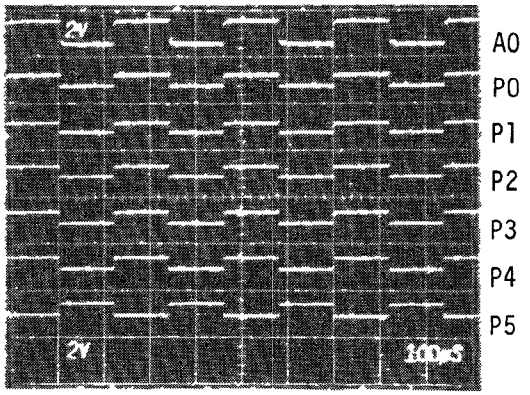


Fig 13. Block diagram for full adder (FA) and half adder (HA) used in 6×6 bit parallel multiplier.



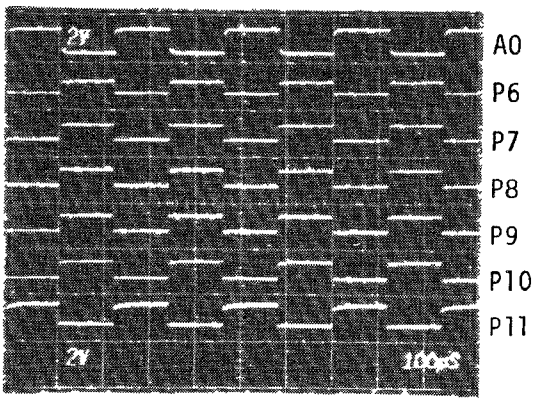


Fig 14 Outputs of 6×6 bit parallel multiplier at low frequency test. Input code is $10000S \times 111111 = S\bar{S}S\bar{S}S\bar{S}S\bar{S}S\bar{S}S\bar{S}$, where S is sequential 0/1 pulse applied to $A0$. $V_{DD} = 1.5$ V, $P = 380$ mW

The logic swing obtained in high-speed testing is 230 mV, as shown in Fig. 15. Thus, the current driven by a 160 μm wide EFET push-pull output buffer is estimated to be 230 (mV)/50 (Ω) = 4.6 mA. This indicates that the output buffer speed is 2.2 ns when driving the assumed 10 pF external capacitive load to obtain 1 V logic swing. It might also be the case with other types of output buffers like the 160 μm wide EFET open drain and the 160 μm wide DFET source follower, which is implied by the I-V curves for 20 μm wide EFET and 10 μm wide DFET, as shown in Fig. 10. However, they have not been directly measured yet.

VI. Conclusion

A 1050-gate GaAs gate array has been successfully fabricated using DCFL circuitry. It features 350 ps/gate propagation delay at 0.2 mW/gate power dissipation under the loading condition of 3 mm interconnection line length and three fanouts. A 6×6 bit parallel multiplier was constructed on the gate array. The multiplication time was measured to be 10.6 ns at 380 mW overall power consumption.

Gate array performance is compared with other logic families on the basis of speed, power and integration, as

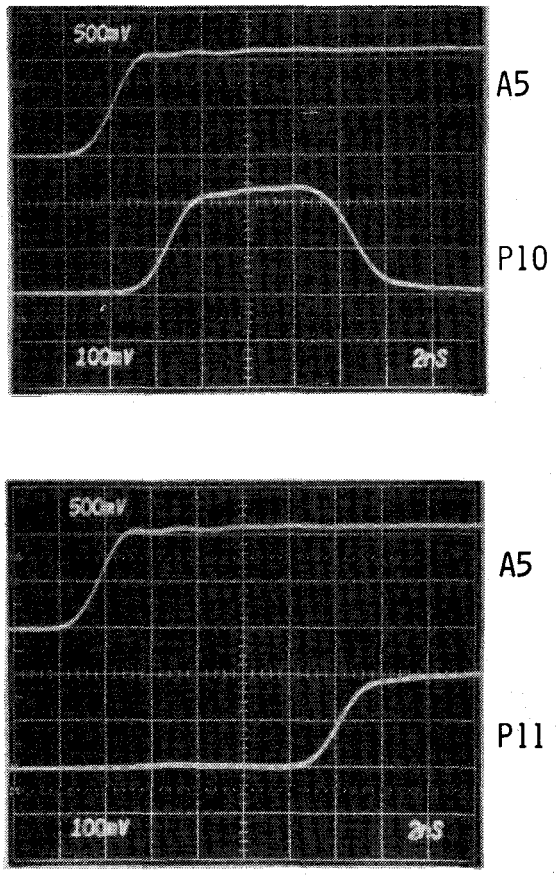


Fig. 15. Output waveforms for product bits $P10$ and $P11$, when $S00001 \times 111111 = S00000S11111$ multiplication was performed. S is the pulse applied to $A5$, which changes from 0 to 1 state. At first, output $P10$ rises, responding to fast arrival of $A5B5(=1)$ calculation at $FA24$. It then returns to zero as a result of carry signal from $FA23$ to $FA24$. This corresponds to the critical path of the multiplier. $V_{DD} = 1.5$ V, $P = 380$ mW.

shown in Fig. 16. As is clearly seen in the figure, the speed for the GaAs gate array is almost the same as that for the Si-ECL. However, the power consumption is much less than for the ECL, that is about 1/10 that for the ECL. Comparing with CMOS, GaAs is much faster. Thus, it can be said that the GaAs gate array has now entered the LSI integration level with both high-speed and low-power performance and seems to fit into the new performance area. This performance indicates that a high-speed GaAs gate array with several thousand gates will be obtainable without introducing a special cooling technique for a chip. Also shown by the dotted bar in the figure is the performance for the projected future GaAs gate array. It would be featured by less than 200 ps/gate delay, less than 0.2 mW/gate power dissipation, and more than 5K gates/chip integration.

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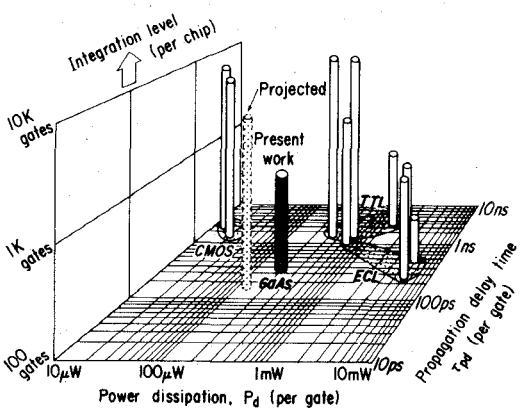

Fig. 16. Performance comparison between gate array families under loading condition on the basis of speed, power, and integration. Present work (GaAs), Si-bipolar, and Si-CMOS are compared. Projected future GaAs gate array is also shown by the dotted bar.

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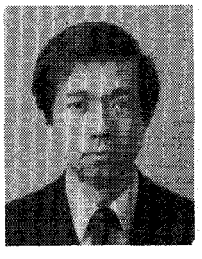

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A Gallium Arsenide Configurable Cell Array Using Buffered FET Logic

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Abstract—**A GaAs configurable cell array has been fabricated using 1 μm gate MESFET's on 3 in GaAs substrates using a planar fabrication technique. Depletion-mode MESFET's configured in BFL structures were used to implement the logic cells. The cells are programmable for several logic functions and two different drive capabilities. Placement and routing software was developed. Cell configuration and array organization were adjusted to optimize the efficiency of the placing and routing software. Measured results on several cell configurations with various device sizes yielded speed-power products ranging from 162 to 460 fJ. A 306 cell array (equivalent to approximately 430 NOR gates) occupying a chip area of 2.0×2.8 mm was fabricated. A 5×5 bit parallel multiplier implemented with this array showed a multiplication time of 6.5 ns, and a power dissipation ranging from 337 to 722 mW corresponding to a cell power of 1.30–2.79 mW/cell.**

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I. INTRODUCTION

GATE arrays offer a viable method for implementing high speed circuits requiring rapid design and fabrication times and low design costs. With the complexity of GaAs circuits surpassing the 3000 gate level of integration [1], gate array development has become feasible. GaAs gate arrays have been demonstrated using both MESFET's and heterostructure bipolar devices [2]–[6]. Each of these approaches have associated advantages with respect to speed, power, noise margins, and process sensitivity.

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