Title	LSI
Author(s)	,
Citation	
Issue Date	2009-03
Type	Thesis or Dissertation
Text version	author
URL	http://hdl.handle.net/10119/8128
Rights	
Description	Supervisor: , ,

A Tunable LSI Based on Timing Skew and Stall Adjustments

Yayumi Uehara (0710013)

School of Information Science,
Japan Advanced Institute of Science and Technology

February 5, 2009

Keywords: skew, stall, tunable LSI, mixed integer linear programming.

The advance of semiconductor process technologies makes it possible to manufacture highly integrated circuits. However, for such highly miniaturized integrated circuits, the variation of characteristics of transistors and wires is becoming relatively larger than ever, and hence the intra- and inter-chip variations of signal propagation delay are becoming relatively larger and larger.

The behavior of a sequential circuit and a datapath circuit can be seen as the signal propagation between registers through combinational circuits. There fore the timing of the latch of the signal is an important factor to define the behavior of the circuit. To design a robust circuit over signal propagation delay variations, overestimated timing margins are required. However, it is an impediment to designing a high performance circuit.

To cope with such a situation, statistical static timing analysis (SSTA) method has been proposed. In such a method, signal propagation delay is estimated statistically, and the designer has to decide a design point considering trade-off between performance and yield. Although a statistical method provides higher performance than conventional worst-case design, most of the manufactured chips have a potential to operate with higher performance than the design point even if the statistical method is applied because it does not reduce delay variations.

In this research, we mainly focus on the datapath part of LSIs. We use the following two techniques which adjust the write timing at each register without changing the clock frequency: (1) timing skew adjustment to each register (2) stall adjustment to each control step. If we apply only the skew adjustment, the datapath does not always have a feasible skew assignment for given delay variations. On the other hand, if we apply only the stall adjustment, it causes the increase in the total number of the execution steps more than necessary. Therefore the purpose of this research is to propose the circuit methodology with timing skew and stall adjustments. At the first step to achieve the purpose, we tackled the problem to minimize the increase in the total number of the execution steps. Since this increase is equal to the total number of inserted stalls, we can formulate this problem as the stall minimization problem. Although the computational complexity of this problem has been undissolved in a general case, we proved that the problem is in the class P if the maximum number of stalls is a constant. As an exact solution technique to the problem, we proposed MILP(mixed integer linear programming)-based method, and the MILP is solved by the commercial solver CPLEX. To evaluate the effectiveness of our method, we applied it to some small benchmark circuits. Signal propagation delays are varied with the normal distribution model. The experimental results show that CPLEX terminated in a reasonable time (a few seconds) for all the circuits we used. While we focus on the total number of the execution steps, the total execution time which is defined as the product of the value of the clock frequency and the total number of the execution steps, has been commonly used as one of the important criteria to evaluate the circuit performance. If we compare the total execution time obtained by our proposed method with (1) the method only allowing the clock period adjustment, and (2) the method only allowing the stall adjustment, the (1) takes the first place and our proposed method follows. The detailed examination of those experimental results suggests us the importance of the control schedule and resource sharing optimizations considering the opportunity of applying skew and stall adjustments.

To develop a datapath synthesis which is appropriate to our approach is one of our important future works. In addition, to develop the method for obtaining actual delays is an important problem. On the other hand, it

is interesting to examine an adjusting method that does not need actual delay values.