Abstract of the Dissertation

Computational Difficulty
Scheduling and Circuit Complexity

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The classification of problems according to their computational difficulty requires establishing both upper and lower bounds on the amount of computational resources necessary to solve them. In this thesis, we are investigating computational difficulty by studying the complexity of scheduling problems and boolean circuits. In particular, we are focusing on single machine scheduling problems with new types of due dates and release dates, and negation-limited circuits, where the number of negations available is restricted.

In 1986, Hall proposed a new type of due dates called generalized due dates. First, we investigate the problems of minimizing the maximum absolute lateness and range of lateness under generalized due dates. In contrast to the traditional due date cases, we show that these problems are NP-hard in the strong sense. Furthermore, we present simple approximation algorithms with non-trivial performance guarantee for these problems. Second, we are concerned with scheduling with both traditional and generalized due dates, and show that a polynomial time algorithm exists for the problem of minimizing the maximum of maximum latenesses induced by traditional and generalized due dates. In addition to scheduling involving generalized due dates, we also consider scheduling with a new type of release dates which are related to the traditional release dates in a similar way as the generalized due dates to the traditional ones. In 1992, Ishii, Tada, and Masuda proposed another new type of due dates called fuzzy due dates. We improve the algorithms for basic scheduling problems with fuzzy due dates.

The difficulty of a problem can be expressed as the number of gates in a circuit with the minimum number of gates, which computes the problem. We consider the complexity of negation-limited inverters, giving lower bounds as well as new upper bounds on the size and depth of the inverters. This suggests improved upper bounds for slice functions as well as a tighter relationship between negation-limited and general circuit complexity. We also show lower bounds for various symmetric functions. Finally, we establish relationships between the number of negations available and circuit sizes.

Key Words: computational complexity, single machine scheduling, due dates, release dates, circuit complexity, negation.