Performance improvement of Logical Circuits on the transistor applying decreasing electric field scaling

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1　Introduction

The advances in LSI circuits have mainly been due to the device scaling law (a law of physics) and the fine fabrication process technology. According to the device scaling law, the thickness of the gate oxide film becomes down to several crystal lattice spaces. In such cases, gate leakage current flows through the oxide insulating film due to the quantum tunneling effect. In order to solve this problem, high permittivity materials are used to maintain a constant electric field while keeping sufficient thickness of the insulating film. The scaling, however ,will reach the limit unless new high permittivity materials are discovered.

This paper proposes a decreasing electric field scaling in order to suppress the gate leakage current due to quantum tunneling effect. This scaling achieves larger integration density, lower power consumption and higher operating frequency of LSI circuits.

Evaluating results of the simulation on logic circuits applied with the proposed scaling method are shown.

2 A decreasing electric field scaling

On an ideal transistor, latency of a CMOS logic circuits depend purely on the capacity and the on-resistance of the gate, and are independent of the thickness of the Gate oxide. Therefore, it is possible to improve performance even when the thickness of the metal-oxide is fixed.

For these reasons we name and propose the method of scaling down the operating voltage, the length and the width of the gate while maintaining a fixed oxide thickness the 'decreasing electric field scaling'.

3 Solution to short channel effect

Short channel effect is a phenomenon that causes the threshold voltage to drop. When the proposed method is used, short channel effect occurs when the length of the gate is scaled down while the thickness of the gate oxide is fixed. When the threshold voltage decreases, the gate leakage current increases and results in increased static power usage. We need to raise the threshold voltage to solve this problem. On the other hand, threshold voltage cannot be independently determined by the gate leakage current. This is because problems such as decrease in supply voltage to observe the scaling or increase in gate on resistance when the gate on current is decreased, in other words increase in latency, exists.

To solve this problem, we control the threshold voltage by channel doping to the appropriate density to seek for a method that suppresses short channel effect and increases performance.

4 Simulation results

SPICE OPUS was used to simulate the circuit. The BSIM4 MOSFET device ver4.0 level 54 enhancement type was adopted for the MOSFET device. The parameter of this device was used as the base model in this paper.

3 MOSEFT models that each represent the performance in frequency, MOSFET guaranteed to outperform existing performance, low power consumption was

designed. The performance was evaluated by simulating a 4-bit accumulator which was synthesized using the proposed method.

The model that represents the performance in speed showed a raise in max clock rate by 900% and decrease in power consumption by 70%, the model that represents MOSFET guaranteed to outperform existing performance outperformed the existing model in clock speed while it showed a decrease in power consumption by 99%, and the low power consumption model showed a decrease in power consumption by 99.93% while the max clock rate was reduced by 80%. Total energy consumption was reduced by 71% in the speed performance model, 99.5% in the MOSFET guaranteed to outperform existing performance model, and 99.6% in the low power consumption model.

5 Conclusion

Transistor with decreasing electric field scaling has the advantage in power consumption and total energy usage. Increase in max clock frequency was also achievable on certain voltages. The decrease in effective voltage due to the increase in the transistors on resistance is the cause to the decrease in the logic circuits max frequency when the supply voltage is decreased. But scaling law method also has the same problems. Therefore, it can be said that there are no differences between the currently existing methods of preoperational scaling while the gate oxide thickness is fixed to suppressed quantum tunneling. The calculation time which determines the logic circuits performance is determined by the multiplication of the gate capacitance and on resistance, in other words, latency. Therefore, even when the on-resistance is increased, by decreasing the gate capacitance in a greater value, it is possible to increase the performance of the logic circuit according to scaling that is independent to the physical property. However, because the problem of decrease in the transistors on current which originated from the proposed method exists, and that the evaluation was made only by simulation, problems such as processes technology remains as a task.