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High-Level Design Conditions and Techniques for Post-Fabrication Timing-Adjustable Datapaths

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The history of LSI is said to be the history miniaturization and speed improvement driven by the progress of fabrication-process technologies. In the past, wire delay was negligible small compared with gate-switching delay, but now the situation has been changed, that is, wire delay is no longer negligible because of the relative improvement of gate-switching delay. As a result, it makes difficult for synchronous circuit to distribute the clock signal without skew (clock phase difference between flip flops). In addition, the variation of signal transmission delay due to variations in fabrication processes becomes larger. Because of these factors, the yield degradation due to timing errors becomes a serious problem. Conventionally, the problem has been fixed by introducing a timing-margin, but it often degrades the circuit performance too much with an excess timing-margin. To overcome such excess timing-margin, a statistical static timing analysis has been studied for improving the accuracy of delay estimation. However it still depends on a fixed temporal margin, and the potential of each individual chip in not fully utilized. We now have another approach such timing issue, that is circuit adjustment of after fabrication. Deskew technique for avoiding timing error due to clock skew and intentional clock skew for avoiding timing error due to signal propagation delay are typical techniques for that purpose. However, the effectiveness of this skew adjustment often fabrication depends deeply on high-level datapath design. This research aims datapath synthesis considering skew adjustment, which can synthesize datapaths with high skew-adjustability under delay variation.

At first, the concept of the success rate of skew-adjustment has been introduced, and its computation algorithms have been studied. Algorithms are (1)exact one, (2)heuristic one and (3)Monte Carlo simulation-based one. Next, as for a first trial to skew-adjustable datapath synthesis, we have studied functional unit(FU) assignment in datapath synthesis. For a given computation algorithm to be implemented and the given operation schedule for this algorithm, we have shown the condition on FU assignment so that the resultant datapath fails in skew adjustment(there is no feasible skew assignment which can solve timing error due to delay variation). Remark that, from the computation process of skew assignment, no feasible skew assignment is equivalent to the existence of a positive cycle on a skew constraint graph which can be constructed algorithmically from the input computation algorithm and FU assignment. The condition says that is (1)two operations(o_1 and o_2) share one FU, or (2)one operation(o_1) and its successor(o_2)(direct or indirect) are assigned to one FU f_1 and another FU f_2, respectively and other pairs of an operation(o_i) and its successor(o_{i+1}) to f_2 and f_3,$\cdots$,f_{p-1} and f_p, and f_p and f_1, then a cycle is formed on a skew constraint graph. The difference between (a)the difference on scheduled control step for o_i and o_{i+1} and (b)the sum of execution times of operations which should be executed between o_i and o_{i+1} is considered as a timing margin, and it its value is small, the corresponding edge weight approaches to zero with negative value. Hence a cycle consisting of those edges can easily become a positive cycle. Based on those observations, (1)the importance of FU assignment to that at least one edge in any cycle has a sufficiently small edge weight is shown, and a FU assignment algorithm to satisfy this constraint has been proposed. In addition, (2)we have proposed a relaxed version of this constraint together with a FU assignment for this relaxed constraint. Finally, we have examined three FU assignments, i.e., conventional one, the relaxed version of skew-adjustable FU assignment and its original version. The original version needs the least namber of FUs in compensation for skew-adjustability. Using the relaxed version, we can reduce the number of FUs, but it still needs extra FUs compared with the conventional design.