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# Arithmetic Extended-Mapping for BICM-ID with Repetition Codes

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**Abstract** — A novel arithmetic extended mapping technique is proposed in this paper for bit-interleaved coded modulation with iterative decoding (BICM-ID) with repetition codes as well as for their modifications. With the proposed mapping scheme, the computational complexity of BICM-ID is significantly reduced compared with conventional quadrature amplitude modulation (QAM) mapping schemes. Performances of BICM-ID using the proposed extended mapping rules are also verified both by the extrinsic information transfer (EXIT) analysis and bit error rate (BER) simulations. The results show that with the proposed BICM-ID scheme, the code rate, at which, given the channel signal-to-noise power ratio (SNR) bit error rate can made arbitrarily small, is almost 90% of channel capacity, and such excellent property holds at relatively wide range of SNR values.

**Keywords**- extended mapping; repetition code; EXIT; BICM-ID; turbo coding; channel capacity;

## I. INTRODUCTION

It has long been believed that when designing wireless communication system using high order modulation such as 16 quadrature amplitude modulation (QAM), bit-wise separability from a symbol corresponding to the bit patterns allocated to the symbol is most important. Gray mapping is the most widely used modulation rule because of the reason described above.

Recently, a technique called bit interleaved coded modulation with iterative decoding (BICM-ID) [1] has been proposed, of which transmitter is a concatenation of an encoder and bit-to-symbol mapper, separated by an interleaver. In the receiver side, the iterative processing for demapping and decoding technique takes place. This is quite reasonable, because BICM-ID systems can be viewed as a serially concatenated turbo system, where the inner component is mapper and the outer component is the channel code used. Therefore, by iterations, bit separability can be enhanced, and bit error rate performance, as a whole can be significantly improved. In [2], it is shown that a BICM-ID scheme comprised of a combination of a constraint length 2 ( $K=2$ ) convolutional code and 8 amplitude shift keying (ASK) with (non-Gray) mapping rule, optimized assuming the availability of full *a priori* information, can achieve near Shannon capacity. Since the  $K=2$  (memory 1) convolutional code is a very “weak” code, it was rarely used in practical communication systems that do not use the iterative detection. In [2], it is shown through extrinsic information transfer (EXIT) analysis [3] that

the reason why such a simple structure can achieve excellent performance is because the EXIT functions of those two components are well-matched while the tunnel still opens until *a posteriori* mutual information reaches very close to one.

Another simpler BICM-ID scheme has been proposed in [4], where encoder is a concatenation of a single parity check code and a repetition code. The coded sequence is interleaved, and mapped on to a signal point in the utilized modulation format, where so called extended mapping [8] is assumed; with extended mapping more than  $M$  bits are allocated to one constellation point, when  $2^M$ -QAM is used. It is shown that the BICM-ID proposed in [4] can also achieve near capacity performance even the structure is extremely simple. However, since determining the optimal bit patterns allocated to the each constellation point for extended mapping that best matches the code structure belongs to the combinatorial problem, it is not practical to directly apply the Ref. [4]’s technique to higher order modulation schemes.

This paper proposes a new BICM-ID scheme, arithmetic mapping BICM-ID, for the systems using higher order modulation. Our proposed technique can also achieve very close-capacity performance. Furthermore, our proposed scheme replace the symbol-level extended mapping by bit-reduction encoding, which can be seen as alternative way of mapping multiple patterns to the same constellation point. This technique eliminates the likelihood calculations for more than  $2^M$  patterns, resulting in significant reduction in computational complexity. This paper also proposes the use of per-dimension non-Gray ASK to eliminate the difficulty in obtaining the optimal allocation pattern, which, as noted above, falls into a combinatory optimization problem.

Results of the EXIT analysis and BER simulation results, conducted to verify the effectiveness of the proposed technique are presented in this paper. It is shown in this paper that the results are exactly consistent with each other. It is noted that this contribution forms a sister paper of another contribution [11] made by one of the authors of this paper.

## II. BICM-ID WITH REPETITION CODE

### A. System Model

In this paper, BICM-ID scheme proposed in [4] is assumed. The schematic diagram of Ref [4]’s proposed technique is

shown in Fig. 1, but because of the space limitation, this paper only provide important properties/observations of the Ref. [4]'s technique. For more details, please see [4].

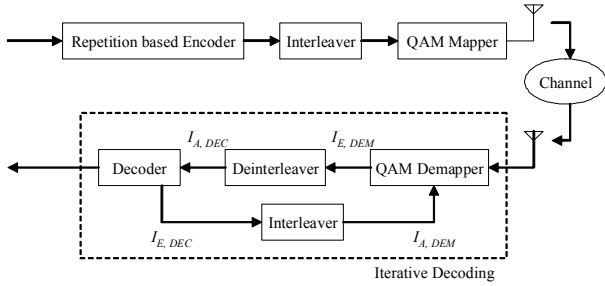


Fig. 1. System Model.

### B. Designing BICM-ID with Repetition Code

As mentioned above, even a “weak” code can be utilized in BICM-ID if the EXIT curves are well matched to that of the demapper. The EXIT function of the repetition code is expressed as

$$I_{E,VND}(I_A) = J(\sqrt{d_v - 1} \cdot J^{-1}(I_A)) \quad (1)$$

where  $d_v$  denotes the repetition times,  $J(\cdot)$  is the function introduced in [3] that converts the standard deviation of the log likelihood ratio (LLR) to mutual information in AWGN channels,  $J^{-1}(\cdot)$  is its inverse function, and  $I_A$  is *a priori* mutual information between the coded bit and the decoder input LLR [5], [6]. Fig. 2 shows EXIT curves of repetition codes with, as a parameter, several different repetition times, referred to as variable node degree  $d_v$ . It is found that the EXIT curves exhibit convex shape with values between the mutual information value being 0 and 1, of which tendency is common to the variable node degree  $d_v$  larger than 2, and the higher the repetition time is, the sharper the convexity of the shape.

Optimization of QAM mapping rule for BICM-ID schemes are discussed in [2], [7] and [8]. The modulation schemes used in these references are non-Gray mappings, of which EXIT curves exhibits relatively sharp rising decay so that they are matched to the EXIT curve of short memory code decoders. This paper however, their decay is not sharp enough in convexity to better match the repetition codes.

Fig. 3 shows EXIT curves of a non-Gray mapped 256-QAM demapper at SNR=0, 5, 10, 15 and 20dB. It is found that non-Gray mapping, in general, with per-symbol bits allocation larger than two times the channel capacity has its EXIT curve exhibiting rising convex shape. In the case of Fig. 3, the mapping rule is optimized such that with full *a priori* information, the extrinsic mutual information has the largest value. Hence, extrinsic mutual information at the EXIT curve's right most point is increased, while that the left most pint is decreased. However, the area below demapper's EXIT curve is equal to averaged constellation constrained capacity (CCC) per bit, according to the area property [9]. Thus the number of bits assigned to one constellation point is larger than two times the channel capacity, EXIT curve becomes convex shape. With

256-QAM, for example, 8 bits are assigned to one modulation symbol while the channel capacities are 1.00, 2.06, 3.46, 5.23 and 6.66 bits/symbol at SNR=0, 5, 10, 15 and 20 dB, respectively. At SNR=0, 5 and 10 dB, number of bits assigned to one modulation symbol is larger than two times the capacity. As a result, the EXIT curves of 256-QAM optimized with *a priori* information exhibit convex shapes at SNR=10, 5 and 0 dB, as shown in Fig. 3.

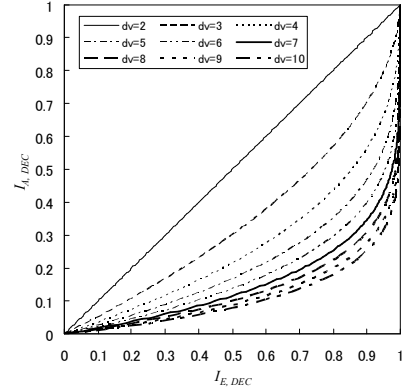


Fig. 2. EXIT curves of repetition codes

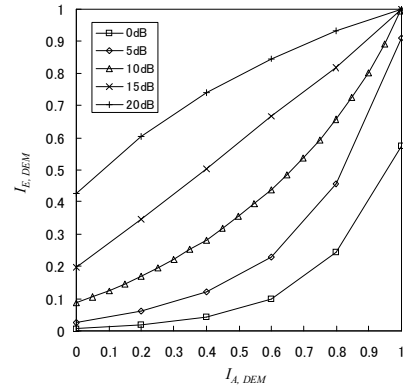


Fig. 3. EXIT curves of a 256-QAM demapper at SNR=0, 5, 10, 15 and 20dB.

Ref. [4] introduces two additional techniques to achieve flexibility in changing the shape of the EXIT curve; one is irregular degree allocation to the variable nodes (=repetition times take different values in one frame to be transmitted), and the other serial concatenation of the repetition code (inner code) and single parity check code (outer code).

The EXIT function of variable node with irregular degree allocation is expressed as

$$I_{E,VND}(I_A) = \frac{\sum_i a_i d_{v,i} \cdot J(\sqrt{d_{v,i} - 1} \cdot J^{-1}(I_A))}{\sum_i a_i d_{v,i}}, \quad (2)$$

where  $a_i$  denotes the number of variable node of which degree is  $d_{v,i}$ .

When the serially concatenating the single parity check code as the outer code, parity bits are appended, according to the information bits. Afterwards, information bits as well as the parity bits are encoded by the repetition code encoder. Fig. 4 shows effect of single parity check codes, where it is found that the right part of the EXIT curve is further shifted to the right. On the contrary, it is found from Eq. (2) that irregular degree allocation affects the whole portion of the curve.

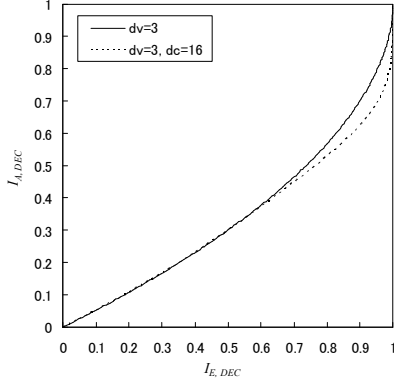


Fig. 4. Effect of single parity check code for repetition code.

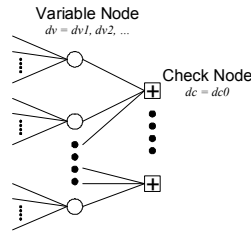


Fig. 5. Tanner graph of repetition-based code in [4].

The whole decoder structure presented in [4] is shown in Fig. 5. The EXIT function of the decoder is expressed as

$$I_{E,DEC}(I_{A,DEC}) = \frac{\sum_i a_i \cdot d_{v,i} \cdot J\left(\sqrt{(d_{v,i}-1) \cdot J^{-1}(I_{A,DEC})^2 + J^{-1}(I_{E,CND,i})^2}\right)}{\sum_i a_i \cdot d_{v,i}}, \quad (3)$$

where  $I_{E,CND,i}$  is the extrinsic mutual information output from the check node connected to variable node with degree  $d_{v,i}$ , and  $I_{E,CND,i}$  is the output of the check node decoder. It is well known that  $I_{E,CND,i}$  can be approximated by

$$I_{E,CND,i} \approx 1 - J\left(\sqrt{d_c - 1} \cdot J^{-1}(1 - I_{A,CND,i})\right), \quad (4)$$

where  $I_{A,CND,i}$  is a *a priori* information input to the check node and  $d_c$  is degree of the check node, as described in [5], [6]. If each check node is connected uniformly to variable nodes the mutual information of the variable nodes decoder output can be expressed as

$$I_{A,CND,i} = \frac{\sum_j a_j \cdot J\left(\sqrt{d_{v,j}} \cdot J^{-1}(I_{A,DEC})\right)}{\sum_j a_j}. \quad (5)$$

If each check node is connected to only the variable nodes having the same degree  $d_{v,i}$ ,  $I_{A,CND,i}$  is expressed as

$$I_{A,CND,i} = J\left(\sqrt{d_{v,i}} \cdot J^{-1}(I_{A,DEC})\right). \quad (6)$$

As described above, Ref. [4]'s proposed coding scheme enables flexible design of its EXIT curve shape so as to match the decoder EXIT curve shape of demapper. Furthermore, local iteration in the decoder is not required, because each variable node is connected to only one check node. If not, iteration between variable nodes and check nodes is necessary, like in the LDPC codes. This significantly reduces the computational complexity of the decoding process.

### C. Coding rate of the Repetition Code with Single Parity Check Code.

First, one single parity check bit is appended to each set of  $d_c - 1$  information bits, and thus the coding rate of the single parity check code is  $(d_c - 1)/d_c$ . Afterwards,  $a_i$  bits are repeated by repetition encoder with degree  $d_{v,i}$ , thus the total number of coded bits are  $\sum_i a_i d_{v,i}$  while the number of the bits before repetition is  $\sum_i a_i$ . Thus the total coding rate of the repetition code with single parity check code, described above, is shown as

$$\frac{\sum_i a_i}{\sum_i a_i d_{v,i}} \cdot \frac{d_c - 1}{d_c}. \quad (7)$$

## III. EXTENDED MAPPING DESIGN

Even though the coding scheme proposed in [4] provides us with a lot of flexibility in designing EXIT curve, we need further degrees of freedom in designing the EXIT curve for the QAM mapping rule so that demapper and decoder EXIT curves have exact matching. To achieve this goal, QAM with per-symbol bit number larger than twice the channel capacity, optimized with full *a priori* information, provides us with a good solution. This section proposes a new, but very simple coding scheme that can provide further design flexibility.

### A. Demapping Operations

If an  $M$  bit pattern  $(b_0, b_1, \dots, b_{M-1})$  is mapped onto one of the  $2^M$  constellation points  $(c_0, c_1, \dots, c_{2^M-1})$ , the extrinsic LLR of the coded bit, output from the demapper, can be calculated as

$$L_e(b_i) = \log \frac{\sum_{c_k | c_k(b_i)=0} p(x | c_k) \cdot p(c_k | b_i = 0)}{\sum_{c_k | c_k(b_i)=1} p(x | c_k) \cdot p(c_k | b_i = 1)} \quad (8)$$

for the bit  $b_i$ , where  $x$  is the received sampled value of the symbol. The probability density function (pdf) of  $x$  is given by

$$p(x | c_k) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{|x - c_k|^2}{2\sigma^2}\right) \quad (9)$$

in additive white Gaussian noise (AWGN) channel with a noise variance  $\sigma^2$  and

$$p(c_k | b_i = b) = \prod_{j \neq i} \frac{\exp(-c_k(b_j)L_a(b_j))}{1 + \exp(-L_a(b_j))}, \quad (10)$$

where  $c_k(b_j)$  is the  $j$ -th bit value (0 or 1) on the constellation point  $c_k$  and  $L_a(b_j)$  is the *a priori* LLR of the bit  $b_j$ . Eq. (8) can be simplified to

$$L_e(b_i) = \log \frac{\sum_{c_k | c_k(b_i)=0} \exp\left(-\frac{|x-c_k|^2}{2\sigma^2} - \sum_j c_k(b_j)L_a(b_j)\right)}{\sum_{c_k | c_k(b_i)=1} \exp\left(-\frac{|x-c_k|^2}{2\sigma^2} - \sum_j c_k(b_j)L_a(b_j)\right)} - L_a(b_i). \quad (11)$$

In practice, the demapper has to calculate

$$\frac{|x-c_k|^2}{2\sigma^2} + \sum_j c_k(b_j)L_a(b_j) \quad (12)$$

for every  $c_k$  first, then  $L_e(b_i)$  using (11). This means that the complexity of demapper is in exponential order of number of bits assigned to one modulation symbol. Though this is common to any BICM-ID schemes, the BICM-ID with repetition code is even more complex because it requires larger number of bits assigned to modulation symbol. While it does not affect much at low SNR, it is computationally expensive at relatively high SNR. If SNR is 20dB, for example, 12~16 bits have to be allocated to one symbol because the capacity is more than 6 bits/symbol. Thus, demapper have to calculate the values of (12) 4096~65536 ( $2^{12} \sim 2^{16}$ ) times per each symbol, which may impose unacceptable computational burden for practical applications. The complexity problem due to  $\exp()$  and  $\log()$  in (11) may well be avoided by the Max-Log-Map algorithm, but that for (12) still can not be avoided.

### B. Extended Mapping

In [8], a mapping technique, “Extended Mapping,” is introduced, where the number of bits mapped to each constellation point is larger than  $M$ , with the modulation having  $2^M$  signal points. The bit patterns allocated to one symbol is determined such that the demapper EXIT function has a preferable shape. Ref. [4] presents a BICM-ID technique with extended mapping only with 4-QAM modulation. In this paper, it is shown that using extended mapping, BICM-ID can perform well even if the number of constellation size is larger. Fig. 6 compares EXIT curves of 256-QAM with extended 16-QAM having 8 bits per one symbol. Both are optimized such that with full *a priori* information, the extrinsic mutual information takes the largest value. It is found that both curves are almost the same at SNR=7dB. This is because the number of constellation points 16 ( $=2^4$ ) is enough to deliver  $\sim 2.6$  bits/symbol, which is the channel capacity at SNR=7dB. Therefore, extended mapping is a good choice because with if extended mapping, the total number of the first terms of (12) is reduced. However, the second terms are still unchanged.

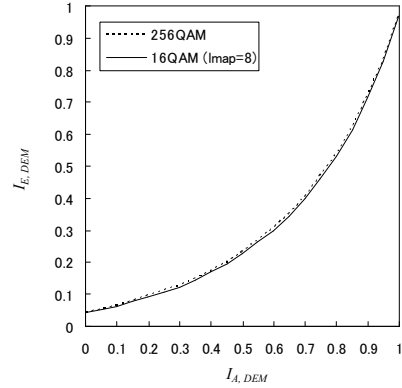


Fig. 6. Comparison of EXIT curves of a 256-QAM and of an extended 16-QAM ( $I_{map}=8$ ) demapper (SNR=7dB)

### C. Arithmetic Extended Mapping

To reduce the complexity due to the second term of (12), we proposed a novel extended mapping technique, named “Arithmetic Extended Mapping.” Our proposed scheme further extends the mapping rule according to an “arithmetical” rule. First, the number of bits to be mapped on to a symbol is reduced by a set of check node encoders, referred to as “bit-reduction encoder” in this paper. The purpose of the “bit-reduction encoding” is to reduce the number of the bits to be mapped onto one symbol to the number which standard (i.e. not extended) mapping rule allocates to each symbol. An example of bit-reduction encoder is shown in Fig. 7, where the symbol boxed-plus denotes check sum (exclusive-OR) operation. Eight bits ( $b_0, b_1, \dots, b_7$ ) are input to the bit-reduction encoder and four bits ( $m_0, m_1, \dots, m_3$ ) are output. Afterwards, the bits ( $m_0, m_1, \dots, m_3$ ) are mapped onto one 16-QAM symbol by the normal (non-extended) mapping rule. With this operation, still 8 bits ( $b_0, b_1, \dots, b_7$ ) can be transmitted using only 16 combinations, with help of *a priori* information at the receiver.

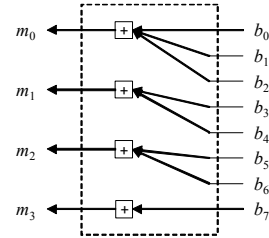


Fig. 7. Example of bit-reduction encoder.

In the receiver, first the demapper calculates from the received symbol with no *a priori* information the extrinsic information for the bits ( $m_0, m_1, \dots, m_3$ ). The extrinsic information of ( $b_0, b_1, \dots, b_7$ ) is then calculated using extrinsic information for the bits ( $m_0, m_1, \dots, m_3$ ) provided by the bit-reduction decoder, as

$$L(u_1 \oplus u_2 \oplus \dots \oplus u_n) = 2 \tanh^{-1} \left( \prod_{i=1}^n \tanh \frac{L(u_i)}{2} \right), \quad (13)$$

which is exactly the same operation as a check node decoder of the LDPC codes. For example, the extrinsic output for  $b_0$  in Fig.

7 can be calculated by (13), using extrinsic LLR for  $m_0$  from the demapper and *a priori* information for  $b_1$  and  $b_2$ . In decoding, the *a priori* information from the decoder of the outer code (=Ref. [4]'s proposed structure), which is provided via the interleaver, is used by the check node decoder to update the LLR, according to (13). The output of the check node decoder is input to demapper as *a priori* information. The demapper calculates the updated extrinsic information using the *a priori* information from the check node decoders using (11) and (12).

It should be noted here that for any codeword, bit  $b_i$  should not affect more than one modulation bit  $m_j$  in the bit-reduction encoder. This is because (13) is correct only if the all inputs to the check node decoder are considered as independent. Because the outputs of the QAM demapper corresponding to the identical received signal are not independent, another interleaver should be placed between QAM demappers and check node decoders, similarly to the MIMO case, as shown in [5]. This requires local iterations to be performed, which increases computational complexity.

In the proposed scheme, the computational complexity of the demapper is reduced significantly because the number of the second term in (12) is not affected by the length extension for mapping. The number of constellation points should be only necessary enough to achieve near Shannon capacity performance. The convexity of the EXIT curve can be realized by bit-reduction encoder, as well as the QAM mapping rule. In other words, the shape of EXIT curve can be designed by both mapping rule of the modulator and check node degree allocations in the bit-reduction encoder.

Though the flexibility of design of the proposed scheme is less than the extended mapping introduced in [8], still it preserves large degrees-of-freedom in flexibly changing the shape of the EXIT curve so that it is better-matched to the EXIT curve of the repetition code, as described later.

The computational complexity of the demapping can further be greatly reduced if the mapping is performed independently in-phase and quadrature dimensions. In Fig. 8, two 8-bit codewords (each denoted by  $b_0, b_1, \dots, b_7$  and  $b_8, b_9, \dots, b_{15}$ ) are reduce to two 4-bits ( $m_0, m_1, \dots, m_3$ ) codewords, respectively by the bit-reduction encoder described above. The each 4-bits codeword is mapped on to a non-Gray 16-ASK modulation, independently between in-phase and quadrature dimensions (I-ch and Q-ch, respectively), which are then combined into a complex I+jQ symbol. This technique is very suitable especially when high order modulation is required at a relatively large SNR range, say, SNR=20dB. This is because the complexity for demapping of 256-QAM may still be too large for practical use. Therefore, splitting the complex modulation into two one-dimensional modulation is very effective in reducing the complexity. In this case, the calculation of (12) for only 32 points (16 points for each 16-ASK demapper) is needed, and the processing for check node decoder is easy even if 16 bits are mapped onto one modulation symbol. The complexity is extremely low and it is no longer "exponential order" of the modulation multiplicity.

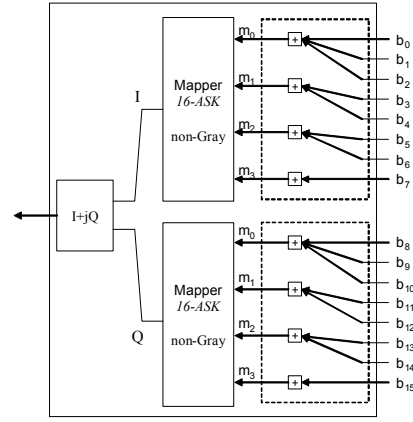


Fig. 8. Arithmetic extended mapping 256-QAM ( $L=16$ )

#### D. Designing Arithmetic Extended Mapping

Even with the simplified scheme shown in Fig. 8, our proposed arithmetic extended mapper still has enough flexibility to the EXIT curve shape so that it is well-matched to the repetition code. We also preserve the flexibility in determining the degree allocation of check nodes in bit-reduction encoder as well as mapping rule of ASK (or QAM). The extrinsic information from the decoder for arithmetic extended mapper, without *a priori* information, is expressed as

$$I_{E,DEM}(0) = \frac{\sum_{i|d_{c,i}=1} I_{E,m_i}(0)}{\sum_{i|d_{c,i}=1} 1} \quad (14)$$

where  $I_{E,m_i}(0)$  and  $d_{c,i}$  denotes the extrinsic output of the non-Gray demapper without *a priori* information, and the degree of a check node connected to the modulation bit  $m_i$ . The extrinsic information  $I_{E,m_i}(0)$  of the bit  $m_i$ , to which the degree of the check node connected is more than 1, does not affect the extrinsic information output from arithmetic extended demapper without *a priori* information; this is because the check node decoder output is zero if one of its inputs is zero, as shown in (13). This means at least one check node has to have degrees  $d_c=1$ , as shown in Fig. 7. Otherwise, the demapper cannot extract any information from received signal at the first iteration. The less number of check node decoders with  $d_c=1$ , the less extrinsic information at the left most point. Moreover, the smaller the  $I_{E,m_i}(0)$  values for check node decoders with  $d_c=1$ , the less extrinsic information at the left most point.

However, on the contrary, the extrinsic information with full *a priori* information from the arithmetic extended demapper is described as

$$I_{E,DEM}(1) = \frac{\sum_i d_{c,i} I_{E,m_i}(1)}{\sum_i d_{c,i}}, \quad (15)$$

where  $I_{E,m_i}(1)$  is the extrinsic output of the non-Gray demapper with full *a priori* information. The outputs of non-Gray demapper are weighted by  $d_{c,i}$  in (15). This means that the

extrinsic information at the right most point gets larger if the check node decoder having higher degrees, is connected to the modulation bit  $m_i$  of which extrinsic output  $I_{E,m_i}(l)$  from non-Gray demapper is larger. Thus, to maximize the extrinsic output with full *a priori* information, maximum allowed number of the check node degree has to be assigned to, at least, one modulation bit, and check node degrees=1 is assigned to the others. Then, optimization of mapping rule, which maximizes (15), is completed. Any results of the optimization directly conducted to the extended mapping in [8], are supposed to be equivalent to the result of the optimization above, if the optimization is perfectly performed for maximizing extrinsic output. This optimization can be performed by using binary switching algorithm (BSA) introduced in [10]. BSA often stacks on local maximums especially in the case of the total number of bits assigned is large. However, optimization of mapping rule of non-Gray mapping for arithmetic extended mapping rarely stacks on local maxima because the number of bits of the non-Gray mapping is smaller than that of extended mapping. Moreover, optimization of the arithmetic extended mapping using BSA converges in much less steps than direct optimization for extended mapping.

Fig. 9 shows an example of the result of the optimization. The optimization with weights of  $d_{c,i}=\{5, 1, 1, 1\}$  and  $d_{c,i}=\{3, 2, 2, 1\}$  using BSA result in the same mapping rule shown in Fig. 9. EXIT curves of the arithmetic extended mapping, which is a combination of non-Gray 16-ASK shown in Fig. 9 and the bit-reduction encoders with check node degree of  $d_{c,i}=\{5, 1, 1, 1\}$  and  $d_{c,i}=\{3, 2, 2, 1\}$ , are shown in Fig. 10 and Fig. 11, at SNR=15dB and 5dB, respectively. It is found that the extrinsic outputs without *a priori* information (at left most point) are reduced, while they are increased with full *a priori* information (at right most point), compared with that of the demapper itself for 16-ASK shown in Fig. 9. It is also found that the bit-reduction encoder with check node degrees allocation of  $\{3, 2, 2, 1\}$  is better matched with the EXIT curves of the repetition code at SNR=15dB, while  $\{5, 1, 1, 1\}$  is slightly better at SNR=5dB. As mentioned above, the result with  $d_{c,i}=\{5, 1, 1, 1\}$  is supposed to maximize the extrinsic output with full *a priori* information. However, it is not always the best solution for the BICM-ID with the repetition code. In the case the output at right most point is high enough, it is better to reduce the left most hand, as shown in Fig. 10. Thus, we choose the degree allocation of  $d_{c,i}=\{3, 2, 2, 1\}$  with non-Gray 16-ASK presented in Fig. 9 as an example in evaluations hereafter. The EXIT curves of the demapper for Fig. 8 with non-Gray 16-ASK mapping in Fig. 9 at several SNR points are shown in Fig. 12. It is shown that the EXIT curves exhibit rising convex shapes in a wide range of SNR. The demapper EXIT curve can be designed more flexibly using modulation doping technique proposed in our sister paper [11].

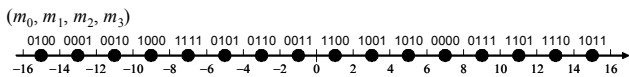


Fig. 9. Base Mapping (Optimized non-Gray 16-ASK)

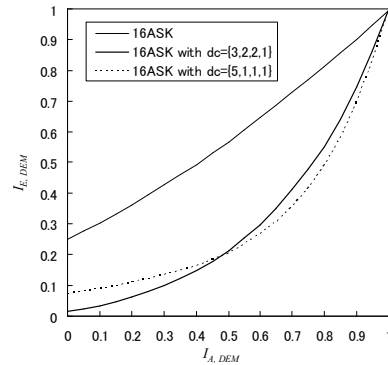


Fig. 10. EXIT curve of arithmetic extended mapping at SNR=15dB

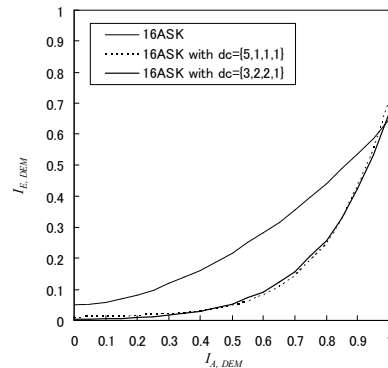


Fig. 11. EXIT curve of arithmetic extended mapping at SNR=5dB

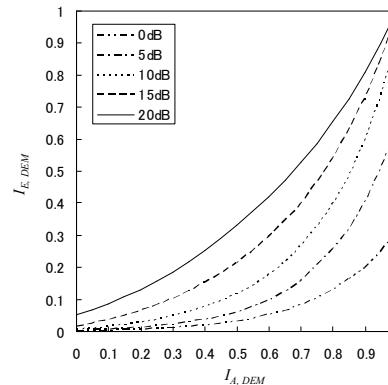


Fig. 12. EXIT curves of a demapper of proposed mapping at SNR=0, 5, 10, 15 and 20dB.

### E. Design Example of the Repetition Codes for proposed mappings

A block diagram of the whole structure of the proposed BICM-ID scheme is shown in Fig. 13. The multiplexers/demultiplexers for I-ch and Q-ch in Fig. 8 are not shown explicitly. The code design example for each SNR in Fig. 12 are listed in TABLE I. The EXIT curves of the codes, listed in TABLE I, are calculated using (3). Their shapes are well-matched to that of the demapper in Fig. 12 at SNR=20, 15, 10, 5 and 0dB as shown in Fig. 14~Fig. 18 respectively. The

combination of the arithmetic extended mapping, proposed in this paper, and repetition code with single parity check code, proposed in [4], is expected to perform near Shannon capacity performance, because the gap between EXIT curves of the decoder and demapper, which corresponds to the rate loss, is extremely small, as shown in Fig. 14~Fig. 18. The rate loss can not be reduced anymore, especially at SNR=15dB and 10dB. This means the bit rates achieved by the proposed BICM-ID almost reach the CCC of the QAM constellation.

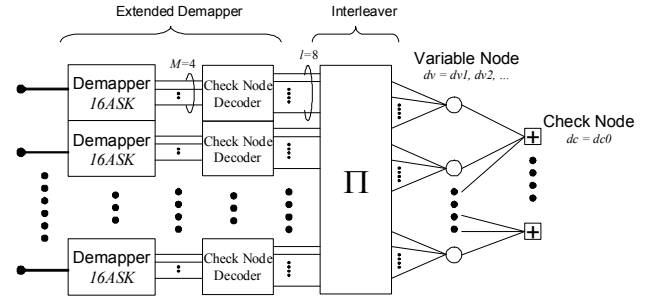


Fig. 13. Proposed BICM-ID scheme using arithmetic extended mapping.

TABLE I. CODE DESIGN EXAMPLES

Code Type	Code design		
	Variable node degrees	Check node degree	Coding rate
I	$d_{v1}=11$ (93 %), $d_{v2}=100$ (7 %)	$d_c=8$	0.0508
II	$d_{v1}=5$ (93 %), $d_{v2}=50$ (7 %), $d_{v3}=100$ (0.1 %)	$d_c=32$	0.1175
III	$d_{v1}=3$ (87 %), $d_{v2}=15$ (13 %), $d_{v3}=80$ (0.6 %)	$d_c=512$	0.1992
IV	$d_{v1}=2$ (44 %), $d_{v2}=3$ (35 %), $d_{v3}=5$ (14 %), $d_{v4}=12$ (7 %)	$d_c=512$	0.2876
V	$d_{v1}=2$ (55 %), $d_{v2}=3$ (33 %), $d_{v3}=5$ (12 %)	$d_c=1024$	0.3714

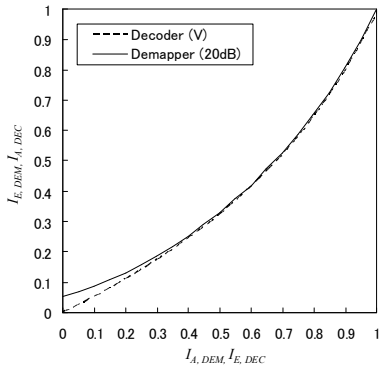


Fig. 14. EXIT chart of proposed mapping with the Code V (SNR=20dB)

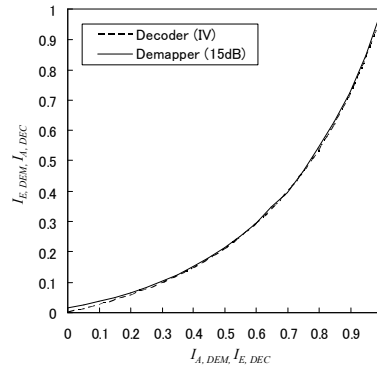


Fig. 15. EXIT chart of proposed mapping with the Code IV (SNR=15dB)

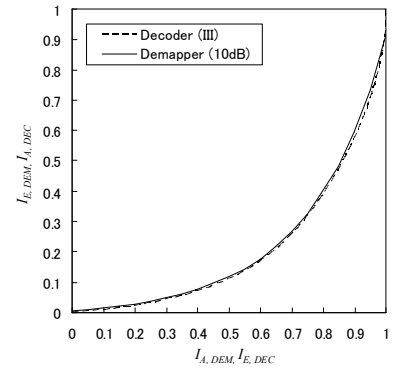


Fig. 16. EXIT chart of proposed mapping with the Code III (SNR=10dB)

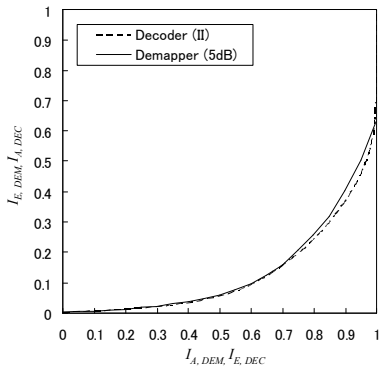


Fig. 17. EXIT chart of proposed mapping with the Code II (SNR=5dB)

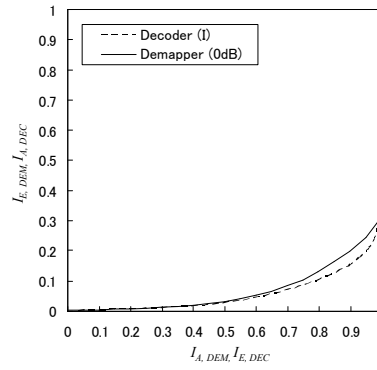


Fig. 18. EXIT chart of proposed mapping with the Code I (SNR=0dB)

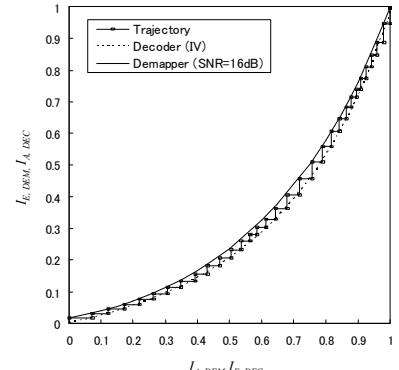


Fig. 19. Exemplifying trajectory of the proposed BICM-ID

#### IV. CHAIN SIMULATION RESULTS

A series of chain simulations assuming the conditions summarized in TABLE II were conducted. The block size of

about 5000 information bits is chosen in the simulations for practicality. The codes listed in TABLE I are used, which are designed to match the arithmetic extended mapping shown in Fig. 8 with non-Gray 16-ASK mapping presented in Fig. 9 at



SNR=0, 5, 10, 15 and 20dB. An example of the snapshot trajectory on EXIT chart is shown in Fig. 19, together with its corresponding EXIT chart. Since the code IV is designed at SNR=15dB, narrow tunnel is constantly open between the mutual information 0 to almost 1 at SNR=16dB. The trajectory shown in Fig. 19 is very well matched with the EXIT curves. Fig. 20 shows the BER simulation results. Sharp turbo cliffs appear at the targeted SNRs. If the code size is larger, the turbo cliffs will be even shaper. It is also shown that BER floor at below  $10^{-3}$  appears with code I and II, which are caused only by the intersection points of EXIT curves, because there are no cycles in the decoder. The BER floor can be reduced by redesigning the mapping rule since the mapper used in this simulation is designed to match at relatively high SNRs, thus the gaps between EXIT curves at SNR=0dB around right most point is larger than with higher SNRs, as shown in Fig. 18. If an arithmetic extended mapper with less number of bits assigned is used, the curves should be better-matched with repetition codes at low SNRs, say, SNR=0 and 5dB. Although proposed BICM-ID scheme has BER floor more or less due to the intersection point in EXIT chart, it can be designed so as to reduce the floor to a smaller level than the values allowed practically, using both flexibilities of the repetition code and the mapping scheme. This is one of the significant advantageous points of the proposed BICM-ID scheme.

The bit rates achieved by the proposed BICM-ID are shown in Fig. 21, as well as the bit rates achieved by the BICM-IDs presented in [2], [7] and [8] with “plus”, “cross” and “triangle” marks, respectively. Fig. 21 shows that our proposed BICM-ID outperforms the other BICM-ID schemes, even with its extremely simple structure.

TABLE II. SIMULATION CONDITIONS

Item	Values
Number of Information bits	about 5000 bits (Minimum multiple of $d_c-1$ , which is greater than or equal to 5000)
Modulation	Arithmetic Extended Mapping of Fig. 8 with 16-ASK in Fig. 9.
Coding	Code I, II, III, IV and V in TABLE I.
Interleaver	Random interleaver
Data	Random binaries
Channel	AWGN
Number of Iterations	100

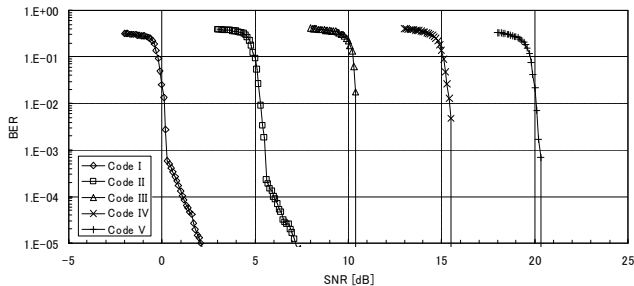


Fig. 20. Bit error rates simulation results of the proposed BICM-ID scheme.

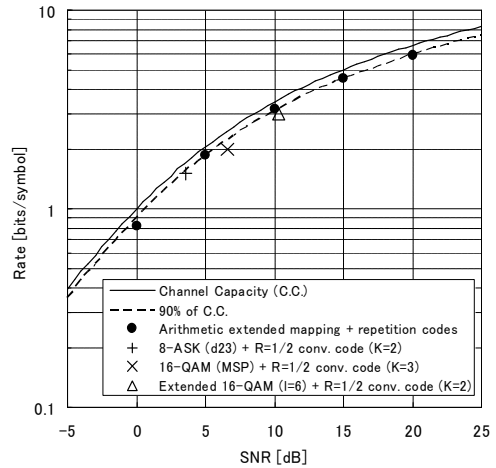


Fig. 21. Bit rates achieved by the proposed BICM-ID

## V. CONCLUSION

A novel mapping technique, named arithmetic extended mapping, has been proposed for BICM-ID with repetition codes and their modifications. The computational complexity in the demapper can be reduced significantly using proposed extended mapper. Performance of proposed BICM-ID scheme has been verified both by EXIT analysis and BER simulations. The results show that the proposed BICM-ID can achieve almost 90% of channel capacity even at relatively high SNRs.

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