Totally solution-processed ferroelectric-gate thin-film transistor

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We have fabricated inorganic ferroelectric-gate thin film transistors (FGTs) using only a chemical solution deposition (CSD) process. All layers, including the channel [indium-tin-oxide (ITO)], ferroelectric-gate insulator [$Pb(Zr,Ti)O_3$], gate electrode ($LaNiO_3$) and source/drain electrodes (ITO), were formed by the CSD process. The fabricated FGT exhibited typical n-channel transistor operation with good saturation in drain current and drain voltage (I_D-V_D) characteristics. The obtained on/off current ratio, memory window, and subthreshold voltage swing were about 10^7, 2.5 V, and 420 mV/decade, respectively. © *2010 American Institute of Physics*.
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Metal-oxide materials exhibit a wide range of electrical properties and metal-oxide films have been intensively studied for applications in various electronic devices. In particular, the use of metal oxide films for thin-film transistors (TFTs) is very promising. Such TFTs include not only transistors for flat-panel displays and system-on-panel, in which oxide semiconductors such as ZnO,[1] In–Zn–O (IZO),[2] and In–Ga–Zn–O (IGZO) (Ref. 3) have been studied for active channels but also transistors for nonvolatile memories using ferroelectric films as gate insulators. The latter types of ferroelectric-gate TFTs (FGTs) with a stacked semiconductor/ferroelectric structure are one of the most promising candidates for oxide-based nonvolatile memory because they do not require a Si substrate and because of their simple device structure, low power consumption, and high-speed operation. FGTs' simple device structure facilitates both easy scalability and low processing costs together with a wide selection of substrates. We already reported good transistor operations of the FGTs using $(Bi,La)_4Ti_3O_{12}$ (Ref. 4) or $Pb(Zr,Ti)O_3$ (PZT) (Ref. 5) film as a gate insulator and indium-tin-oxide (ITO) film as a channel. However, these TFTs and FGTs are generally prepared by using mainly conventional vacuum deposition processes such as sputtering, pulsed laser deposition, chemical vapor deposition, and so on which result in high fabrication costs.

As an alternative to the conventional vacuum deposition process, a solution deposition process would facilitate low cost processing because of its low equipment costs, process simplicity and direct patternability by using printing techniques. Recently, TFTs with solution-processed conductive metal-oxide channels composed of ZnO,[6,7] IZO,[8,9] and ITO (Ref. 10) have been reported. However, those TFTs only partially employed a solution-based fabrication process, with conventional vacuum deposition processes being used to fabricate other parts of the device. To achieve ultralow cost fabrication, it is critical to employ a totally solution-based process, in which all parts of the device are fabricated from solution-derived materials only. This total solution processing could eventually lead to "total printing electronics" for further cost reduction.

In this study, we present FGTs in which all layers were fabricated by a chemical solution deposition (CSD) process. We used $LaNiO_3$ (LNO) film as a gate electrode on which a PZT ferroelectric gate insulator was formed, and ITO films were used both for the channel and as source-drain electrodes. The fabricated FGT had a bottom gate electrode and bottom contact source-drain electrodes on a single-crystal $SrTiO_3$ (STO) substrate as shown in Fig. 1(a). Figure 1(b) shows the magnified top-view microscope image of this device. We adopted LNO film as a gate electrode to obtain PZT film with good crystalline quality and electrical properties because LNO is a perovskite-type conductive oxide with a lattice constant of a= ~3.86 Å that is comparable with that of PZT (a= ~4.01 Å).

To prepare the FGT, the LNO bottom gate (100 nm) was first formed by the CSD process. A precursor solution of LNO film was prepared by dissolving 0.1 mol/kg lanthanum nitrate hexahydrate $[La(NO_3)_3 \cdot 6H_2O]$ and 0.1 mol/kg nickel acetate tetrahydrate $[Ni(OAc)_2 \cdot 4H_2O]$ in an alcohol solvent. The LNO precursor solution was spin coated on STO(111) substrate, dried at 160 °C in air for 5 min and then crystallized at 750 °C in O_2 for 15 min. Then, the LNO gate electrode was patterned by photolithography and wet-etching. In

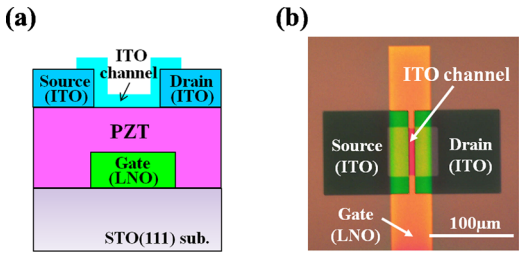

FIG. 1. (Color online) (a) Device structure of FGT and (b) top view microscope image of FGT.

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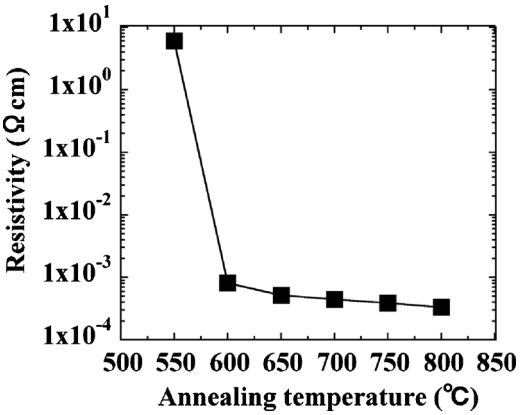

FIG. 2. Resistivity of LNO films on STO(111) substrate as function of annealing temperature.

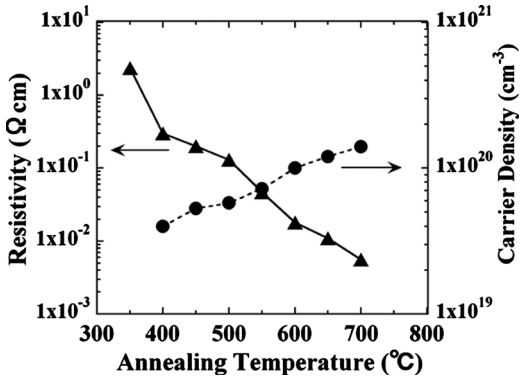

FIG. 3. Resistivity and carrier density of ITO films as function of annealing temperature.

the second step of the FGT fabrication, the $Pb_{1.2}Zr_{0.4}Ti_{0.6}O_3$ (PZT) gate insulator (255 nm) was formed by the CSD process. We used an alkoxide-based PZT precursor solution. This solution was spin coated, dried at 240 °C in air for 10 min and consolidated at 400 °C in air for 10 min. Then, a gate contact hole was formed by photolithography and wet-etching. After that, the PZT film was crystallized at 625 °C in air for 15 min. In the third FGT fabrication step, the ITO source-drain electrodes (200 nm) were formed by the CSD process using a carboxylate-based ITO precursor solution (5 wt % SnO_2-doped). This solution was spin coated on the PZT layer, consolidated at 300 °C in air for 10 min and patterned by photolithography and wet-etching. After the exposed PZT surface (the channel region) was treated by Ar plasma, the ITO source-drain electrodes were crystallized at 600 °C in air for 15 min. Finally, the ITO channel (20 nm) was fabricated by the CSD process. The ITO precursor solution was spin coated, consolidated at 300 °C in air for 10 min and patterned by photolithography and wet-etching followed by crystallization at 450 °C in air for 40 min. The channel length (L_{SD}), channel width (W) and gate electrode width (L_G) of the fabricated device were 5 μm, 60 μm, and 50 μm, respectively.

Figure 2 shows the dependence of the resistivity of LNO films (100 nm) fabricated on STO(111) substrates on annealing temperature. The resistivity was measured by using the four probes method. As figure shows, low resistivity less than 10^{-3} Ω cm, which is lower than the reported one,[11–13] was obtained when the film was annealed at higher than 600 °C. Figure 3 shows the resistivity and carrier density of ITO films (20 nm) measured by using the van der Pauw method. The resistivity of the 20-nm-thick ITO thin film decreased with increasing annealing temperature, whereas the carrier density increased with increasing annealing temperature. Notably, ITO was used both as a channel layer and for the source-drain electrodes in the FGTs prepared here. Because a channel requires an appropriate carrier density for its complete depletion, whereas the electrodes require low resistivity, we prepared these two types of ITO films under different annealing conditions according to the results shown in Fig. 3. In particular, a 450 °C-annealed ITO film was used for the channel to achieve a carrier density of 4.8×10^{19} cm^{-3} and a resistivity of 2.0×10^{-1} Ω cm while 600 °C-annealed ITO films were used for the source-drain electrodes to achieve a carrier density of 1.0×10^{20} cm^{-3} and a resistivity of 1.8×10^{-2} Ω cm.

Figure 4(a) shows an x-ray diffraction (XRD) spectrum obtained from the PZT/LNO/STO(111) perovskite stacked structure. We annealed LNO and PZT films at 750 °C and 625 °C, respectively because the annealing temperature of LNO film should be higher than that of PZT from a viewpoint of process stability. We found that both LNO and PZT

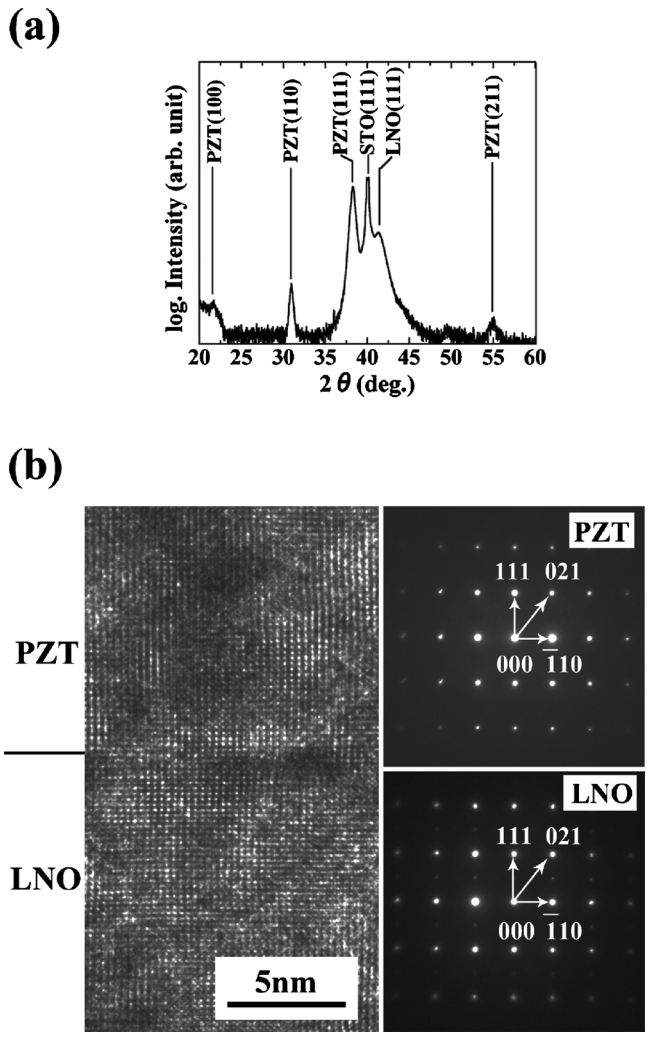

FIG. 4. (a) XRD spectrum from the PZT/LNO/STO stacked structure and (b) cross-sectional TEM image and TED patterns of PZT/LNO stacked structure.

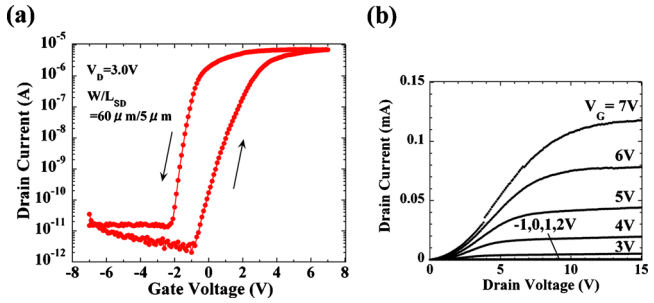

FIG. 5. (Color online) (a) I_D-V_G characteristics and (b) I_D-V_D characteristics of FGT with 20 nm thickness of ITO channel.

films exhibit a (111) preferred orientation that was induced from the single-crystal STO(111) substrate. A cross-sectional transmission electron microscope (TEM) image of PZT/LNO hetero-interface region and transmission electron diffraction (TED) patterns of PZT and LNO films are shown in Fig. 4(b). The TEM image reveals that PZT/LNO interface almost does not have any interfacial layers which would have prevented good crystal growth and electrical properties of the PZT films. A lattice structure in both the LNO and PZT films also can be observed in the TEM image. Clear diffraction spots appeared in the TED patterns, indicating that high-quality crystalline LNO and PZT films were fabricated on STO substrate. The TED images also indicate that PZT(111) was grown on LNO(111), with measured lattice mismatch of less than 5%. These results suggest that local epitaxial growth can be achieved even in the solution-derived hetero-structure.

A remanent polarization (P_r) of 32 $\mu C/cm^2$ was obtained from the polarization-voltage (P-V) hysteresis measurements on ITO/PZT/LNO (200 nm/255 nm/100 nm) capacitors. This is a typical P_r value for a PZT film. On the other hand, according to the carrier concentrations of ITO films shown in Fig. 3, the intrinsic charge per unit area of an ITO film annealed at 450 °C was calculated to be as low as 9.6 $\mu C/cm^2$, which was smaller than the P_r of PZT film. This difference in charge densities indicates that the huge polarization charge of the PZT film could deplete all the electrons in a 20-nm-thick-ITO film. If a paraelectric SiO_2 film was used as a gate insulator, controlling all the charge in ITO channel (9.6 $\mu C/cm^2$) would be impossible because the maximum charge of such an SiO_2 film is generally limited to only 3.5 $\mu C/cm^2$ at the breakdown voltage of around 10 MV/cm.

Figure 5 shows the I_D-V_G [Fig. 5(a)] and I_D-V_D [Fig. 5(b)] characteristics of the fabricated FGT device. For I_D-V_G characteristics, we obtained a typical n-channel transfer curve with a counterclockwise hysteresis loop at low operation voltage (less than ±10 V) owing to the ferroelectric nature of the PZT gate insulator, and for I_D-V_D characteristics we observed good drain current saturation. The obtained on/off current ratio and memory window were about 10^7 and 2.5 V, respectively. Moreover, we obtained good sub-threshold voltage swing of 420 mV/decade, which probably can be attributed to the large equivalent capacitance of the PZT gate insulator.

The field-effect mobility, μ_{FE}, was deduced from $\mu_{FE} = I_{ds}[(W/2L_{SD})C_{ox}\cdot(V_G - V_T)^2]^{-1}$, where I_{ds} is the output current in saturation region, C_{ox} is the equivalent capacitance per unit area of the gate insulator, V_G is the gate voltage, V_T is the threshold voltage, W is the channel width, and L_{SD} is the channel length. We assumed equivalent C_{ox} as $P(V_G)/V_G$ from P-V hysteresis, where $P(V_G)$ is the polarization of the PZT film as a function of the gate voltage. By using the parameters of $P(V_G)=46.4$ $\mu C/cm^2$, $V_G=6.0$ V, $V_T=2.5$ V, $W=60$ μm, and $L_{SD}=5$ μm, we estimated the μ_{FE} of this FGT to be 0.2 cm^2/V s. This apparent low mobility may have been caused by the deficient conductivity of the ITO source-drain electrodes, and this issue could be solved by using a different highly conductive material for electrodes. However, despite the estimated low channel mobility, an adequate on-current was obtained because of the large charge density induced by the ferroelectric-gate insulator.

In summary, we have fabricated a FGT using only CSD process for all its layers, including the gate electrode, gate insulator, source-drain electrodes and channel. This FGT exhibited equivalent or better transistor operation compared with FGTs prepared by means of vacuum deposition processes.[3,4,14,15] In this letter, we suggested that the "total solution process" could be used instead of conventional vacuum processes for fabrication of inorganic TFTs. Use of such a total solution process would represent advancement toward "total printing inorganic electronics" that could enable ultra-low-cost and low-energy fabrication of sophisticated inorganic TFTs and memories.

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